"A SEMICONDUCTOR MEMORY".

The present invention relates to a semiconductor memory which is constructed of a monolithic semiconductor integrated circuit.

In recent years, the demand for a semiconductor memory having a large capacitance is increased greatly with the progress in semiconductor technology and the development in the technique of use for the semiconductor device.

In the case where a Read Only Memory (ROM) having a large capacitance is to be manufactured a number of problems arise.

For example, the number of memory cells to be coupled to data lines is increased with the increase in the memory capacitance. Moreover, the undesired stray or parasitic capacitance, which is liable to be coupled to the data lines, is increased with the increase in the number of the memory cells. As a result, when in a data read out operation, the changing rate of the data signals, which are fed to the data lines by a selected memory cell, is restricted by the relatively large capacitance of the data lines. In other words, the driving ability of the data lines by the selected memory cell is relatively reduced.

The signal lines such as the data lines are frequently elongated when it is intended to increase the memory capacitance. In this case, since the signal lines themselves have not negligible resistances and since undesired capacitances having relatively large values are coupled to the signal lines, these lines experience relatively long signal delays.

In the case where it is desired to manufacture a semiconductor integrated circuit device having a large capacitance, it is desirable to scale down the circuit elements or wiring layers constructing the semiconductor integrated circuit device with a view to achieving a variety of objects such as to prevent a reduction in the fabrication yield being caused by the crystal defect of a semiconductor substrate, the area of the semconductor substrate from being substantially increased, and the power consumption from being greatly increased.

The signal lines thus scaled down have relatively high resistances and hence experience long signal delays.

In order to make the responding rate of a high-capacitance ROM equal to or higher than that of a low-capacitance ROM, it is necessary to eliminate the adverse affections which are caused by the relative reduction in the driving ability of the data lines by the memory cell and by the increase

in the delay time periods of the signal lines.

On the other hand, the defects of the memory cells raise special problems in the high-capacitance ROM.

It is well known from information theory to use an error correcting code which will be shortly referred to as "ECC".

We have conceived that a circuit for correcting error by the use of the aforementioned ECC (which circuit will be shortly referred to as the "ECC circuit") is built in a semiconductor memory.

It is an object of the present invention to provide a semicondcutor memory which is capable of improving the fabrication yield.

It is another object of the present invention to provide a semiconductor memory which is capable of improving the function of built-in ECC circuits and to simplify the circuit construction thereof.

According to the present invention there is provided a semiconductor memory including:

(a) a plurality of memory cells arranged in a matrix form in one semiconductor chip for storing one set of data having check bits;

(b) a selecting circuit for selecting those of said plural memory cells, which are grouped into one set, in response to the address signals; and

(c) an error correcting code circuit formed in said semiconductor chip and adapted to be fed with one set of data which are read out of the memory cells selected,

wherein each set of the data is stored in the plural memory cells which are spaced from each other farther than one of said memory cells.

The present invention will now be described in greater detail by way of example with reference to the accompanying drawings, wherein:-

Figure 1 is a block circuit diagram showing a preferred form of ROM;

Figures 2A, 2B and 2C are specified circuit diagrams showing the circuit blocks DSA_1, $M\text{-}ARY_1$, MPX_1, SA, MPX_3 and DSA_3 of Figure 1;

Figure 3 is a circuit diagram showing an X-decoder;

Figure 4 is a circuit diagram showing a Y-decoder;

Figure 5 is a circuit diagram showing an ECC circuit;

Figure 6 is a circuit diagram showing an exclusive OR circuit; and

Figure 7 is a diagram illustrating the operational waveforms of the circuits of Figures 2A to 2C.

Referring to Figure 1, the ROM shown is equipped with four memory arrays $M\text{-}ARY_1$ to $M\text{-}ARY_4$, and has a memory capacitance of about 1 megabits as a whole. Each of the memory arrays $M\text{-}ARY_1$ to $M\text{-}ARY_4$ is composed of the memory arrays, which are arranged in 512 rows x 608 columns, and has a memory capacitance

of 311,296 bits. The circuit blocks shown are respectively formed in a semiconductor substrate by the well-known MOS circuit integrating technique. The arrangement of the major circuit blocks is made to correspond to the actual geometrical arrangement on the semiconductor substrate.

The insulated gate field effect transistors (which will be shortly referred to as "MOSFETs") for constructing each of the circuit blocks are of an enhancement mode N-channel type unless otherwise specified.

The respective memory arrays $M\text{-}ARY_1$ to $M\text{-}ARY_4$ have their row addresses selected by X decoders $X\text{-}DCR_1$ and $X\text{-}DCR_2$ and their column addresses selected by a Y-decoder $Y\text{-}DCR_1$.

The two X-decoders $X\text{-}DCR_1$ and $X\text{-}DCR_2$ have such word drivers as will become apparent from the following description and generate 2^{10} (= 1024) decoded output signals by decoding row address signals A_0 to A_9. The X-decoder $X\text{-}DCR_1$ is arranged between the two memory arrays $M\text{-}ARY_1$ and $M\text{-}ARY_2$ which are arranged at the left hand side of the drawing, whereas the X-decoder $X\text{-}DCR_2$ is arranged between the memory arrays $M\text{-}ARY_3$ and $M\text{-}ARY_4$ which are arranged at the right hand side of the drawing. The 512 decoded output signals generated by the X-decoder $X\text{-}DCR_1$ are applied commonly to the memory arrays $M\text{-}ARY_1$

and M-ARY$_2$. Likewise, the 512 decoded output signals generated by the X-decoder X-DCR$_2$ are applied commonly to the memory arrays M-ARY$_3$ and M-ARY$_4$.

A Y decoder Y-DCR$_1$ generates 32 decoded output signals by decoding column address signals A_{10} to A_{14} of five bits. Multiplexers MPX$_1$ to MPX$_4$ are respectively coupled to the memory arrays M-ARY$_1$ to M-ARY$_4$. The multiplexors MPX$_1$ to MPX$_4$ are made operative to act as column switches. Each of the multiplexors MPX$_1$ to MPX$_4$ is fed with the 32 decoded signals of the Y-decoder Y-DCR$_1$. One is selected from 32 columns by each of the multiplexors MPX$_1$ to MPX$_4$. Since each of the memory arrays M-ARY$_1$ to M-ARY$_4$ has 608 columns, 19 columns are simultaneously selected from each memory array in response to one Y-decoded output signal.

In accordance with the construction so far described, 38 memory cells are simultaneously selected in response to one X-decoded output signal and one Y-decoded output signal.

A sense amplifier SA for amplifying the information signal (or the data signal) which is generated by the memory cell selected is constructed of a differential circuit. The sense amplifier SA is made operative to amplify the voltage difference between the data signal, which is read out of the memory cell, and a predetermined reference

voltage. In order to cause the voltage difference, which is to be amplified, to accurately correspond to the content of the data signal read out of the memory cell and to reach a desired level within a relatively short period of time, the reference voltage is set not at an absolutely constant level but at a relative level. In other words, the reference voltage is set at such a value as to correspond to the potential at the column to which the memory cell selected is coupled.

The column lines of the memory arrays are fed with reference voltage. In order to set the reference voltage at a proper level, there are provided dummy cell arrays DSA_1 to DSA_4 which respectively correspond to the memory arrays $M\text{-}ARY_1$ to $M\text{-}ARY_4$. The dummy cell arrays DSA_1 to DSA_4 are coupled to the column lines of the corresponding memory arrays. The dummy cell arrays DSA_1 and DSA_2 are respectively selected by the X decoders $X\text{-}DCR_1$ and $S\text{-}DCR_2$.

The dummy cell arays DSA_1 and DSA_2, which are arranged at the left hand side of Fig. 1, and the dummy cell arrays DSA_3 and DSA_4, which are arranged at the right hand side, are alternatively selected

in response to the highest bit signal A_9 of the X address signals A_0 to A_9 of 10 bits

The dummy cell arrays DSA_1 and DSA_2, which are coupled to the memory arrays $M\text{-}ARY_1$ and $M\text{-}ARY_2$, are selected when the respective row lines of the memory arrays $M\text{-}ARY_3$ and $M\text{-}ARY_4$ are selected by the X-decoder $X\text{-}DCR_2$. On the contrary, the dummy cell arrays DSA_3 and DSA_4, which are coupled to the memory arrays $M\text{-}ARY_3$ and $M\text{-}ARY_4$, are selected when the respective row lines of the memory arrays $M\text{-}ARY_1$ and $M\text{-}ARY_2$ are selected.

The respective column lines of the memory array $M\text{-}ARY_1$ of Fig. 1 are paired with the respective column lines of the memory array $M\text{-}ARY_3$. On the other hand, the multiplexor MPX_1 is paired with the multiplexor MPX_3. In the data read out operation, the same signal as that which is fed from the Y-decoder $Y\text{-}DCR_1$ to the multiplexor MPX_1 is also fed to the multiplexor MPX_3. As a result, the sense amplifier SA is fed with the data signal to be amplified by way of one of the multiplexors MPX_1 and MPX_3 and with the reference voltage by way of the other multiplexor. Likewise, the column lines of the memory array $M\text{-}ARY_2$ are paired with the column lines of the memory array $M\text{-}ARY_4$, and the multiplexors MPX_2 and MPX_4 are paired

with each other.

The data signals of 38 bits, which are read out of the 38 memory cells selected in response to one of the X-decoded output signals and one of the Y-decoded output signals, are amplified by the sense amplifier SA and are fed to an ECC circuit so that their errors are corrected by the ECC circuit. In the signals of 38 bits fed to the ECC circuit, the 32 bits are used as the data signals whereas the remaining 6 bits are used as the parity signals. In response thereto, the ECC circuit generates the data signals of 32 bits, which have their errors corrected.

The information signals (or the output data) of 32 bits having their errors corrected by the ECC circuit are fed to a multiplexor MPX_0 which is provided to reduce the number of the external terminals of the ROM. The respective 8 bits of the output data signals of 32 bits are selected by the action of the multiplexor MPX_0. The data signals of 8 bits are fed through an output buffer DOB to the external terminals DO_0 to DO_7 of the ROM. As a result, the data signals of 32 bits of the ECC circuit are transferred sequentially four times to the external terminals DO_0 to DO_7. For these sequential output operations, address signals A_{15} and A_{16} are used. The ROM

is equipped with a Y decoder Y-DCR$_2$ for decoding the address signals A_{15} and A_{16}. The multiplexor MPX$_0$ has its operations controlled by the decoded signals which are generated by the Y decoder Y-DCR$_2$. As a result, the data signals of 32 bits are consecutively fed to the external terminals DO$_0$ to DO$_7$ in accordance with the fact that the states of the address signals A_{15} and A_{16} of 2 bits are consecutively changed.

The ROM is also equipped with an address buffer ADB. This address buffer ADB receives the external address signals A_0 to A_{16} through the external terminals in order to generate the internal address signals a_o and $\bar{a}_0$ to a_{16} and $\bar{a}_{16}$ at true and false levels, which signals are to be fed to the decoders. The address buffer ADB has its operations controlled by a chip select signal Ce which is fed from a control circuit CNT.

This control circuit CNT generates the chip select signal Ce in response to an external chip select signal CE which is to be fed to the external terminals. The control circuit CNT is provided with a signal generator (not shown) for generating precharge pulses ϕ_{pc} and with such signal generators ϕ_x-Gen and ϕ_y-Gen as will become apparent from Figures 3 and 4.

The address signals which are required by the internal signal generators of the control circuit CNT are fed from the address buffer ADB.

The signal generator for generating the precharge pulses ϕ_{pc} can be constructed of a circuit for detecting the change in the level of at least one of the address signals A_0 to A_{16} and a suitable circuit such as a pulse generating circuit. The precharge pulses ϕ_{pc} are set at a high level for a predetermined period of time when the chip select signals are fed to the terminal CE and when at least one of the signals A_0 to A_{14} of the address signals A_0 to A_{16} is changed while the chip select signals are being fed.

To the memory arrays, there are respectively coupled such precharge elements as will be made apparent from the later description. The data lines (i.e., the column lines) of the respective memory arrays are reset by the fact that the precharge elements are operated by the precharge pulses ϕ_{pc}. The data can be read out at high speed by the fact that the respective data lines are forcibly reset irrespective of their previous levels. The precharge pulses ϕ_{pc} are also used for resetting the sense amplifier.

The ROM is used as a character generator for producing Chinese characters. The pattern of one character is displayed with display dots which are arranged in a matrix form of 32 rows and 32 columns, for example. Since one letter requires the data signals of 32 bits x 32 bits, the ROM can be stored with 1024 character patterns.

Referring now to the specific circuits of the memory arrays and the sense amplifier shown in Figures 2A to 2C, the memory arrays $M\text{-}ARY_1$ and $M\text{-}ARY_3$ are made to have a substantially identical construction. The memory array $M\text{-}ARY_1$ has 512 word lines W_0 to W_{511} which are elongated in the vertical direction of Figure 2A. The 512 word lines of the memory array $M\text{-}ARY_1$ are made common with the 512 word lines of the memory array $M\text{-}ARY_2$ which is shown in Figure 1. Likewise, the memory array $M\text{-}ARY_3$ has 512 word lines which are elongated in the vertical direction. The 512 word lines of the memory array $M\text{-}ARY_3$ are also made common with the 512 word lines which are provided in the memory array $M\text{-}ARY_4$ shown in Figure 1. The respective word lines are deemed as row lines. The memory array $M\text{-}ARY_1$ has an earth line and a data line which are elongated in the horizontal direction of Figure 2A and which are alternately arranged. As shown, the

first line G_{a0} is the earth line whereas the second line D_{a0} is the data line. In Figure 2A, the respective earth lines are designated at suffix G whereas the respective data lines are designated at suffix D.

The data lines respectively construct the column lines. The memory array M-ARY_1 of Figure 1 has the 608 column lines, as has been described above. In the memory array M-ARY_1 of Figure 2A, however, one data line is made to substantially correspond to two column lines, as will become apparent from the following description. As a result, the number of the data lines belonging to the memory array M-ARY_1 is set at not 608 but half that amount i.e. 304. The ROM can be highly integrated by reducing the number of the data lines. The respective data lines of the memory array M-ARY_1 are coupled through the multiplexor MPX_1 to common data lines CD_0 and CD_1 and so on. Since the substantial one data line constructs the two column lines, 16 (i.e. 32/2) data lines D_{a0} to D_{a15} are made to correspond to one common data line, e.g. CD_0.

In the memory array M-ARY_1, memory MOSFETs M_0 to M_{31} are formed to respectively correspond to the nodes of the word and data lines. Each of the

memory MOSFETs has its gate connected with the corresponding word line, its drain connected with the corresponding data line and its source connected with the corresponding earth line. With the respective data lines and the respective earth lines with the exception of the earth line G_{a0} which is arranged at the end portion of the memory array M-ARY_1, there are commonly connected the drains and sources of the respective memeory MOSFETs M_0, M_1, M_2 and so on which are connected with an identical word line. The earth lines and the data lines are constructed of the semiconductor regions which are integrally formed with the semiconductor regions constructing the sources and drains of the memory MOSFETs. Each of these memory MOSFETs has its threshold voltage predetermined in response to the information "0" or "1".

The multiplexor MPX_1 is constructed of: transmission gate MOSFETs which are substantially interposed between the data lines and the common data line; and switch MOSFETs which are interposed between the respective earth lines and a common earth line CG_a. The data lines D_{a0} to D_{a15} are coupled to the common data line CD_0 through transmission gates MOSFETs S_{a0} to A_{a15} which construct the multiplexor. The common data line CD_0 is connected with one of the input terminals of the sense amplifier. The earth lines G_{a0} to G_{a15} are connected with the common

earth line CG_a through switch MOSFETs Q_{a0} to Q_{a15} which act as column switches.

The MOSFETs S_{a0} to S_{a15} have their gates respectively fed with the decoded signals C_0 to C_{15} which are generated by the Y address decoder $Y\text{-}DCR_1$ shown in Figure 1. The decoded signals C_0 to C_{15} are generated by decoding the address signals A_{10} to A_{13}. The MOSFETs Q_{a0} to Q_{a15} have their gates fed with the decoded signals C_0 to C_{15} and the decoded signals C_{01} to C_{1500} which are generated by logical circuits (not shown) which are made receptive of the address signal A_{14}. It is necessary to complementarily switch the switch MOSFET, which is coupled to the earth line arranged at one side of the data line to be selected, and the switch MOSFET which is coupled to the earth line arranged at the other side of that data line. It is also necessary to render the switch MOSFET, such as the MOSFET Q_{a1}, conductive, which MOSFET is coupled to the earth line interposed between the two data lines, when the memory MOSFET interposed between that earth line and one of the data lines is to be selected and when the memory MOSFET interposed between that earth line and the other data line is to be selected. For example, the decoded signal C_{1500} is preset at such a value as to satisfy the relationship expressed by the following logical equation (1), whereas the

decoded signal C_{01} is similarly preset at such a value as to satisfy the relationship expressed by the following logical equation (2):

$$C_{1500} = C_0 \cdot \overline{a_{14}} + C_{15} \cdot a_{14} \quad \text{- - - - - - - - (1);}$$

and

$$C_{01} = C_0 \cdot a_{14} + C_1 \cdot \overline{a_{14}} \quad \text{- - - - - - - - - (2).}$$

In Figure 2A, the earth lines, which are arranged above the respective data lines D_{a0} to D_{a15}, are selected by the AND signals of the decoded signals C_0 to C_{15} and the internal address signal $\overline{a_{14}}$, whereas the earth lines, which are arranged below the respective data lines D_{a0} to D_{a15}, are selected by the AND signals of the decoded signals C_0 to C_{15} and the address signal a_{14}.

The dummy cells DS_{a0} to DS_{a31} are respectively coupled to the data lines, the dummy cells having an identical construction. In Figure 2A, only the circuit of the dummy cell DS_{a0} is specifically shown so as to simplify the illustration. The dummy cell DS_{a0} is constructed of: MOSFETs Q_{d1} and Q_{d2} which are connected in series with each other and which are adapted to be switched by an internal address signal a_a; and a MOSFET Q_s which is connected in series with the MOSFETs Q_{d1} and Q_{d2} and which is adapted to be switched by the decoded signal C_0.

The MOSFETs Q_{d1} and Q_{d2} are designed to have the same size as that of the memory MOSFETs of the

memory array. Moreover, the MOSFETs Q_{d1} and Q_{d2} are fabricated simultaneously with and in the same size as those of the memory MOSFETs, which have a low threshold voltage. As a result, the composed conductance of these MOSFETs Q_{d1} and Q_{d2} when rendered conducting is made to have about a half value of the conductance of the MOSFET having the low threshold voltage when the latter is selected. Those of the memory MOSFETs, which have a high threshold voltage, are held in their substantially conducting states irrespective of whether they are selected or not. As a result, the composed conductance of the MOSFETs Q_{d1} and Q_{d2} of the dummy cells is made to have a higher conductance of the memory MOSFET having a high threshold voltage when the latter is selected. In other words, the composed conductance of the MOSFETs Q_{d1} and Q_{d2} takes an intermediate value between the conductance of the memory MOSFET having the low threshold voltage and the conductance of the memory MOSFET having the high threshold voltage.

The MOSFET Q_s of the dummy cell is provided to reduce the power consumption at the dummy cells which need not be selected. The MOSFET Q_s has its size so selected as to have a sufficiently higher conductance than the combined conductances of the MOSFETs Q_{d1} and Q_{d2}. As a result, the conductance of the dummy cell in the selected state, i.e., the conductance between the output node DN of the dummy cell and the earth

potential point of the circuit is substantially equal to the combined conductances of the MOSFETs Q_{d1} and Q_{d2}.

As has been described above, the MOSFETs Q_{d1}, Q_{d2} and Q_s which constitute the dummy cell are formed simultaneously with the memory MOSFETs. As a result, it is possible to avoid an increase in the number of the manufacture steps when constructing the ROM. Moreover, it is possible to make effective use of such well-known features of the fabrication technique of the semiconductor integrated circuit device that there are few characteristic dispersions between the circuit elements which are simultaneously formed. More specifically, in the case of the characteristics of the memory MOSFETs, e.g. the conductances thereof are changed by the dispersions in the fabrication conditions, similar characteristic changes occur in the MOSFETs Q_{d1} and Q_{d2}. As a result, the combined conductances of the MOSFETs Q_{d1} and Q_{d2} can be reduced to about a half of the conductance of the memory MOSFETs having the low threshold voltage without being substantially influenced by the dispersions in the fabrication conditions. Thus, it is possible to fabricate a memory which can enjoy a high yield.

Precharge MOSFETs Q_{P0}, Q_{P1}, Q_{P2} are respectively coupled to the data lines, which MOSFETs are adapted to be switched by the precharge

pulses ϕ_{pc}. These precharge pulses ϕ_{pc} are generated by the control circuit CNT shown in Figure 1, as has been described above. The precharge pulses ϕ_{pc} are set, as has been described above, at the high level for a predetermined period of time when the address signals to be fed from the address buffer ADB. The control circuit CNT also generates the chip select signal Ce which is to be fed to such circuits as are shown in Figures 3 and 4. The chip select signal Ce is set at a high level in accordance with the fact that the chip select signal CE coming from the outside of the IC is at a high level. The chip select signal Ce thus set is fed to the address buffer, the decoders and other blocks. These blocks are activated in response to the high level of the chip select signal Ce and in activated in response to the low level of the same signal. Thus, the unnecessary power consumption of the ROM as a whole can be reduced by the controls of the respective circuits by the chip select signal Ce.

Referring now to Figure 2B, a sense amplifier SA_{d0} is constructed of: latch type amplifying MOSFETs Q_4 and Q_5 which have their gates and drains cross-linked; and precharge MOSFETs Q_6 and Q_7 which are connected with the respective

drains of the MOSFETs Q_4 and Q_5.

Since the precharge MOSFETs Q_6 and Q_7 are made to have relatively high conductances, the paired input and output terminals of the sense amplifier SA_{d0} are precharged to a high level when the precharge pulses ϕ_{pc} are generated, which level is substantially equal to a power source voltage V_{cc}. The paired input and output terminals of the sense amplifier SA_{d0} are fed with the output signals which come from the corresponding left and right hand memory arrays $M\text{-}ARY_1$ and $M\text{-}ARY_3$ by way of the common data lines CD_0 and $\overline{CD_0}$.

Likewise, the sense amplifier SA_{d1} is fed with the output signals which come from the memory arrays $M\text{-}ARY_1$ and $M\text{-}ARY_3$ through the common data lines CD_1 and $\overline{CD_1}$.

In each of the memory arrays, the writing operation of the information in the memory MOSFETs is conducted by implating impurity ions in the regions which are to be formed the channels of the memory MOSFETs. In other words, the threshold voltage of the memory MOSFETs is determined by the impurity ion implantations. Into the channel-formed regions of the memory MOSFETs required to have the high threshold voltage, for

example, there are implanted the impurity ions which have the conduction type inverted from that channel conduction type. No ion implantation for shifting the threshold value is conducted into the channel-formed regions of the memory MOSFETs which are required to have the low threshold voltage. As a result, the binary signal "1" or "0" can be written in the memory MOSFETs. In this case, the threshold voltage of the memory MOSFETs, which is determined by the ion implantations, is made to correspond to the value "1" of the binary signal. The low threshold voltage of the memory MOSFETs into which no ion has been implanted is made to correspond to the value "0" of the binary signal.

The read out operations are conducted by detecting whether the memory MOSFETs are rendered substantially conducting or non-conducting, when they are selected, by the voltage applied between their gates and sources. In other words, the read out operations correspond to the detection of whether the conductance of the memory MOSFET selected is high or low. The reference for this detection of the level is given by the dummy cells,

as has been described above.

Next, the operations of the mask type ROM will be described.

Now, it is assumed that those of the decoded signals generated by the X decoder $X\text{-}DCR_1$ shown in Figure 1, which are to be fed to the word line W_0, for example, are set at the high level together with those C_0 of the decoded signals generated by the Y decoder $Y\text{-}DCR_1$ shown in Figure 1 by the suitable combinations of the address signals A_0 to A_{13}. With this assumption, the transfer MOSFETs S_{a0}, S_{a16} and so on, which are coupled to the data lines D_{a0}, D_{a16} and so on, are rendered conductive by the action of the decoded signal C_0. Accordingly, the memory MOSFETs M_0 and M_1, and M_{32} and M_{33}, which have their drains coupled to the data lines D_{a0} and D_{a16} and their gates coupled to the word line W_0, are brought into their states in which they can be selected.

It is determined by the address signal A_{14} which memory MOSFET M_0 or M_1 is to be selected and which the MOSFET M_{32} or M_{33} is to be selected. For example, in the case where the internal address signal a_{14} is set at the high level in accordance with the fact that the address signal A_{14} is set at the high level, the decoded output signal C_{01} of the Y decoder $Y\text{-}DCR_1$ is accordingly set at the high level. As a result, the switch MOSFETs Q_{a1},

Q_{a17} and so on are rendered conductive so that the earth lines G_{a1}, G_{a17} and so on are set at the earth potential of the circuit. As a result, the potential at the word line W_0 is applied between the gate and source of the memory MOSFET M_1 of the two memory MOSFETs M_0 and M_2. In short, the memory MOSFET M_1 is selected. And, the MOSFET M_{33} is likewise selected from those MOSFETs M_{32} and M_{33}.

When the word line W_0 is selected, incidentally, none of the decoded signals which will raise the potentials of the word lines W_{512} to W_{1023} of the memory array M-ARY_3 to the high level is generated by the X decoder X-DCR_2, as has been described above. As a result, none of the memory MOSFETs constituting the memory array M-ARY_3 is selected.

The selection of the dummy cells will now be described in greater detail. As has been described above, the memory array M-ARY_1 is selected by the low level of the highest address signal A_9 of the address signals A_0 to A_9 of 10 bits, which are fed to the X decoder. At this time, in accordance with the address signal A_9, the internal address signal $\overline{a_9}$ is set at the high level whereas the address signal a_9 is set at the low level. On the contrary, the memory array M-ARY_3 is selected by the high level of the highest address signal A_9.

Thus, in the case where the address signals A_0 to A_9 are so set that the memory MOSFET M_1 coupled to the word line W_0 in the memory array M-ARY$_1$ may be selected, the MOSFETs Q_{d1} and Q_{d2} of the respective dummy cells constituting the dummy cell array DSA_3 are rendered conducting by the high level of the internal address signal $\overline{a_9}$. As a result, the dummy cell array DSA_3 is brought into its selectable state. At this time, the dummy cell array DSA_1 is not brought into its selectable state because the address signal a_9 is at the low level.

As has been previously described, the predetermined ones of the respective dummy cells, which constitute the dummy cell array DSA_3 in its selectable state, are selected. In order to select the data lines, more specifically, the respective decoded signals generated by the Y decoder Y-DCR$_1$ are also fed to the MOSFET Q_s of each dummy cell. As a result, in the case where the memory MOSFETs M_1, M_{32} and so on coupled to the word line W_0 are selected, the dummy cells DS_{b0}, DS_{b16} and so on, which are coupled to the data lines D_{b0}, D_{b16} and so on of the memory array M-ARY$_3$, are accordingly selected. The dummy cells coupled to the other data lines DS_{b1} to DS_{b15} are left unselected. As a result, of the parasitic

capacitances, which are coupled to the respective data lines D_{b0}, D_{b31} and so on precharged through the precharge MOSFETs, the parasitic capacitances coupled to the data lines D_{b0}, D_{b15} and so on do not have their charges discharged through the dummy cells. Thus, it is possible to eliminate the ineffective power consumption.

The memory MOSFET M_1 has a conductance which can be determined in accordance with the memory information given, as has been described above. As a result, the charges at the data line D_{a0}, which has been precharged through the precharge MOSFET Q_{P0}, begins to be released, when the memory MOSFET M_1 is selected, in accordance with the information which has been stored in that MOSFET M_1.

The dummy cell DS_{b0}, which is selected simultaneously with the memory MOSFET M_1, has an intermediate conductance between the conductance of the memory MOSFET, which is stored with the information "1", and the conductance of the memory MOSFET which is stored with the information "0", as has been described above. As a result, the charge at the data line D_{b0}, which has been precharged through the precharge MOSFET, begins to be released, when the dummy cell DS_{b0} is selected, in accordance with the conductance of that dummy cell.

Figure 7 illustrates the changing behaviours of the potentials V_D and $V_{\bar{D}}$ at the paired data lines D_{a0} and D_{b0} with the time. A broken line illustrates the potential change of the data line D_{b0} to which the dummy cell is coupled. On the other hand, a single-dotted line illustrates the potential change of the data line D_{a0} when the memory MOSFET M_1 is stored with the information "0", whereas a double-dotted line illustrates the potential change of the data line D_{a0} when the memory MOSFET M_1 is stored with the information "1".

The sense amplifier SA_{d0} amplifies the potential difference between the paired data lines D_{a0} and D_{b0} in order to feed its amplified signal to common data lines D_0' and $\overline{D_0'}$.

In this case, the lines D_{a2} to D_{a15} of the data lines D_{a1} to D_{a15} of the memory array $M\text{-}ARY_1$ do not have their corresponding earth lines selected. As a result, the precharge level of the data lines D_{a2} to D_{a15} is held as it is in order to prevent any ineffective current consumption from being caused.

The data line D_{a1} is discharged in response to the fact that the memory MOSFET M_2 is rendered conductive by the selection of the word line W_0, for example, because the MOSFET Q_{a1} is conducting.

As a result, the ineffective power consumption, which would be caused if the charge of the data line left unselected, is substantially reduced.

Referring now to Figures 5 and 6, the binary signal inverted from the binary signal to be stored is written in the memory MOSFETs constituting the memory arrays M-ARY$_3$ with a view to reducing both the number of the elements constituting the ECC circuit and the power consumption in the ECC circuit. More specifically, in the case of the memory MOSFET M_0 of the memory array M-ARY$_3$, for example, is to be stored with the binary signals "1", it is written with the binary signal "0" which is inverted from the binary signal "1". By this writing operation, a level corresponding to the binary signal stored in the memory MOSFET is always fed from the left hand input and output terminals of the sense amplifier, no matter whichever memory array M-ARY$_1$ or M-ARY$_3$ might allow its memory MOSFET to be selected. From the right hand input and output terminals of the sense amplifier, on the other hand, there is fed a level which corresponds to the binary signal inverted from the above referred to one.

Figure 3 is a circuit diagram showing the embodiments of the X-address decoders X-DCR$_1$ and X-DCR$_2$ of Figure 1.

The X-address decoder $X\text{-}DCR_1$ is constituted by a plurality of unit decoders UD_{x0} to UD_{x511} which are made to correspond one-to-one to the word lines W_0 to W_{511}, whereas the X address decoder $X\text{-}DCR_2$ is constituted by a plurality of unit decoders UD_{x512} to UD_{x1023} which are similarly made to correspond one-to-one to the word lines W_{512} to W_{1023}.

The respective unit decoders UD_{x0} to UD_{x1023} have constructions which are identical to each other. Figure 3 only shows the circuit of the unit decoder UD_{x0}.

Referring to Figure 3, the unit decoder UD_{x0} is constructed of: logical MOSFETs Q_{10} to Q_{19} which are supplied with a predetermined combination of the address signals a_0 and $\overline{a_0}$ to a_9 and $\overline{a_9}$; a precharge MOSFET Q_{20} which is connected between the common drain of the former two MOSFETs and the power source terminal V_{cc}; a cut MOSFET Q_{21}; and an output MOSFET Q_{22} which is supplied with the decoded signal through the cut MOSFET Q_{21}.

The precharge MOSFET Q_{20} has its gate fed with the control signal (i.e. the chip select signal) Ce, whereas the output MOSFET Q_{22} has its drain fed with the output of the signal generator ϕ_x-Gen.

This signal generator ϕ_x-Gen is made operative to generate its signal at a high level in response to the address signals a_0 and $\overline{a_0}$ to

a_9 and $\overline{a_9}$ if even one group of the address signals a_0 and $\overline{a_0}$ to a_9 and $\overline{a_9}$ have their levels varied.

The output of the unit decoder UD_{x0} will now be described in greater detail. If all the address signals A_0 to A_9 fed to the external terminals, for example, are varied to the low level, the address signals a_0 to a_9 to be generated by the address buffer ADB shown in

Fig. 1 are accordingly varied to the low level, whereas the address signals $\overline{a_0}$ to $\overline{a_9}$ are accordingly varied to the high level. As a result, all the parallel-connected MOSFETs Q_{10} to Q_{19} are rendered non-conductive. The common drains of the MOSFETs Q_{10} to Q_{19} are set at the precharge level, i.e., the high level, as a result of the fact all of them are non-conductive. The high-level signal of the common drain is fed through the cut MOSFET Q_{21} to the gate of the output MOSFET Q_{22}. As a result, the output MOSFET Q_{22} is rendered non-conductive.

That output signal of the signal generator ϕ_x-Gen, which is preset at the low level, is raised to the high level for a predetermined time period in accordance with the fact that the address signals are varied in the above manner. This high-level output signal of the generator ϕ_x-Gen is transmitted through the output MOSFET Q_{22} to the word line W_0. In other words, the word line W_0 is set at the select level. As a result, it is possible to select the memory MOSFET which is coupled to that word line W_0.

In the unit decoder UD_{x0}, a parasitic capacitance (not shown) exists between the gate and source of the output MOSFET Q_{22}. This parasitic capacitance

is charged through the cut MOSFET Q_{21}. When the output of the signal generator ϕ_x-Gen is varied to the high level after the parasitic capacitance has been charged, the word line W_0 has its signal accordingly varied to the high level. Since the parasitic capacitance substantially acts as a bootstrap capacitance, the gate potential of the MOSFET Q_{22} is boosted to have a sufficiently high level as a result that the word line W_0 is raised to the high level. As a result, the conductance of the output MOSFET Q_{22} is increased to a sufficiently high level. The cut MOSFET Q_{21} is automatically rendered non-conductive by the bootstrap voltage fed from the parasitic capacitance, because its gate is maintained at the level of the power source voltage V_{cc}. As a result, the cut MOSFET Q_{21} acts to prevent the charge of the parasitic capacitance from being discharged.

When the output of the signal generator ϕ_x-Gen is returned from the high level to the low level, the word line W_0 is accordingly lowered to the low level through the output MOSFET Q_{22}.

In the case where at least one of the address signals A_0 to A_9 is boosted to the high level, at least one of the MOSFETs Q_{10} to Q_{19} of the unit decoder UD_{x0}

is accordingly rendered conductive. The common drain of the MOSFETs Q_{10} to Q_{19} is maintained at the low level even if the MOSFET Q_{20} is rendered conductive by the precharge pulses Ce. The output MOSFET Q_{22} is rendered non-conductive by the low-level signal at the common drain. As a result, the word line W_0 is maintained at the low level.

Referring now to Figure 4 which shows one embodiment of the circuit of the Y address decoder $Y\text{-}DCR_1$ shown in Figure 1, the Y decoder $Y\text{-}DCR_1$ is constructed of unit decoders UD_{y0} to UD_{y15} and logical circuits LG_0 to LG_{15}.

The unit decoders and the logical circuits have constructions respectively identical to one another. Figure 4 specifically shows the constructions of the unit decoder UD_{y0} and the logical circuit LG_0.

The unit decoder UD_{y0} is constructed of: logical MOSFETs Q_{30} to Q_{33} which are connected in parallel with one another and which are supplied with a predetermined combination of the address signals a_{10} and $\overline{a_{10}}$ to a_{13} and $\overline{a_{13}}$; a precharge MOSFET Q_{34} which is connected with the common drains of the former MOSFETs; a cut MOSFET Q_{35} and an output MOSFET Q_{36} which is supplied with the decoded signals

through the cut MOSFET Q_{35}. The output MOSFET Q_{36} has its drain coupled to the output terminal of the signal generator ϕ_y-Gen. The signal generator ϕ_y-Gen has a construction similar to that of the generator ϕ_x-Gen as to generate a high-level signal for a predetermined time period if any one group of the address signals a_{10} and $\overline{a_{10}}$ to a_{14} and $\overline{a_{14}}$ has its level varied.

The output signals C_0 to C_{15} of the respective unit decoders of Fig. 4 are partly used as the select signals of the multiplexors shown in Fig. 1 and partly applied to the gates of the MOSFETs Q_{37} and Q_{38} of the logical circuits LG_0 to LG_{15}. The MOSFETs Q_{37} and Q_{38} of the respective logical circuits have their drains respectively fed with the address signals a_{14} and $\overline{a_{14}}$. From the sources of the respective MOSFETs Q_{37} and Q_{38} of each of the logical circuits, there are generated the decoded signals C_0, C_{1500} and so on which act as the AND outputs.

For example, if the address signals A_{10} to A_{13} are varied to the low level whereas the address signal A_{14} is varied to the high level, the internal address signals a_{10} to a_{13} and $\overline{a_{14}}$ fed from the address buffers shown in Fig. 1 are accordingly varied to the low level, whereas the address signals $\overline{a_{10}}$ to

$\overline{a_{13}}$ and a_{14} are accordingly varied to the high level so that the parallel-connected MOSFETs Q_{30} to Q_{33} of the unit decoder UD_{y0} are rendered non-conductive whereas the output MOSFET Q_{36} is rendered conductive.

At this time, the high-level signal is generated from the signal generator ϕ_y-Gen by the changes in the address signals. This high-level signal of the generator ϕ_x-Gen is transmitted to the gates of the MOSFETs Q_{37} and Q_{38} through the output MOSFET Q_{36} of the unit decoder UD_{y0}. As a result, the MOSFET Q_{38} is rendered conductive. The high-level address signal a_{14} fed to the drain of the MOSFET Q_{38} is fed out through the same MOSFET Q_{38}. In short, the high-level output signal C_0 and the high-level decoded signal C_{01} are generated by the decoder $Y\text{-}DCR_1$.

Referring now to Figure 5, which is a circuit diagram shown one embodiment of the ECC circuit of Figure 1, a logical operation circuit ELG responds to the read signals D_0' and $\overline{D_0'}$ to D_{31}' and $\overline{D_{31}'}$, and P_0 and $\overline{P_0}$ to P_5 and $\overline{P_5}$ of 38 bits from the memory arrays in order to form the syndromes S_0 to S_5 for designating the error bits from a predetermined combination of exclusive ORs.

The respective parity check bits P_0 to P_5 of

6 bits of the information of 38 bits written in the memory arrays have their values predetermined by the data signals of 32 bits and a suitable check matrix.

The following Table 1 tabulates one example of the check matrix:

Table 1 Check Matrix

Syndromes \ Bit No.	Information Bits															
	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	D_9	D_{10}	D_{11}	D_{12}	D_{13}	D_{14}
S_0	1	1	1	1	1										1
S_1	1					1	1	1	1						1
S_2		1				1				1	1	1			1
S_3			1				1			1			1	1	
S_4				1				1			1		1		
S_5					1				1			1		1	

(Continued)

Information Bits

D_{15}	D_{16}	D_{17}	D_{18}	D_{19}	D_{20}	D_{21}	D_{22}	D_{23}	D_{24}	D_{25}	D_{26}	D_{27}	D_{28}	D_{29}	D_{30}	D_{31}
1	1	1	1	1	1	1							1	1		
1	1	1					1	1	1	1					1	
			1	1			1	1			1	1	1		1	1
1			1		1	1	1		1		1	1				
	1			1	1			1		1	1			1		1
		1				1			1	1		1	1	1	1	1

(Continued)

Parity Bits					
P_0	P_1	P_2	P_3	P_4	P_5
1					
	1				
		1			
			1		
				1	
					1

In the Table 1, flags 1 are attached to the bits to be referred to.

The following table 2 tabulates a specified example of the written data W which are to be written in the memory arrays. In the Table 2, incidentally, characters B_0 to B_{31} are attached to the data signals, whereas characters BP_0 to BP_5 are attached to the parity signals.

Table 2 (W)

B_0	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8	B_9	B_{10}	B_{11}	B_{12}	B_{13}	B_{14}	B_{15}	B_{16}
1	1	1	1	1	0	0	0	0	0	0	0	0	0	1	1	1

(Continued)

B_{17}	B_{18}	B_{19}	B_{20}	B_{21}	B_{22}	B_{23}	B_{24}	B_{25}	B_{26}	B_{27}	B_{28}	B_{29}	B_{30}	B_{31}
1	1	1	1	1	0	0	0	0	0	0	1	1	0	0

(Continued)

BP_0	BP_1	BP_2	BP_3	BP_4	BP_5
1	1	1	1	1	1

The values of the respective parity bits are determined by the fact that those bits of the data signals of 32 bits to be written in, which are designated by the Table 1, are referred to. The parity bits to be determined are set at such values that the exclusive OR values of the bit signals referred to and the parity bits to be determined take "0". In other words, the respective parity bits are so determined that the exclusive OR values of the bits to be referred to in view of the Table 1 take "0".

For example, the parity bit BP_0 of the Table 2 is set in the following manner. In order to set the parity bit BP_0, more specifically, the data bits B_0 to B_4, B_{14} to B_{21}, B_{28} and B_{29} of the data bits B_0 to B_{31} of 32 bits are referred to in accordance with the first row (i.e., the syndrome S_0) of the Table 1. The exclusive OR of the data bits thus referred take the value "1". In accordance with this, the parity bit BP_0 take the value "1". In other words, the exclusive OR between the data bits referred to and the parity bit BP_0 is made to take

the value "0".

In the following, the data are referred to on the basis of the syndromes S_1 to S_5 appearing in the second to fifth rows of the Table 1 so that the parity bits BP_1 to BP_5 are so determined as to have their exclusive OR values reduced to "0".

In the case where the respective data bits of 32 bits are set to have the values of the Table 2, all the parity bits BP_0 to BP_5 are made to have the value "1", as tabulated in the same Table.

As is apparent from the Table 1 and the above explanations relating thereto, the logical equations for determining the syndromes S_0 to S_5 are expressed by the following equations (3) to (8):

$$S_0 = B_0 \oplus B_1 \oplus B_2 \oplus B_3 \oplus B_4 \oplus B_{14} \oplus B_{15} \oplus B_{16} \oplus B_{17} \oplus B_{18} \oplus B_{19} \oplus B_{20} \oplus B_{21} \oplus B_{28} \oplus B_{29} \oplus BP_0 \quad \cdots (3);$$

$$S_1 = B_0 \oplus B_5 \oplus B_6 \oplus B_7 \oplus B_8 \oplus B_{14} \oplus B_{15} \oplus B_{16} \oplus B_{17} \oplus B_{22} \oplus B_{23} \oplus B_{24} \oplus B_{25} \oplus B_{30} \oplus BP_1 \quad \cdots (4);$$

$$S_2 = B_1 \oplus B_5 \oplus B_9 \oplus B_{10} \oplus B_{11} \oplus B_{14} \oplus B_{18}$$

$$\oplus B_{19} \oplus B_{22} \oplus B_{23} \oplus B_{26} \oplus B_{27} \oplus B_{28}$$

$$\oplus B_{30} \oplus B_{31} \oplus BP_2 \text{ - - - - - - - - - - - - - - (5);}$$

$$S_3 = B_2 \oplus B_6 \oplus B_9 \oplus B_{12} \oplus B_{13} \oplus B_{15} \oplus B_{18}$$

$$\oplus B_{20} \oplus B_{21} \oplus B_{22} \oplus B_{24} \oplus B_{26} \oplus B_{27}$$

$$\oplus BP_3 \text{ - - - - - - - - - - - - - - - - - - (6):}$$

$$S_4 = B_3 \oplus B_7 \oplus B_{10} \oplus B_{12} \oplus B_{16} \oplus B_{19} \oplus B_{20}$$

$$\oplus B_{23} \oplus B_{25} \oplus B_{26} \oplus B_{29} \oplus B_{31} \oplus BP_4 \text{ - - - - (7);}$$

and

$$S_5 = B_4 \oplus B_8 \oplus B_{11} \oplus B_{13} \oplus B_{17} \oplus B_{21} \oplus B_{24}$$

$$\oplus B_{25} \oplus B_{27} \oplus B_{28} \oplus B_{29} \oplus B_{30} \oplus B_{31}$$

$$\oplus BP_5 \text{ - - - - - - - - - - - - - - - - - - (8).}$$

Incidentally, the symbols $\oplus$ appearing in the above logical equations indicate an exclusive OR operation.

The logical operation circuit FLG shown in Fig. 5 is constructed of logical circuits (not shown) for forming such syndromes S_0 to S_5 as satisfy the above equations (3) to (8). Incidentally, the sequence of the exclusive OR operations of the plural bits can be freely selected. In order to determine the exclusive OR values of the four bits B_0 to B_3, for example, therefore, the output $B_0 \oplus B_1$

is formed by the first exclusive OR circuit, and the output $B_2 \oplus B_3$ is formed by the second exclusive OR circuit so that these two outputs thus formed may be fed to the third exclusive OR circuit. As is apparent from the mutual comparisons of the equations (3) to (8), the exclusive OR values of the bits B_{14} to B_{17}, for example, appear commonly in the equations (3) and (4). The exclusive OR value of the bits B_{18} and B_{19} appears commonly in the equations (3) and (5). In order to reduce the number of the logical circuits constituting the logical operation circuit ELG, therefore, the exclusive OR value shared among the respective equations may be formed in advance by the common circuits, respectively.

The defects, which are established in advance in the memory MOSFET, switch MOSFET and signal line to be selected, and the substantial defects, which are caused during the operations of the circuit by the undesired changes in the circuit operating conditions, invite errors in the read out data which are to be fed to the ECC circuit.

Now, it is assumed that the memory cells to be written with the write data W as appearing in the Table 2 are selected and that the read out data R at that time make such errors as are tabulated

in the following Table 3. In other words, it is assumed that the seventh bit B_7 of the read out data R is changed from the value "0" to the value "1".

Table 3 (R)

B_0	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8	B_9	B_{10}	B_{11}	B_{12}	B_{13}	B_{14}	B_{15}	B_{16}
1	1	1	1	1	0	0	1	0	0	0	0	0	0	1	1	1

(Continued)

B_{17}	B_{18}	B_{19}	B_{20}	B_{21}	B_{22}	B_{23}	B_{24}	B_{25}	B_{26}	B_{27}	B_{28}	B_{29}	B_{30}	B_{31}
1	1	1	1	1	0	0	0	0	0	0	1	1	0	0

(Continued)

BP_0	BP_1	BP_2	BP_3	BP_4	BP_5
1	1	1	1	1	1

The logical operation circuit ELG in the ECC circuit logically calculates the syndromes S_0 to S_5 in accordance with the equations (3) to (8) when it is fed with those data (R). In the calculating procedures of determining those syndromes S_0 to S_5, the seventh bit B_7 is used in the logical operation to determine the syndromes S_1 and S_4, as is apparent from the Table 1. As a result that the seventh bit B_7 is charged from "0" to "1", the syndromes S_1 and S_4 respectively take the value "1". There is no error in the bits which are to be introduced into the calculating procedures of determining the

other syndromes S_0, S_2, S_3 and S_5. As a result, the syndromes S_0, S_2, S_3 and S_5 respectively take the value "0".

When the read out data R tabulated in the Table 3 are fed out, more specifically, the bit patterns of the syndromes S_5 to S_0 generated by the logical operation circuit ELG are expressed by "010010". This bit pattern becomes coincident with the bit pattern of the syndromes S_5 to S_0 indicating the seventh bit D_7 in the check matrix of the Table 1. In this check matrix, more specifically, the pattern of the syndromes S_5 to S_0 in the row of the bit D_7 is expressed by "010010", which is coincident with the bit pattern of the syndromes S_5 to S_0 generated from the logical operation circuit. Here, the blank columns in the check matrix are deemed to take the value "0".

As will be apparent from the Table 1, the respective signals of 38 bits are set with the plural check bits. The check bits set for one signal have a pattern which corresponds only to that signal.

In the event that the check matrix has the form tabulated in the Table 1, the bit pattern, which is constructed of the syndromes S_5 to S_0 fed from the logical operation

circuit ELG shown in Fig. 5, corresponds one-to-one to the positions of the error data bits of the read out data R.

The syndromes S_0 to S_5 generated by the logical operation circuit ELG are fed either directly or through inverters to the decoder DCR.

This decoder DCR is made operative to decode the syndromes S_0 to S_5 in order to generate the decoded signals indicative of the error units. The decoder DCR is constructed of AND gates G_0 to G_{31} which are made to correspond one-to-one to the data signals of 32 bits. The respective AND gates G_0 to G_{31} have their respective inputs so determined as to detect the different bit patterns. Each of the AND gates generates the "0" level, unless the data bits corresponding thereto are erroneous, and the "1" level if those bits are erroneous. For example, the AND gate G_0 generates the "1" level signal, if the first unit (or the first bit) signal of the data signals of 32 bits is erroneous, and otherwise the "0" level signal, as will be apparent from both the connections shown and the check matrix of the Table 1.

The respective outputs of the decoder DCR, i.e., the outputs of the AND gates G_0 to G_{31} and

the information bits B_0 to B_{31} of the read out data R are respectively fed to the exclusive OR circuits EOR_0 to EOR_{31}. These exclusive OR circuits EOR_0 to EOR_{31} form the error-corrected output data D_0 to D_{31} which are to be fed to the multiplexor MPX_0 shown in Fig. 1. If an error exists in the seventh data signal shown in the Table 3, for example, the output of the AND gate G_6 accordingly takes the value "1" so that the seventh signal read out erroneously as the above value "1" is inverted from the value "1" to the value "0" by the exclusive OR circuit EOR_7. In other words, the data signal D_6 is corrected to the right value.

The ECC circuit is enabled to correct the error of 1 bit but disabled to correct the error of 2 or more bits. In the case where the ECC circuit is provided in order to correct the error of 2 or more bits, the construction is complicated, and the number of the elements is increased. In this case, moreover, the parity bits have to be substantially increased.

Fig. 6 shows one specific embodiment of the inside of the logical operation circuit ELG and the exclusive OR circuit to be used for the error correction.

The exclusive OR circuit is constructed of

p-channel type MOSFETs Q_{p1} to Q_{p4} and n-channel MOSFETs Q_{n1} to Q_{n4}. The MOSFETs Q_{p1} and Q_{p2} and the MOSFETs Q_{n1} and Q_{n2} are respectively arranged in series, and the MOSFETs Q_{p3} and Q_{p4} and the MOSFETs Q_{n3} and Q_{n4} are likewise arranged in series. The junction between the MOSFETs Q_{p2} and Q_{n1} and the junction between the MOSFETs Q_{p4} and Q_{n3} are inter-connected in order to generate and output OUT. The MOSFETs Q_{n1} and Q_{n2} have their gates respectively fed with input signals $\underline{a}$ and $\underline{b}$, and the MOSFETs Q_{n3} and Q_{n4} have their gates respectively fed with input signals $\overline{a}$ and $\overline{b}$.

On the other hand, the MOSFETs Q_{p1} and Q_{p4} have their gates respectively fed with the input signals $\overline{a}$ and $\overline{b}$, and the MOSFETs Q_{p2} and Q_{p3} have their gates respectively fed with the input signals $\underline{b}$ and $\underline{a}$.

Now, when both the input signals $\underline{a}$ and $\underline{b}$ are at the high ("1") level, the MOSFETs Q_{n1} and Q_{n2} are rendered conductive to vary the output OUT to the low ("0") level. When both the input signals $\overline{a}$ and $\overline{b}$ are at the high level, the MOSFETs Q_{n3} and Q_{n4} are rendered non-conductive to likewise vary the output OUT to the low level.

Moreover, when the input signal $\underline{a}$ (or $\overline{a}$) is at the low level and the input signal $\overline{b}$ (or $\underline{b}$) is at the low level, the MOSFET Q_{p3} (or Q_{p1}) and the MOSFET Q_{p4} (or Q_{p2}) are rendered conductive in order to boost the output OUT to the high level. When

the input signals a and b have their levels thus made coincident, the output OUT is varied to the low level. In the case of inconsistency, the output OUT is raised to the high level.

The exclusive OR circuit shown has a small number of elements (e.g. 8) and allows no current to flow between the power source voltage V_{cc} and earth so that its power consumption is very low.

The logical operation circuit ELG of the ECC circuit performs such logical operations as are expressed by the foregoing logical equations (3) to (8) so as to form the syndromes S_0 to S_5, as has been described above. In other words, a number of the exclusive OR operations are performed in the logical operation circuit.

By using the exclusive OR circuit shown in Figure 6 as the logical circuit constituting the logical operation circuit ELG, it becomes possible to construct the logical operation circuit of a relatively small number of the elements and to reduce the power consumption to a relatively low level.

As has been described with reference to Figure 2, moreover, the data read out of the lefthand input and output terminals of the respective sense amplifiers always become a positive-phase output D_n' whereas the data read out of the righthand input and output terminals always become a negative-phase

output $\overline{D_n}'$ as a result that the inverted information is written in the righthand memory arrays M-ARY$_3$ and M-ARY$_4$. Accordingly, the data read out of the sense amplifiers can be fed as they are to the exclusive OR circuits in the logical operation circuit ELG so that this circuit ELG can be further simplified.

The respective information and parity signals constituting one set of the data are extracted from the respective memory groups each of which has 32 memory cells (i.e., the memory MOSFETs).

The 32 memory MOSFETs have their respective gates coupled to one word line and their drains and sources connected in series, as will be seen from Figure 2. The memory MOSFET are selected one by one from the respective memory cell groups in response to the decoded signals fed from the X decoder X-DCR$_1$ or X-DCR$_2$ and the decoded signals fed from the Y decoder R-DCR$_1$. In this case, the orders or positions of the respective memory cell groups of the memory MOSFETs to be selected are identical to each other. In other words, the plural signals constituting one set of data are read out of the memory MOSFETs which are located at every 32 ones and which are coupled to one word line.

In the large-capacity memory of the monolithic IC type, a defect is liable to occur simultaneously in the plural memory cells which are adjacent to each

other. This defect is caused by the incompleteness which is inevitable in the IC fabrication technique. The mask films, which are made of photoresist for selectively etching insulating and/or conducting films, for example, are not always produced to a satisfactory level because they are adversely affected by the irregularity in their material or by dust. If the defects such as undesirable roughnesses or pin holes exist in the pattern of the mask film worked, they are transferred to the insulating or conducting films to be worked by that mask film. If the mask film to be used for implanting impurity ions, these impurity ions may be introduced into the undesired portion of the surface of the semiconductor substrate or may not be introduced into the desired portion. The semiconductor substrate to be used intrinsically has such a defect, e.g. a crystal defect which will deteriorate the characteristics of the semiconductor elements to be formed thereon.

In a large-capacitance memory, the semiconductor elements and the wiring layers have fine sizes so as to ensure the high integration. As a result, a plurality of circuit elements are liable to be included in the area of one defect.

For the mask-type ROM shown in Figures 2A to 2C, it is possible to switch the column switches MOSFETs S_{a0} and S_{a1}, for example, in response to the

common decoded signal C_0 and to feed the outputs of the column switches MOSFETs S_{a0} and S_{a1} to the different sense amplifiers. In this case, the pieces of information of the memory MOSFETs M_0 and M_1, for example, can be simultaneously extracted by boosting the potentials of the word line W_0 and the decoded signals C_0 and C_{01} to the high level. In this case, however, the memory MOSFETs adjacent to each other are selected. Accordingly, the possibility that the pieces of information of 2 or more bits simultaneously extracted become erroneous. If these two bits are to be corrected in the ECC circuit, as has been described above, many parity bits are required. Incidentally, in the case where the ECC circuit having a 2-bit correcting ability, the number of the parity bits is significantly increased to twice the number. Therefore, this is not practical because the substantial data storage capacitance is substantially reduced.

According to the present invention, one group of data to be fed to the ECC circuit is constructed of the signals which are read out of the plural memory cells formed in scattered positions on the semiconductor chip.

The specific circuits shown in Figures 2A to 2C will now be described in greater detail. The adjacent memory cells (i.e. the memory MOSFETs),

e.g. the MOSFETs M_0 and M_1 are not simultaneously selected. In the event that the respective column switches MOSFETs are switched in response to the different decoded signals, it not being possible to extract anything but the information of 1 bit. In the event that such groups are formed, it is possible to simultaneously extract the information of plural bits. Since the groups are made to have similar constructions, there are always formed between two memory MOSFETs to be selected such a number of the memory MOSFETs as can constitute one side of one group. As a result, the distance between the memory MOSFETs to be selected has a relatively large value. In other words, the plural bits constituting the data fed to the ECC circuit are extracted from the memory MOSFETs which are formed in scattered positions on the chip. The plural defective cells formed in a concentrated manner are scattered into plural groups of data. As a result, the error bits included in one group of data can be reduced to about 1 bit at the most. Thus, even the ECC circuit having a low error correcting ability (e.g. 1 bit correcting ability) can correct the error bit. As a result, the fabrication yield of the semiconductor memory can be significantly improved.

In the semiconductor memory shown in Figures 2A to 2C, a desired number of the memory

MOSFETs are selected from the plural memory MOSFETs (i.e. the memory cells) coupled to one word line so that a necessary number of bits can be fed to the ECC circuit by the single addressing operation. Thus, the information can be read out at a relatively high speed.

In view of the fact that the ECC circuit has a low correcting ability as in the above it can be used to simplify the circuit construction and so reduce the number of the parity bits. As a result, it is possible to enlarge the data storage capacity.

In a modified form, in the circuit shown in Figures 2A to 2C, the MOSFETs Q_{d1} and Q_{d2} may be replaced by a single MOSFET which has a conductance equal to the combined conductances of the two MOSFETs which it replaces. In the case where it is possible to increase the power consumption the MOSFET Q_s may be omitted. Alternatively, the MOSFET Q_s can be omitted by applying a signal such as the address signal a_9 to one of the MOSFETs Q_{d1} and Q_{d2} and a signal such as the decoded signal C_0 to the other. In this modifcation, there is no increase in the power consumption. Furthermore, the information to be written in the memory array M-ARY_3 and M-ARY_4 need not be inverted. In this modification, however, it is necessary to modify the ECC circuit. It will be appreciated that the ECC circuit cannot be one

shown in Figure 5.

The present invention can be applied not only to a vertical type mask ROM and a programmable ROM (e.g. EPROM or EAROM) in addition to the above referred to horizontal mask ROM but also a ramdom access memory (i.e. RAM). Moreover, the arrangement of the memory cells to be stored with plural bits (including parity bits) constituting one set of data may be made such that the memory cells are spaced alternately by at least one of them.

Attention is drawn to our APplication No. 83.01289 (Serial No. 2,116,389) from which this Application has been divided.

CLAIMS.

1. A semiconductor memory including:

(a) a plurality of memory cells arranged in a matrix form in one semiconductor chip for storing one set of data having check bits;

(b) a selecting circuit for selecting those of said plural memory cells, which are grouped into one set, in response to the address signals; and

(c) an error correcting code circuit formed in said semiconductor chip and adapted to be fed with one set of data which are read out of the memory cells selected,

wherein each set of the data is stored in the plural memory cells which are spaced from each other farther than one of said memory cells.

2. A semiconductor memory according to claim 1, wherein each of said memory cells in made of a read only memory cell.

3. A semiconductor memory according to claim 1 or 2, further including a transfer circuit for sequentially transferring the error-corrected data which are fed from said error correcting code circuit.