INTEGRATED FIN-BASED FIELD EFFECT TRANSISTOR (FINFET) AND METHOD OF FABRICATION OF SAME

FIELD OF THE DISCLOSURE

[0001] The present disclosure relates to multiple gate field effect transistors (FETs), such as metal oxide semiconductor field effect transistors (MOSFETs), and in particular, to Fin-based field effect transistors, also known as FinFETs.

BACKGROUND OF THE DISCLOSURE

[0002] Perhaps the single most important device in modern electronic systems is the MOSFET. Such devices are used not only as transistors but also as passive devices, such as resistances and capacitances. The ability to scale such devices down to ever smaller dimensions has allowed electronic systems to become smaller to the point of enabling many hand-held and pocket-size systems. However, at the current pace of device scaling, it is predicted that planar transistors will soon reach their limits, in terms of minimize size. Further, as these devices get smaller, they increasingly suffer from undesirable short channel effects, such as off-state leakage current, which increases power consumption by the device.

[0003] As a result, multiple-gate MOSFETs have become of increased interest, based on their use of multiple gates on multiple surfaces, thereby more effectively suppressing off-state leakage currents. Further, these multiple gates allow enhanced current in the on-state, i.e., the drive current. Such advantages result in lower power consumption and enhanced device performance. Moreover, such non-planar devices are smaller than conventional planar transistors, thereby enabling even higher circuit densities and, therefore, smaller system sizes.

[0004] One particular multiple-gate MOSFET that has been developed is a FinFET, in which the conducting channel is disposed around a thin silicon "Fin", which serves as the body of the device. The dimensions of the Fin establish the effective channel length for the transistor.

[0005] Conventional FinFETs are fabricated using silicon over insulator (SOI) techniques. However, such devices often have poor thermal properties, e.g., poor heat dissipation, as well as relatively significant external resistances. Accordingly, an improved FinFET would be desirable.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] Figure 1 is a plan view of an integrated FinFET in accordance with an exemplary embodiment.

[0007] Figures 2-5 are cross-sectional views of the FinFET of Figure 1 along lines 2a-2d, respectively.

[0008] Figures 6-8 are cross-sectional views during fabrication of the shallow trench isolation (STI) of the device of Figure 1.

[0009] Figures 9-12 are cross-sectional views of the fabrication of the shallow trench isolation using TEOS oxide.

[0010] Figure 13 is a cross-sectional view illustrating the implantation of the N-well and P-well.

[0011] Figures 14-15 are cross-sectional views of the EPI growth.

[0012] Figures 16-17 are cross-sectional views of the EPI hard mask deposition.

[0013] Figures 18-19 are cross-sectional views of the fabrication of the EPI Fin mandrels.

[0014] Figures 20 and 21 are cross-sectional views of the fabrication of the mandrel spacers.

[0015] Figures 22-23 are cross-sectional views of the etching of the spacers.

[0016] Figures 24-25 are cross-sectional views of the removal of the mandrels.

[0017] Figures 26-27 are cross-sectional views of the Fin hard mask etching.

[0018] Figures 28-29 are cross-sectional views of the removal of the spacers.

[0019] Figures 30-31 are cross-sectional views of the Fin etching.

[0020] Figures 32-33 are cross-sectional views of the isolation of undesired Fins for removal.

[0021] Figures 34-35 are cross-sectional views of the removal of the undesired Fins.

[0022] Figures 36-37 are cross-sectional views of the removal of the resist used for isolating undesired Fins.

[0023] Figures 38-39 are cross-sectional views of the high K gate material deposition.

[0024] Figures 40-41 are cross-sectional views of the metal gate deposition.

[0025] Figures 42-43 are cross-sectional views of the metal gate hard mask.

[0026] Figures 44-45 are cross-sectional views of the deposition of metal gate resist.

[0027] Figures 46-47 are cross-sectional views of the hard mask etch.

[0028] Figure 48 is a cross-sectional view of the resist removal.

[0029] Figures 49-51 are cross-sectional views of the metal gate and high K gate etching.

[0030] Figures 52-53 are cross-sectional views of the spacer deposition and etching.

[0031] Figures 54-55 are cross-sectional views of the P-source/drain and N-source/drain implants.

[0032] Figures 56-57 are cross-sectional views of the P-EPI and N-EPI merges.

[0033] Figures 58-59 are cross-sectional views of the TEOS oxide deposition.

[0034] Figure 60 is a cross-sectional view of the fabrication of the local interconnect.

[0035] Figure 61 is a plan view of a FinFET in accordance with an alternative exemplary embodiment.

[0036] Figures 62-65 are cross-sectional views of the device of Figure 61 along lines 131a-131d, respectively.

[0037] Figure 66 is a plan view of a conventional FinFET.

[0038] Figures 67-70 are cross-sectional views of the device of Figure 66 along lines 233a-233d, respectively.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0039] The following detailed description is of example embodiments of the presently claimed invention with references to the accompanying drawings. Such description is intended to be illustrative and not limiting with respect to the scope of the present invention. Such embodiments are described in sufficient detail to enable one of ordinary skill in the art to practice the subject invention, and it will be understood that other embodiments may be practiced with some variations without departing from the spirit or scope of the subject invention.

[0040] An integrated fin-based field effect transistor (FinFET) and method of fabricating such devices on a bulk wafer with EPI-defined fin heights over shallow trench isolation (STI) regions are provided. The FinFET channels overlie the STI regions within the semiconductor bulk, while the fins extend beyond the STI regions into the source and drain regions which are implanted within the semiconductor bulk. With bulk source and drain regions, reduced external FinFET resistance is provided, and with the fins extending into the bulk source and drain regions, improved thermal properties is provided over conventional silicon on insulator (SOI) devices.

[0041] Advantageously, such a device minimizes external resistances by allowing the source and drain regions to be located in the bulk and closer to the channel. Further advantageously, an undoped channel epitaxial (EPI) based Fin is disposed over shallow trench isolation (STI), such that the EPI layer allows for better control of the Fin heights, with less variability, and more consistent Fins, e.g., no undercutting. Further advantageously, such a device allows for performance enhancement from the introduction of additional strain in the STI layer, as well as from the bulk source and drain regions. Further advantageously, heat

dissipation is increased with the Fins connected to the source and drain regions with the bulk substrate.

[0042] In accordance with an exemplary embodiment, the FinFET channel will be completely over STI while the Fins extend beyond the STI into the bulk source and drain regions. The source and drain regions can be formed using conventional source and drain implants and wells below. Extension of the Fins into the bulk source and drain regions allow for improved thermal properties similar to those using conventional bulk techniques, as opposed to SOI. With the FinFET channel over the STI, the Fin height in the channel region is determined by the deposited EPI layer over the STI. The bulk source and drain regions help reduce external resistances. The device architecture includes flexibility with respect to strain enhancement techniques in the STI layer below the channel and gate and also from the bulk source and drain regions.

[0043] Referring to Figures 1 and 2-5, a FinFET 1 in accordance with an exemplary embodiment includes a bulk source and drain and EPI merge area 3, shallow trench isolation 4, gate electrodes 5, epitaxial Fins 6, EPI merges 7, P-type source and drain regions 8, spacers 9, local interconnects 10, P-type bulk substrate 11, P-well 12, N-well 13, high K film 14, N-source and drain regions 15, silicide 16, gate hard mask 17 and TEOS regions 18, substantially as shown. As discussed in more detail below, the shallow trench isolation (STI) regions are disposed within the bulk, with the source and drain regions disposed between neighboring STI regions. The Fins are disposed substantially normal to the STI regions, with parts of which disposed over STI regions and other parts of which disposed within the source and drain regions. Each of the gate electrodes is disposed over portions of each of the Fins and laterally away from the source and drain regions, i.e., not above the source and drain regions.

[0044] The processing steps as discussed below are conventional in nature and, therefore, well known to one of ordinary skill in the art. The order in which the processing steps are discussed is not intended to necessarily be the only order in which such processing steps may be practiced, but rather are shown by way of example.

[0045] Referring to Figures 6-8, as seen along lines 2c and 2d (Figure 1), a photo resist 21 is deposited over the bulk 11 and etched away to produce the STI trenches 22, 23.

[0046] Referring to Figures 9-12, as seen alternately along lines 2c and 2d, respectively, TEOS oxide 24 is deposited and then removed by chemical-mechanical polishing (CMP), thereby filling in the STI trenches.

[0047] Referring to Figure 13, the P-well 12 and N-13 are implanted.

[0048] Referring to Figures 14 and 15, as seen along lines 2c and 2d, respectively, an EPI layer 25 is grown and planarized, and merged, e.g., in the sequence depicted at the right side of the figures. As will be readily appreciated by one of ordinary skill in the art, growing an EPI layer at is but one example of this stage of the fabrication process. Other types of semiconductor materials commonly used in the fabrication of circuits can also be used, including other silicon-based films laterally overgrown as depicted here, as well as gallium arsenide (GaAs), diamond-based or carbon nanotube films (e.g., using deposition).

[0049] Referring to Figures 16-17, as seen along lines 2c and 2d, respectively, a hard mask 26 is deposited over the EPI layer 25.

[0050] Referring to Figures 18-19, as seen along lines 2c-2d, respectively, Fin mandrel resist 27 is deposited over the EPI layer 26.

[0051] Referring to Figures 20-21, as seen along lines 2c-2d, respectively, material 28 to form the mandrel spacers is deposited.

[0052] Referring to Figures 22-23, as seen along lines 2c-2d, respectively, etching leaves what will ultimately serve as spacers 28a.

[0053] Referring to Figures 24-25, as seen along lines 2c-2d, respectively, the mandrels 27 are removed.

[0054] Referring to Figures 26-27, as seen along lines 2c-2d, respectively, the hard mask 26 is etched, thereby leaving hard mask regions 26a below the spacers 28a.

[0055] Referring to Figures 28-29, as seen along lines 2c-2d, respectively, the spacers 28a are removed.

[0056] Referring to Figures 30-31, as seen along lines 2c-2d, respectively, the Fins are formed by etching the EPI layer 25, thereby leaving portions 25a of the EPI layer beneath the hard mask portions 26a.

[0057] Referring to Figures 32-33, as seen along lines 2c-2d, respectively, masking material 29 is applied to protect the desired Fins while exposing the undesired Fins for removal.

[0058] Referring to Figures 34-35, as seen along lines 2c-2d, respectively, the undesired Fins are removed.

[0059] Referring to Figures 36-37, as seen along lines 2c-2d, respectively, the masking material 29 is removed, thereby exposing the desired Fins.

[0060] Referring to Figures 38-39, as seen along lines 2c-2d, respectively, high K gate material 31 is deposited.

[0061] Referring to Figures 40-41, as seen along lines 2c-2d, respectively, metalization 32 for the gate electrodes is deposited. As will be readily appreciated by one of ordinary skill in the art, the exemplary fabrication process as described thus far is a single gate metalization scheme. As will be further appreciated, more complex processes can be used in accordance with well known techniques, e.g., fabricating a more complex gate using one metal for P-channel devices and another metal for N-channel devices. Additionally, the gates can be fabricated with a gate first or replacement gate flow as is well known in the art.

[0062] Referring to Figures 42-43, as seen along lines 2c-2d, respectively, a hard mask 33 is deposited.

[0063] Referring to Figures 44-45, as seen along lines 2c-2d, respectively, masking material 34 is selectively applied over the metalization 33.

[0064] Referring to Figures 46-47, as seen along lines 2c-2d, respectively, the hard mask 33 is etched, thereby leaving only a selected portion 33a.

[0065] Referring to Figure 48, the masking material 34 is removed.

[0066] Referring to Figures 49-51, the gate metalization 32 and high K gate material 31 is etched, thereby leaving selected portions 32a, 31a.

[0067] Referring to Figures 52-53, as seen along line 2c, spacer material 35 is selectively deposited and then etched away, thereby leaving selected portions 35a.

[0068] Referring to Figures 54-55, as seen along line 2d, masking material 36 is deposited and etched, following which the P-type source and drain regions 37 and N-type source and drain regions 38 are implanted.

[0069] Referring to Figures 56-57, as seen along line 2d, P-EPI 39p and N-EPI 39n merges are applied.

[0070] Referring to Figures 58-59, as seen along lines 2c-2d, respectively, TEOS 41 is applied.

[0071] Referring to Figure 60, as seen along line 2d, the TEOS oxide 41 is etched to allow formation of the local interconnect 42, e.g., by tungsten deposition, following which chemical and mechanical planarization (CMP) can be used to provides a planar surface.

[0072] Referring to Figures 61-65, a FinFET 131 in accordance with an alternative embodiment includes bulk source and drain regions and EPI merge areas 133, shallow trench isolation 134, gate electrodes 135, epitaxial Fins 136, EPI merges 137, P-type source and drain regions 138, spacers 139, local interconnects 140, P-type bulk substrate 141, P-well

142, N-well 143, high K film 144, N-type source and drain regions 145, silicide 146, gate hard mask 147, TEOS oxide 148, ultra thin boxes 149 and epitaxial silicon Fins 150, substantially as shown. The larger volume of the epitaxial material 137 used for the Fins advantageously allows for use of increased strain within the device channels.

[0073] Referring to Figures 66-70 a conventional FinFET 232 includes source and drain regions and EPI merge areas 234, shallow trench isolation 235, gate electrodes 236, epitaxial Fins 237, EPI merges 238, spacers 239, P-type source and drain regions 240, local interconnects 241, TEOS oxide 242, high K film 243, gate hard mask 244, silicide 247 and N-type source and drain regions 248 disposed substantially as shown over a box 246, which, in turn, is disposed over the P-type bulk substrate 245. The spacers 239 protect the gates 236 during diffusion of the source and drain regions, and also prevent strain material from getting too close to the gate 236. Further, the lower volume of EPI merges 7 to surround the Fins minimize potential strain effects.

[0074] Also, integrated circuit design systems (e.g., work stations with digital processors) are known that create integrated circuits based on executable instructions stored on a computer readable medium including memory such as but not limited to CDROM, RAM, other forms of ROM, hard drives, distributed memory, or any other suitable computer readable medium. The instructions may be represented by any suitable language such as but not limited to hardware descriptor language (HDL) or other suitable language. The computer readable medium contains the executable instructions that when executed by the integrated circuit design system causes the integrated circuit design system to produce an integrated circuit that includes the devices or circuitry as set forth above. The code is executed by one or more processing devices in a work station or system (not shown). As such, the devices or circuits described herein may also be produced as integrated circuits by such integrated circuit systems executing such instructions.

[0075] Various other modifications and alternations in the structure and method of operation of this invention will be apparent to those skilled in the art without departing from the scope and the spirit of the invention. Although the invention has been described in connection with specific preferred embodiments, it should be understood that the invention as claimed should not be unduly limited to such specific embodiments. It is intended that the following claims define the scope of the present invention and that structures and methods within the scope of these claims and their equivalents be covered thereby.

WHAT IS CLAIMED IS:

1. An apparatus including an integrated fin-based field effect transistor (FinFET), comprising:

a bulk region;

a plurality of substantially parallel shallow trench isolation (STI) regions disposed within first portions of said bulk region;

a plurality of source and drain regions each of which is disposed between neighboring ones of said plurality of STI regions within second portions of said bulk region;

a plurality of fin regions disposed substantially normal to said plurality of STI regions and each of which includes

first portions disposed over a portion of said plurality of STI regions, and

second portions disposed within a portion of said plurality of source and drain regions; and

a plurality of gate regions each of which is disposed over a respective portion of said plurality of fin regions and a respective one of said plurality of STI regions and laterally away from neighboring ones of said plurality of source and drain regions.

2. The apparatus of claim 1, wherein said plurality of fin regions comprises a plurality of portions of an epitaxial film.

3. The apparatus of claim 1, wherein said plurality of fin regions comprises a plurality of portions of a silicon-based film.

4. The apparatus of claim 1, wherein said plurality of fin regions comprises a plurality of portions of a gallium arsenide film.

5. The apparatus of claim 1, wherein said plurality of fin regions comprises a plurality of portions of a diamond-based film.

6. The apparatus of claim 1, wherein said plurality of fin regions comprises a plurality of portions of a carbon nanotube film.

7. A method of fabricating an integrated fin-based field effect transistor (FinFET), comprising:

etching and filling a plurality of shallow trench isolation (STI) regions within first portions of a bulk region;

implanting a plurality of source and drain regions within second portions of said bulk region, wherein each of said plurality of source and drain regions is disposed between neighboring ones of said plurality of STI regions;

forming a plurality of fin regions substantially normal to said plurality of STI regions, wherein each of said plurality of fin regions includes

first portions disposed over a portion of said plurality of STI regions, and

second portions disposed within a portion of said plurality of source and drain regions; and

depositing each of a plurality of gate regions over a respective portion of said plurality of fin regions and a respective one of said plurality of STI regions and laterally away from neighboring ones of said plurality of source and drain regions.

8. The method of claim 7, wherein said forming a plurality of fin regions comprises depositing and growing an epitaxial film.

9. The method of claim 7, wherein said forming a plurality of fin regions comprises depositing and growing a silicon-based film.

10. The method of claim 7, wherein said forming a plurality of fin regions comprises depositing a gallium arsenide film.

11. The method of claim 7, wherein said forming a plurality of fin regions comprises depositing a diamond-based film.

12. The method of claim 7, wherein said forming a plurality of fin regions comprises depositing a carbon nanotube film.

13. A computer readable medium comprising a plurality of executable instructions that, when executed by an integrated circuit design system, cause the integrated circuit design system to produce:

an integrated fin-based field effect transistor (FinFET), comprising:

a bulk region;

a plurality of substantially parallel shallow trench isolation (STI) regions disposed within first portions of said bulk region;

a plurality of source and drain regions each of which is disposed between neighboring ones of said plurality of STI regions within second portions of said bulk region;

a plurality of fin regions disposed substantially normal to said plurality of STI regions and each of which includes

first portions disposed over a portion of said plurality of STI regions, and

second portions disposed within a portion of said plurality of source and drain regions; and

a plurality of gate regions each of which is disposed over a respective portion of said plurality of fin regions and a respective one of said plurality of STI regions and laterally away from neighboring ones of said plurality of source and drain regions.

14. The apparatus of claim 13, wherein said plurality of fin regions comprises a plurality of portions of an epitaxial film.

15. The apparatus of claim 13, wherein said plurality of fin regions comprises a plurality of portions of a silicon-based film.

16. The apparatus of claim 13, wherein said plurality of fin regions comprises a plurality of portions of a gallium arsenide film.

17. The apparatus of claim 13, wherein said plurality of fin regions comprises a plurality of portions of a diamond-based film.

18. The apparatus of claim 13, wherein said plurality of fin regions comprises a plurality of portions of a carbon nanotube film.