STACKABLE SEMICONDUCTOR PACKAGE AND METHOD FOR MANUFACTURING SAME

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

The present invention relates to semiconductor packages, leadframe assemblies therefor and a method of manufacture, and more particularly, but not by way of limitation, to a stackable semiconductor package and a method for manufacturing the same.

HISTORY OF RELATED ART

It is conventional in the electronic industry to encapsulate one or more semiconductor devices, such as integrated circuit dies, or chips, in a semiconductor package. These plastic packages protect a chip from environmental hazards, and provide a method of and apparatus for electrically and mechanically attaching the chip to an intended device. Recently, such semiconductor packages have included metal lead frames for supporting an integrated circuit chip which is bonded to a chip paddle region formed centrally therein. Bond wires which electrically connect pads on the integrated circuit chip to individual leads of the lead frame are then incorporated. A hard plastic encapsulating material, or encapsulant, which covers the bond wire, the integrated circuit chip and other components, forms the exterior of the package. A primary focus in this design is to provide the chip with adequate protection from the external environment in a reliable and effective manner.

As set forth above, the semiconductor package therein described incorporates a lead frame as the central supporting structure of such a package. A portion of the lead frame completely surrounded by the plastic encapsulant is internal to the package. Portions of the lead frame extend internally from the package and are then used to connect the package externally. More information relative to lead frame technology may be found in Chapter 8 of the book Micro Electronics Packaging Handbook, (1989), edited by R. Tummala and E. Rymaszewski, incorporated by reference herein. This book is published by Van Nostrand Reinhold, 115 Fifth Avenue, New York, New York.

Once the integrated circuit chips have been produced and encapsulated in semiconductor packages described above, they may be used in a wide variety of electronic appliances. The variety of electronic devices utilizing semiconductor packages has grown dramatically in recent years. These devices include cellular phones, portable computers, etc. Each of these devices typically include a printed circuit board on which a significant number of such semiconductor packages are secured to provide multiple electronic functions. These electronic appliances are typically manufactured in reduced sizes and at reduced costs, which results in increased consumer demand. Accordingly, not only are semiconductor chips highly integrated, but also semiconductor packages are highly miniaturized with an increased level of package mounting density.

According to such miniaturization tendencies, semiconductor packages, which transmit electrical signals from semiconductor chips to printed circuit boards and support the semiconductor chips on the printed circuit boards, have been designed to have a small size. By way of example only, such semiconductor packages may have a size on the order of 1x1mm to 10x10 mm. Examples of such semiconductor packages are referred to as MLF (micro leadframe) type semiconductor packages and MLP (micro leadframe

package) type semiconductor packages. Both MLF type semiconductor packages and MLP type semiconductor packages are generally manufactured in the same manner.

Even though semiconductor packages have been miniaturized, space on a printed circuit board remain limited and precious. Thus, there is a need to find both a method and a carrier package design to maximize the number of semiconductor packages that can be fitted onto an electronic device, yet minimize the space needed to attach these semiconductor packages. One method to minimize space needed to attach the semiconductor packages is to stack the semiconductor packages on top of each other.

SUMMARY OF THE INVENTION

The present invention relates to stackable semiconductor packages and methods for manufacturing the same. More particularly, one aspect of the present invention comprises a semiconductor package wherein the semiconductor package includes a lead frame, a semiconductor chip, a plurality of electrical paths electrically connecting the semiconductor chip to the leadframe, and a sealing material. The leadframe has a plurality of leads, each one of the plurality of leads having a top portion exposed to a top surface of the semiconductor package and a bottom portion resting flush with a bottom surface of the semiconductor package. In this manner, the leads extending from the top to the bottom surface of the semiconductor package provide an electrical path for connecting and electrically powering a second semiconductor package stacked on top of a first semiconductor package.

In another aspect, the present invention relates to a method for stacking semiconductor packages. More particularly, the method comprises the steps of physically and electrically connecting a bottom side of a first semiconductor package to a printed

circuit board, the first semiconductor package having a plurality of leads, each one of the first plurality of leads having a first section exposed to a first top surface of the first semiconductor package and a second section resting flush against a first bottom surface of the first semiconductor package. A second semiconductor package is then physically and electrically connected to the top of the first semiconductor package. The second semiconductor package includes a second plurality of leads in generally the same position as the first plurality of leads.

BRIEF DESCRIPTION OF THE DRAWINGS

A more complete understanding of the carrier package according to the present invention may be obtained by reference to the following detailed description when taken in conjunction with the accompanying drawings wherein:

FIGURE 1 is a side-elevational, cross-sectional view of a prior art semiconductor package;

FIGURE 2 is a side-elevational, cross-sectional view of a first embodiment of a semiconductor package constructed in accordance with the principles of the present invention;

FIGURE 3 is a side-elevational, cross-sectional view of a method for stacking the first embodiment of a semiconductor package constructed in accordance with the principles of the present invention;

FIGURE 4 is a side-elevational, cross-sectional view of a second embodiment of a semiconductor package constructed in accordance with the principles of the present invention;

FIGURE 5 is a side-elevational, cross-sectional view of the second embodiment of a semiconductor package constructed in accordance with the principles of the present invention after the semiconductor package has been prepared for stacking;

FIGURE 6 is a side-elevational, cross-sectional view of a method for stacking the second embodiment of a semiconductor package constructed in accordance with the principles of the present invention;

FIGURE 7 is a side-elevational, cross-sectional view of a third embodiment of a semiconductor package constructed in accordance with the principles of the present invention;

FIGURE 8 is a side-elevational, cross-sectional view of the third embodiment of a semiconductor package constructed in accordance with the principles of the present invention after the semiconductor package has been prepared for stacking;

FIGURE 9 is a side-elevational, cross-sectional view of a method for stacking the third embodiment of a semiconductor package constructed in accordance with the principles of the present invention;

FIGURE 10 is a side-elevational, cross-sectional view of a fourth embodiment of a semiconductor package constructed in accordance with the principles of the present invention;

FIGURE 11 is a side-elevational, cross-sectional view of the fourth embodiment of a semiconductor package constructed in accordance with the principles of the present invention after the semiconductor package has been prepared for stacking;

FIGURE 12 is a side-elevational, cross-sectional view of a method for stacking the fourth embodiment of a semiconductor package constructed in accordance with the principles of the present invention;

FIGURE 13 is a side-elevational, cross-sectional view of a fifth embodiment of a semiconductor package constructed in accordance with the principles of the present invention;

FIGURE 14 is a side-elevational, cross-sectional view of the fifth embodiment of a semiconductor package constructed in accordance with the principles of the present invention after the semiconductor package has been prepared for stacking;

FIGURE 15 is a side-elevational, cross-sectional view of a method for stacking the fifth embodiment of a semiconductor package constructed in accordance with the principles of the present invention;

FIGURE 16 is a side-elevational, cross-sectional of a sixth embodiment of a semiconductor package constructed in accordance with the principles of the present invention;

FIGURE 17 is a side-elevational, cross-sectional view of a method for stacking the sixth embodiment of a semiconductor package constructed in accordance with the principles of the present invention;

FIGURE 18 is a side-elevational, cross-sectional of a seventh embodiment of a semiconductor package constructed in accordance with the principles of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

The present invention may be understood more readily by reference to the following detailed description of preferred embodiments of the invention and the figures.

Referring now to FIGURE 1, there is shown a side-elevational, cross-sectional view of prior art semiconductor package 50. Semiconductor package 50 has a semiconductor chip 51 attached to a paddle 52. Paddle 52 is a part of leadframe 50a. A plurality of leads 53, also a part of leadframe 50a, surround but do not touch paddle 52. A plurality of wires 54 electrically connect semiconductor chip 51 to leads 53. The wires 54 are generally thin and made of gold, silver, or aluminum. The entire assembly–except for outer portions of leads 53–is enclosed by a nonconducting sealing material 55. Sealing material 55 may be, thermoplastics or thermoset resins, with the thermoset resins including silicones, phenolics, and epoxies. Prior art semiconductor package 50 cannot be stacked on top of each other because no electrical path exists to electrically link the semiconductor on the top to a printed circuit board.

Referring now to FIGURE 2, there is shown a side-elevational, cross-sectional view of semiconductor chip package 60, a first embodiment of a semiconductor package

constructed in accordance with the principles of the present invention. Semiconductor package 60 has a semiconductor chip 61, a leadframe 69, and a plurality of wires 64. The above components are encased in a nonconductive sealing material 65, which may be thermoplastics or thermoset resins, with the thermoset resins including silicones, phenolics, and epoxies.

Still referring to FIGURE 2, leadframe 69 will now be described in more detail. Leadframe 69 has paddle 62 and a plurality of leads 63 all held in a spacial relationship by a tie bar (now shown) that surrounds leadframe 69. Leadframe 69 is made of a heat and electrically conductive material such as, for example, copper. Paddle 62 is of a generally flat rectangle shape, in some embodiments square, having a certain thickness. Paddle 62 may, but does not necessarily have to be, etched for better locking strength to sealing material 65. A bottom side of paddle 62 rests flush with and is exposed to the outside of semiconductor package 60. Exposing the bottom side of paddle 62 to the outside environment increases the heat dissipation capabilities of semiconductor package 60. The exposed portion of paddle 62 may be coated or electroplated with a corrosion-minimizing material such as, for example, tin, gold, tin lead, nickel palladium, tin bismuth, or an alloy thereof. A plurality of leads 63 surround, but do not touch, paddle 62. Each one of leads 63 has a top side 66, a bottom side 67, and an inwardly extending member 68. Top side 66 of each one of leads 63 rests flush with the upper surface of semiconductor package 60, while bottom side 67 of each one of leads 63 rests flush with the lower surface of semiconductor package 60. Electrical power passes through semiconductor package 60 by traveling from top side 66 to bottom side 67 or vice versa. The exposed portions of top side 66 and bottom side 67 may be coated or electroplated with a corrosion-minimizing material such as, for example, tin, gold, tin lead, nickel palladium, tin bismuth, or an alloy thereof. A notch 68a is created by inwardly extending member 68a. Notch 68 increases the locking strength between each lead of leads 63 and

semiconductor package 60 and decreases the likelihood of a lead of leads 63 from becoming detached form semiconductor package 60. Semiconductor chip 61 is attached to the top side of paddle 62 by using an adhesive known in the art.

Still referring to FIGURE 2, a plurality of wires 64 electrically connect semiconductor chip 61 to leadframe 69. Wires 64 are generally thin in dimension and are made of an electrically conductive material such as gold, silver, or aluminum. Heat generated from the operation of semiconductor chip 62 can travel through wires 64 and be dissipated to the outside environment via leads 63. Each wire of wires 64 is attached to a bond pad (not shown) on semiconductor chip 62 at one end and is attached at a second end to the inwardly extending member 68 of one of the leads 63.

Still referring to FIGURE 2, sealing material 65 encapsulates leadframe 69, semiconductor chip 61, and wires 64 except for top side 66, bottom side 67, and the bottom of paddle 62. Top side 66, bottom side 67, and the bottom of paddle 62 rest flush with the surface of carrier package 60.

Referring now to FIGURE 3, there is shown semiconductor packages 70 and 71, both embodiments of semiconductor packages constructed in accordance with the principles of the present invention. Semiconductor package 70 is attached to the top of semiconductor package 71 so that leads 73 of semiconductor package 71 touch and electrically connect with leads 75 of semiconductor package 70. The bottom surface of semiconductor package 71 may be attached to a printed circuit board (not shown) of an electronic device or may be attached to another semiconductor package having leads in generally the same locations. Yet another semiconductor package having leads located generally at the same place as semiconductor package 70 may be attached to the top surface of semiconductor package 70. To physically and electrically attach semiconductor

packages 70 and 71 to each other, to another semiconductor package, or to a printed circuit board, any method commonly used in the art can be used, including, but not limited to, soldering one object to the other.

Referring now to FIGURE 4, there is shown semiconductor package 80, a second embodiment of a semiconductor package constructed in accordance with the principles of the present invention. Semiconductor package 80 has semiconductor chip 81, a leadframe 80a, and a plurality of wires 84. These components are set into place using sealing material 85, which includes thermoplastics or thermoset resins, with the thermoset resins including silicones, phenolics, and epoxies.

Still referring to FIGURE 4, except for the shape of the leads 83, semiconductor package 80 is constructed in generally the same manner and has generally the same components as semiconductor package 60. Each one of the leads 83 has a bottom side 86 and a top side 87. The bottom surface of bottom side 86 rests flush with the bottom side of semiconductor package 80 and is exposed to the outside environment. Top side 87 has an inwardly extending member 88 and an outwardly extending member 89. Inwardly extending member 88 is used for attaching to the plurality of wires 84. Outwardly extending member 89 is used to electrically connect integrated circuit chip 81 to a printed circuit board (not shown) just like prior art semiconductor package 50 or, as described below, is used to stack semiconductor packages onto each other. A notch 88a formed by inwardly extending member 88 increases the locking strength between leads 83 and semiconductor package 80 so as to decrease the likelihood of a lead of leads 83 from becoming detached from semiconductor package 80. To minimize corrosion, the bottom exposed surface of bottom side 86 and the outwardly extending member 88 may be coated or electroplated with a protective material, such as, for example, tin, gold, tin lead, nickel palladium, tin bismuth, or any alloy thereof.

Referring now to FIGURE 5, there is shown a side-elevational, cross-sectional view of semiconductor package 80 after it has been prepared for stacking. To prepare carrier package 80 for stacking, outwardly extending member 89 is bent upwards and then inwards to partially wrap around the upper surface of semiconductor package 80. In this bent configuration, semiconductor package 80 now has leads 83 that extend from the bottom surface to the top surface of semiconductor package 80, thus providing an electrical path for electrical power to pass through semiconductor package 80 and electrically connecting with another semiconductor package located on top of semiconductor package 80.

Referring now to FIGURE 6, there is shown a side-elevational, cross-sectional view of a method for stacking semiconductor package 91 onto semiconductor package 90. Both semiconductor packages 90 and 91 are of the second embodiment of the semiconductor package constructed in accordance with the principles of the present invention. When stacked onto each other, the top side 92 of semiconductor package 90 comes into physical and electrical contact with the bottom side 93 of semiconductor package 91. In addition, a space 96 is left between semiconductor packages 90 and 91 to allow heat dissipation from the bottom surface of paddle 97 of semiconductor package 91. Bottom side 94 of semiconductor package 90 can be attached to a printed circuit board or another semiconductor package having leads generally located at the same place as semiconductor package 90. Another semiconductor package (not shown) can also be stacked on top of semiconductor package 91 by following the same method as described above. The semiconductor packages are held in this stacked position by applying solder–or any other material commonly used in the art–between the semiconductor packages and/or between a semiconductor package and a printed circuit board.

Referring now to FIGURE 7, there is shown a side-elevational, cross-sectional view of semiconductor package 106, a third embodiment of a semiconductor package constructed in accordance with the principles of the present invention. The location of leads 100 in semiconductor package 106 differs from the location of leads in the embodiments previously described. Each one of the leads 100 has a top side 101 and a bottom side 102. The bottom side 102 is completely encased in sealing material 103 except for the bottom-most surface that is resting flush with the bottom surface of semiconductor package 106. The bottom-most surface of bottom side 102 is exposed to the outside to allow electrical contact with a printed circuit board or with another carrier package (not shown) having leads located at generally the same place as semiconductor package 106. To minimize corrosion, the bottom-most surface of bottom side 102 is coated or electroplated with a protective material such as, for example, tin, gold, tin lead, nickel palladium, or an alloy thereof. Top side 101 has an inwardly extending member 114 and an outwardly extending member 115. Inwardly extending member 114 connects to integrated circuit chip 104 through wires 105. Inwardly extending member 114 also creates notch 114a. Notch 114a increases the locking strength between leads 100 and semiconductor package 106 and decreases the likelihood of leads 100 becoming detached from semiconductor package 106. A small portion of the outwardly extending member 115 is encased in sealing material 103 for increase in locking strength, but the majority portion of outwardly extending member 115 is exposed to the outside for connection to a printed circuit board just like prior art semiconductor package 50 or any other semiconductor package. The exposed portion of outwardly extending member 115 is coated or electroplated with a protective material, including, but not limited to, tin, gold, tin lead, nickel palladium, or an alloy thereof to minimize corrosion.

Referring now to FIGURE 8, there is shown a side-elevational, cross-sectional view of semiconductor package 106 with the exposed section of outwardly extending

member 115 bent upwards. An outside notch 107 is formed by this bending of outwardly extending member 115. Outwardly extending member 115 may rest flush with the top surface of carrier package 106 (FIGURE 8) or protrude slightly upwards as shown in carrier package 108 of FIGURE 9. In this bent configuration, semiconductor package 106 now has leads 100 that extend from the bottom surface to the top surface of semiconductor package 106, thus providing an electrical path through semiconductor package 106 and allows for electrically connecting with another semiconductor package located on top of semiconductor package 106.

Referring now to FIGURE 9, there is shown a cross sectional, side-elevational view of a method for stacking the third embodiment of semiconductor packages constructed in accordance with the principles of the present invention. Semiconductor package 109 is placed on top of semiconductor package 108. The portion of the outwardly extending member 116 protruding out of the top surface of semiconductor package 108 fits into notch 112 of semiconductor package 109. Top side 113 of semiconductor package 109 rests flush with the top surface of semiconductor package 109. Another semiconductor package of the present invention having leads generally in the same place as semiconductor package 109 may be stacked on top of semiconductor package 109. Another semiconductor package having generally the same configuration as semiconductor package 108 can be stacked underneath semiconductor package 108. Alternatively, a printed circuit board can be attached to the bottom surface semiconductor package 108. The semiconductor packages are held together in this stacked position by applying solder–or any other material commonly used in the art–between the semiconductor packages and/or between a semiconductor package and a printed circuit board.

Referring now to FIGURE 10, there is shown a side-elevational, cross-sectional view of semiconductor package 120, a fourth embodiment of a semiconductor package constructed in accordance with the principles of the present invention. Semiconductor package 120 has generally the same components as the embodiments of the present invention already discussed above, including leads 121 that can extend from the bottom surface of semiconductor package 120 to the top surface of semiconductor package 120. However, leads 121 are shaped differently. Each lead of leads 121 has a top side 122 and bottom side 123. Bottom side 123 is enclosed in sealing material 124 except for the very bottom surface, which is exposed to the outside for electrical contact. Top side 122 provides a surface for integrated circuit chip 125 to physically and electrically connect to leads 121 through a plurality of wires 126. Top side 122 also has an outwardly extending member 133. Though a portion of outwardly extending member 133 is enclosed in sealing material 124 for better locking strength between leads 122 and semiconductor package 120, a large part of outwardly extending member 133 is exposed to the outside of semiconductor package 120. If no other semiconductor package is stacked on top of semiconductor package 120, outwardly extending member 133 can be electrically connected to a printed circuit board just like prior art semiconductor package 50. Both the outwardly extending member 133 and the very bottom surface of bottom side 123 are coated or electroplated with a protective material such as, for example, tin, gold, tin lead, nickel palladium, tin bismuth, or any alloy thereof in order to minimize corrosion.

Referring now to FIGURE 11, there is shown a side-elevational, cross-sectional view of semiconductor package 120, with the outwardly extending member 133 of top side 122 bent upwards and then partially wrapped around the top surface of semiconductor package 120. Once the outwardly extending member 133 is wrapped around semiconductor package 120, semiconductor package 120 can be stacked onto another similar semiconductor package as shown in FIGURE 12. In this bent

configuration, semiconductor package 120 now has leads 121 that extend from the bottom surface to the top surface of semiconductor package 120, thus providing an electrical path through semiconductor package 120 and powering another semiconductor package located on top of semiconductor package 106.

Referring now to FIGURE 12, there is shown a side-elevational, cross-sectional semiconductor package 127 stacked onto semiconductor package 128. Leads 130 are physically and electrically connected to leads 132. A space 135 is left between semiconductor packages 127 and 128 to allow for heat dissipation from the bottom surface of paddle 134. Another semiconductor package having leads at generally the same place as semiconductor package 127 can be placed on top of semiconductor package 127. Semiconductor package 128 can also be placed on top of another semiconductor package or be physically and electrically connected to a printed circuit board. Again, the semiconductor packages are held in this stacked position by applying solder–or any other material commonly used in the art–between the semiconductor packages and/or between a semiconductor package and a printed circuit board.

Referring now to FIGURES 13-15, there is shown side-elevational, cross-sectional views of semiconductor package 140, a fifth embodiment of a semiconductor package constructed in accordance with the principles of the present invention. Semiconductor package 140 is similar in construction to semiconductor package 120 of the fourth embodiment. However, leads 141 of semiconductor package 140 are not completely enclosed by sealing material 142, but rather also have an exposed lateral side. Leads 141 also have an outwardly extending member 143 which, as seen in FIGURE 14, can be partially wrapped around the top surface of semiconductor package 140. A plurality of semiconductor packages having leads in generally the same place as semiconductor package 140 can be stacked and affixed onto each other as shown in

FIGURE 115, with the leads 141 providing the physical and electrical contact between the semiconductor packages and with the space 144 between the semiconductor packages allowing heat dissipation. Note if no other semiconductor package is stacked on top of semiconductor package 140, outwardly extending members 143 can be electrically connected to a printed circuit board just like prior art semiconductor package 50.

Referring now to FIGURE 16, there is shown a side-elevational, cross-sectional view of semiconductor package 150, a sixth embodiment of a semiconductor package constructed in accordance with the principles of the present invention. Except for a paddle, semiconductor package 150 has all the components of the previously disclosed embodiments of the semiconductor packages constructed in accordance with the principles of the present invention. Instead, the semiconductor chip 151 of semiconductor package 150 is supported on the bottom side by a plurality of leads 152. Each one of leads 152 has a top side 153, an inwardly extending member 154, and a bottom side 155. Semiconductor chip 150 is attached to the top of inwardly extending member 154. Semiconductor chip 151 is electrically connected to leads 152 through a plurality of wires 156. The bottom surface of bottom side 155 rests flush with the bottom surface of semiconductor package 150; the top surface of top side 153 rests flush with the top surface of semiconductor package 150. A lateral side of each lead of leads 152 is also exposed to be outside of semiconductor package 150. All the exposed parts of leads 152 are coated or electroplated with a corrosion-minimizing material such as, for example, tin, gold, tin lead, tin bismuth, nickel palladium, or an alloy thereof. Because leads 152 extend from the bottom surface of semiconductor package 150 to the top of semiconductor package 150, leads 152 provide an electrical path through semiconductor package 150 and can electrically connect to another semiconductor package located on top of semiconductor package 150.

Referring now to FIGURE 17, there is shown a side-elevational, cross-sectional view of the manner by which the sixth embodiment of semiconductor packages constructed in accordance with the principles of the present invention can be stacked onto each other. Semiconductor package 157 is stacked on top of semiconductor package 158, with leads 160 in semiconductor package 158 physically and electrically connect leads 162 of semiconductor package 157. Another semiconductor package having leads in generally the same place as semiconductor package 157 can be stacked and then affixed to the top of semiconductor package 157. Similarly, semiconductor package 158 can be physically affixed to and electrically connected with a printed circuit board or be stacked and affixed on top of another semiconductor package having leads in generally the same place. The semiconductor packages are held in this stacked position by applying solder–or any other material commonly used in the art–between the semiconductor packages and/or between a semiconductor package and a printed circuit board.

Referring now to FIGURE 18, there is shown a side-elevational, cross-sectional view of semiconductor package 170, a seventh embodiment of a semiconductor package constructed in accordance with the principles of the present invention. Semiconductor package 170 is similar in construction as the first embodiment of the present invention. However, leads 171 in semiconductor package 170 are staggered so that leads 171 are not placed next to each other. This staggered configuration can reduce electrical shorts caused by the close physical proximity of the leads. This staggered configuration can be applied to the leads in each one of the previously described embodiments of the semiconductor package constructed in accordance with the principles of the present invention.

The method for manufacturing the present invention will now be discussed using as an example semiconductor package 60, the first embodiment of a semiconductor package constructed in accordance with the principles of the present invention.

Referring back to FIGURE 2, there is shown semiconductor package 60. To manufacture semiconductor package 60, first, semiconductor chip 61 is attached to paddle 62 by using an adhesive. Note, in the semiconductor package of the sixth embodiment, the semiconductor chip is supported by leads instead of a paddle and so the semiconductor chip of the sixth embodiment would be attached to the leads at this step. After attaching semiconductor chip 61 to paddle 62, the semiconductor chip 61 is electrically connected to leads 63 via wires 64 using any wire bonding method known in the art. A sealing material 65 is then melted and poured onto lead frame 69, semiconductor chip 61, and wires 64. The sealing material 65 is then allowed to cool and harden. After the hardening process, excess sealing material 65 is trimmed off either manually or by using a trimming machine. At the same time, leads 63 are also trimmed to their final length. The exposed portions of the leads 63 are then coated or electroplated with a corrosion-minimizing material such as, for example, tin or gold. For the semiconductor packages of the second, third, fourth, and fifth embodiments, if the semiconductor packages are to be stacked, an additional lead-bending step can now be performed.

The following applications are being filed on the same date as the present application and all are incorporated by reference as if wholly rewritten entirely herein, including any additional matter incorporated by reference therein.

Attorney Docket No.	Title of Application	First Named Inventor
45475-00015	Semiconductor Package Having Increased Solder Joint Strength	Kil Chin Lee
45475-00016	Clamp and Heat Block Assembly for Wire Bonding a Semiconductor Package Assembly	Young Suk Chung
45475-00018	Near Chip Size Semiconductor Package	Sean Timothy Crowley
45475-00019	Semiconductor Package	Sean Timothy Crowley
45475-00020	Stackable Semiconductor Package and Method for Manufacturing Same	Sean Timothy Crowley
45475-00024	Method of and Apparatus for Manufacturing Semiconductor Packages	Hyung Ju Lee
45475-00028	Semiconductor Package Having Improved Adhesiveness and Ground Bonding	Sung Sik Jang
45475-00029	Semiconductor Package Leadframe Assembly and Method of Manufacture	Young Suk Chung

It is thus believed that the operation and construction of the present invention will be apparent from the foregoing description of the preferred exemplary embodiments. It will be obvious to a person of ordinary skill in the art that various changes and modifications may be made herein without departing from the spirit and the scope of the invention.

Although a preferred embodiment of the method and apparatus of the present invention has been illustrated in the accompanying drawings and described in the foregoing detailed description, it will be understood that the invention is not limited to the embodiment disclosed, but is capable of numerous rearrangements, modifications, and substitutions without departing from the spirit of the invention as set forth and defined by the following claims.

CLAIMS

WHAT IS CLAIMED IS:

1. A semiconductor package for a semiconductor chip, said semiconductor package comprising:

a lead frame having a plurality of leads, each one of said plurality of leads having a top portion forming a part of a top surface of said semiconductor package and a bottom portion resting flush against a bottom surface of said semiconductor package and being flush therewith;

a plurality of electrical paths electrically connecting said semiconductor chip to said plurality of leads; and

sealing material securing said lead frame, said semiconductor chip, and said plurality of electrical paths.

2. The semiconductor package of claim 1 wherein said lead frame constructed with a chip paddle having a bottom side resting flush against said bottom surface of said semiconductor package.

3. The semiconductor package of claim1 wherein said top portion of each of said plurality of leads rest against a part of said top surface of said semiconductor chip.

4. The semiconductor package of claim 1 wherein said top portion of each one of said plurality of leads extends generally perpendicularly from said top surface of said semiconductor chip.

5. The semiconductor package of claim 1 wherein said top portion and said bottom portion of said plurality of leads are electroplated.

6. The semiconductor package of claim1 wherein said plurality of electrical paths are a plurality of wires.

7. The semiconductor package of claim 6 wherein said plurality of electrically conductive wires are selected from the group consisting of: silver, gold, or aluminum.

8. The semiconductor package of claim 2 wherein said plurality of leads are arranged in at least one single line surrounding said paddle.

9. A semiconductor package of claim 2 wherein said plurality of leads are randomly dispersed in a plurality of lines surrounding said paddle.

10. A method for stacking semiconductor packages, comprising the steps of:

physically and electrically connecting a bottom side of a first semiconductor package to a printed circuit board, said first semiconductor package having a first plurality of leads, each one of said first plurality of leads having a first section exposed to a first top surface of said first semiconductor package and a second section resting flush against a first bottom surface of said first semiconductor package; and

physically and electrically connecting a second semiconductor package to said top of said first semiconductor package, said second semiconductor package having a second plurality of leads in generally the same position as said first plurality of leads.

11. The method for stacking semiconductor packages as in claim 10 wherein said first semiconductor package is soldered to said printed circuit board.

12. A method for stacking semiconductor packages as in claim 10 wherein said second semiconductor package is soldered to said first semiconductor package.

13. A method for manufacturing a semiconductor package, comprising the steps of:

attaching a semiconductor chip to a paddle of a lead frame, said lead frame having a plurality of leads surrounding said paddle;

electrically connecting said semiconductor chip to each one of said plurality of leads via a plurality of wires;

applying a sealing material to secure said semiconductor chip, said lead frame, and said plurality of wires, said sealing material forming a top side and a bottom side of said semiconductor package, with a first section of each of said plurality of leads exposed to said top side of said semiconductor package and a second section of each of said plurality of leads resting flush against said bottom side of said semiconductor package; and trimming off a portion of said lead frame and said sealing material.