FIG. 1

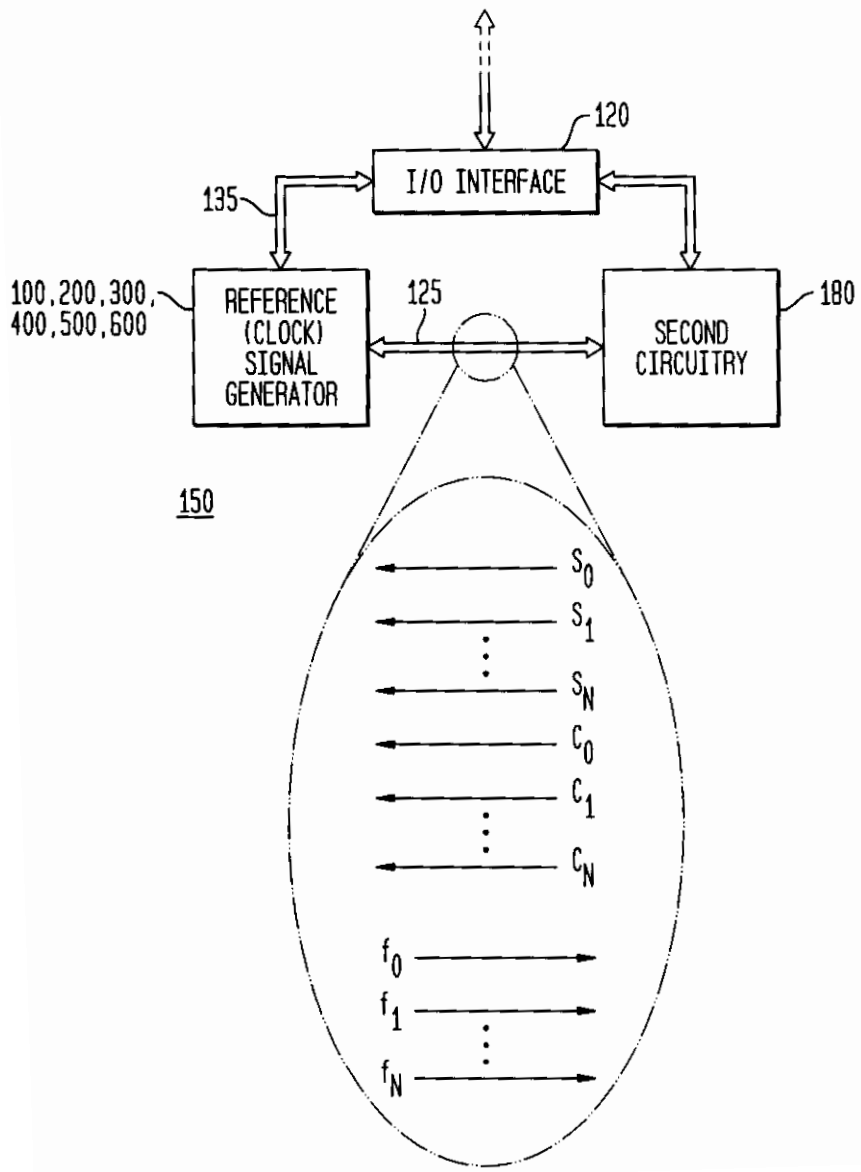

120
I/O INTERFACE
135
100,200,300,
400,500,600
REFERENCE
(CLOCK)
SIGNAL
GENERATOR
125
SECOND
CIRCUITRY
180
150
$S_0$
$S_1$
$S_N$
$C_0$
$C_1$
$C_N$
$f_0$
$f_1$
$f_N$

FIG. 2

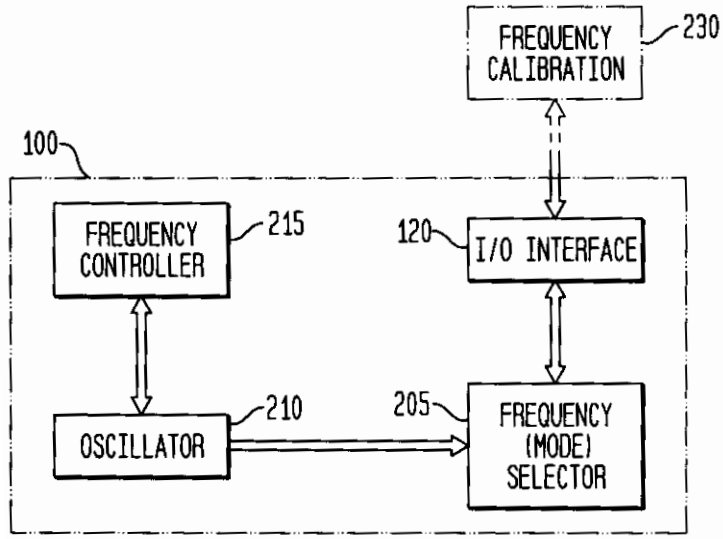

FREQUENCY CALIBRATION
230
100
FREQUENCY CONTROLLER
215
120
I/O INTERFACE
OSCILLATOR
210
205
FREQUENCY (MODE) SELECTOR

FIG. 3

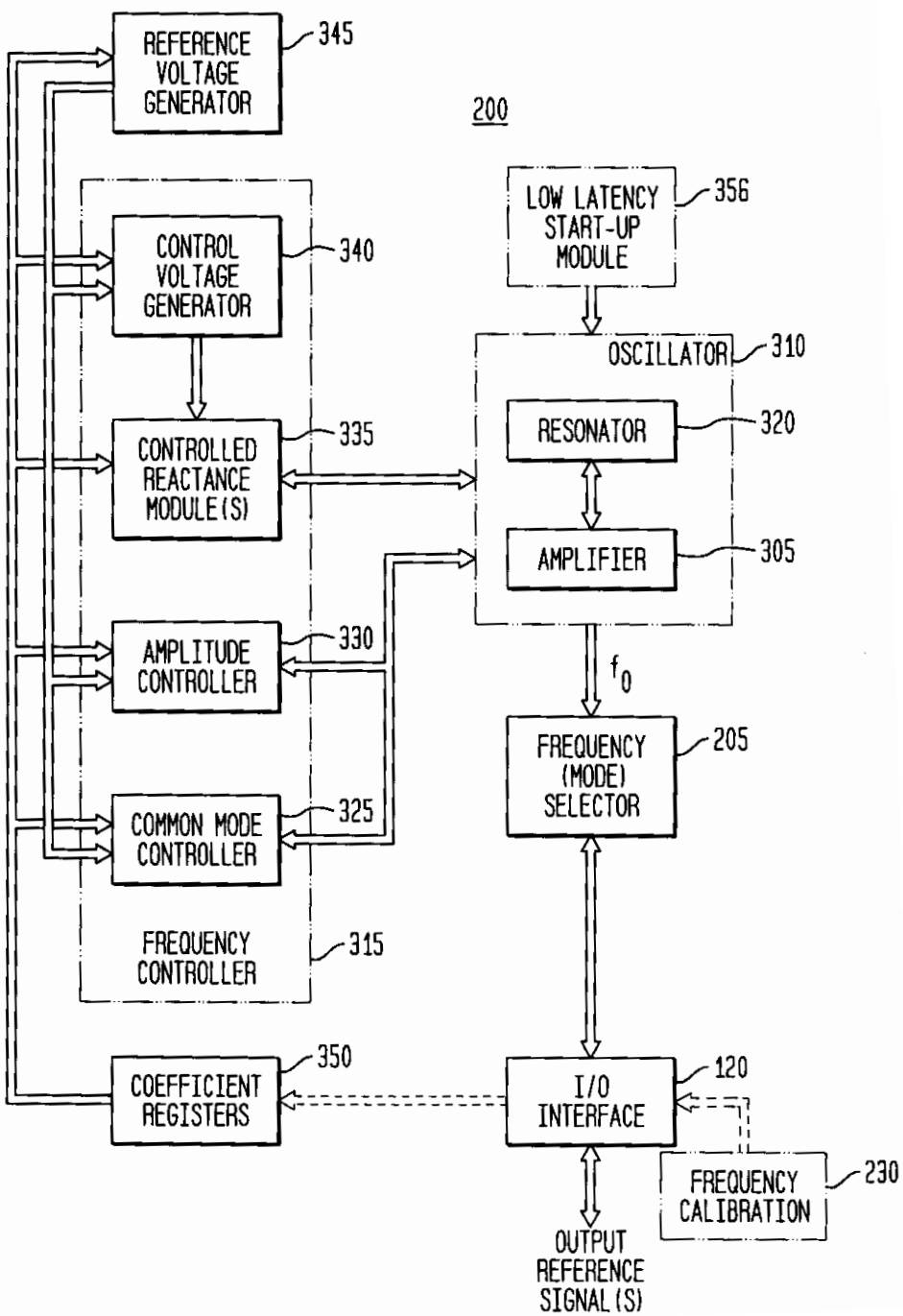

REFERENCE VOLTAGE GENERATOR
345
200
LOW LATENCY START-UP MODULE
356
CONTROL VOLTAGE GENERATOR
340
OSCILLATOR
310
CONTROLLED REACTANCE MODULE(S)
335
RESONATOR
320
AMPLIFIER
305
AMPLITUDE CONTROLLER
330
$f_0$
FREQUENCY (MODE) SELECTOR
205
COMMON MODE CONTROLLER
325
FREQUENCY CONTROLLER
315
COEFFICIENT REGISTERS
350
I/O INTERFACE
120
FREQUENCY CALIBRATION
230
OUTPUT REFERENCE SIGNAL(S)

FIG. 4

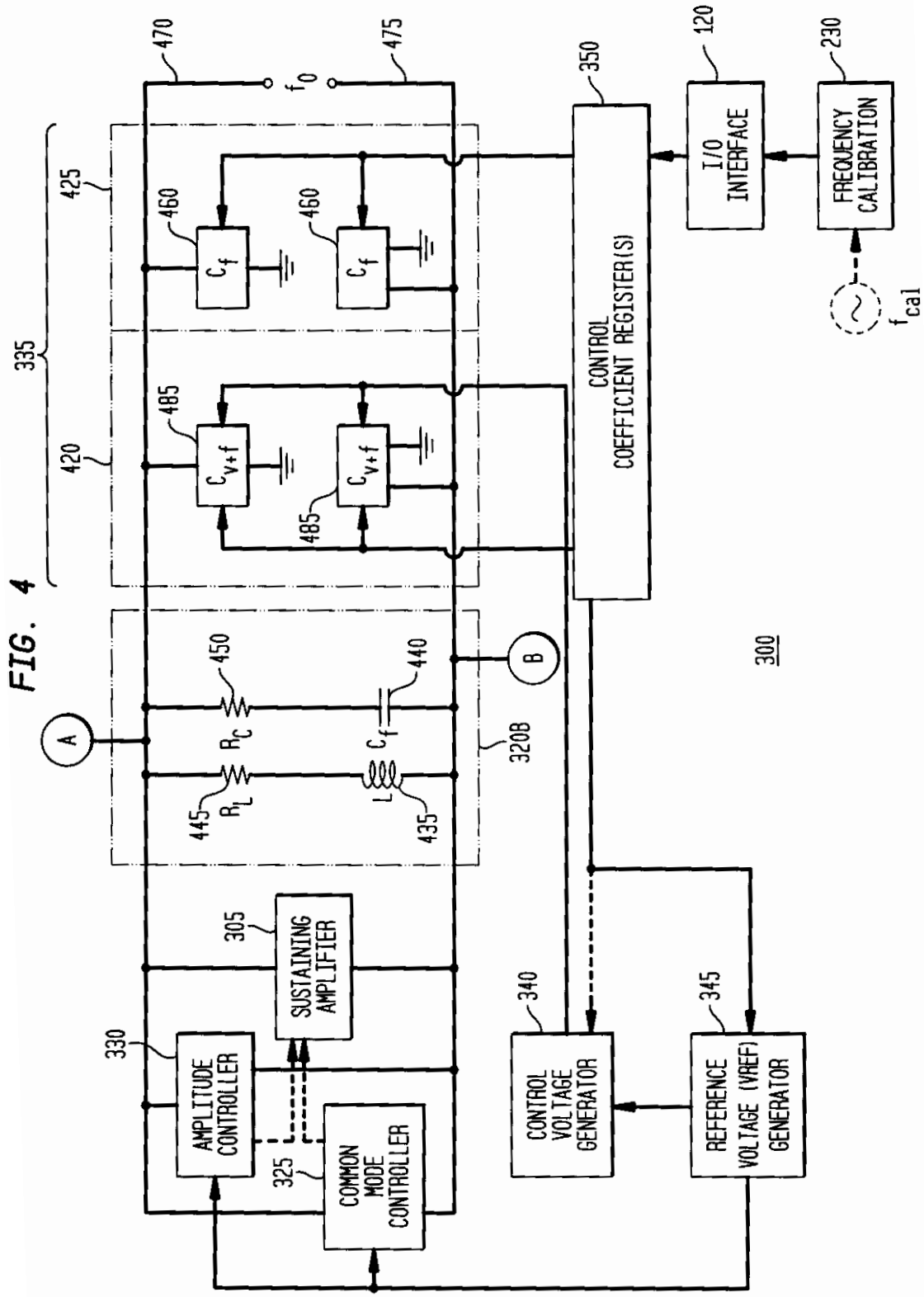

300
335
425
420
470
475
$f_0$
460
$C_f$
485
$C_{V+f}$
450
$R_C$
440
$C_f$
445
$R_L$
L
435
320B
A
B
305
SUSTAINING AMPLIFIER
330
AMPLITUDE CONTROLLER
325
COMMON MODE CONTROLLER
340
CONTROL VOLTAGE GENERATOR
345
REFERENCE VOLTAGE (VREF) GENERATOR
350
CONTROL COEFFICIENT REGISTER(S)
120
I/O INTERFACE
230
FREQUENCY CALIBRATION
$f_{cal}$

FIG. 5

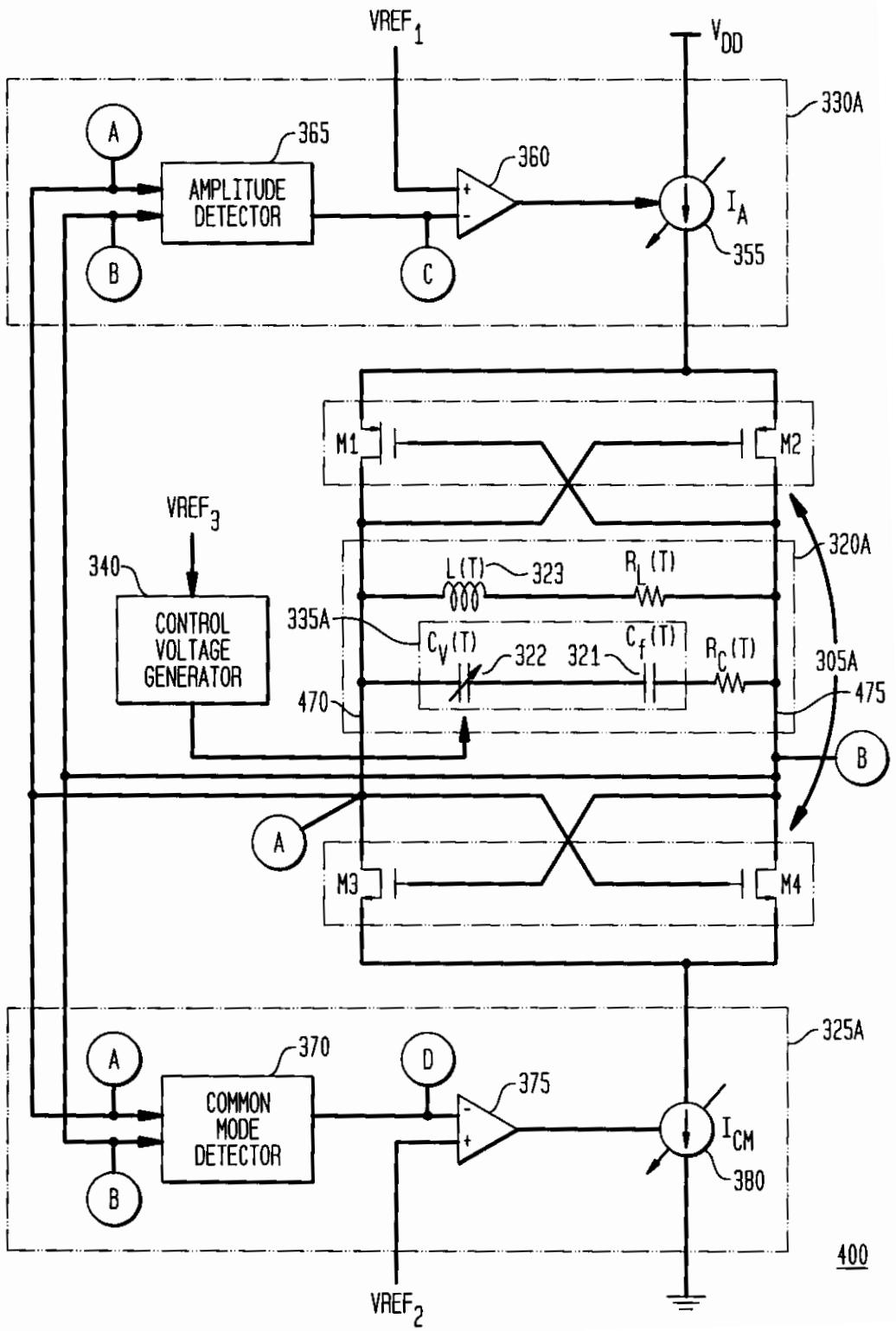

VREF1
VDD
330A
A
365
AMPLITUDE DETECTOR
360
B
C
IA
355
M1
M2
VREF3
320A
340
L(T)
323
RL(T)
CONTROL VOLTAGE GENERATOR
335A
CV(T)
322
321
Cf(T)
RC(T)
305A
470
475
B
A
M3
M4
325A
370
D
375
A
COMMON MODE DETECTOR
ICM
B
380
400
VREF2

FIG. 6

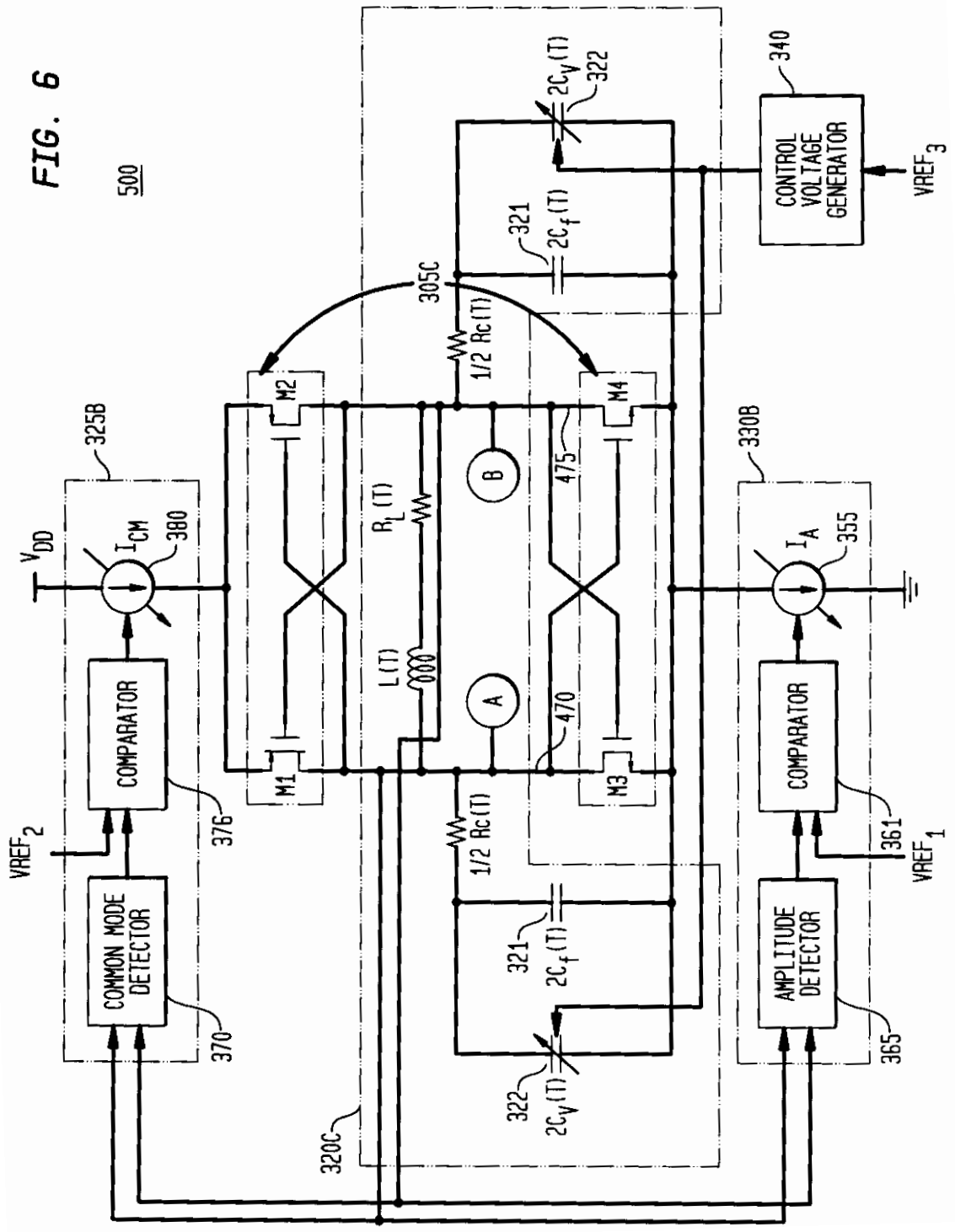

500
340
CONTROL VOLTAGE GENERATOR
VREF3
322
2Cv(T)
321
2Cf(T)
305C
1/2 Rc(T)
325B
330B
VDD
ICM
380
IA
355
M1
M2
M3
M4
RL(T)
L(T)
A
B
470
475
COMPARATOR
376
361
VREF2
VREF1
COMMON MODE DETECTOR
370
AMPLITUDE DETECTOR
365
320C

FIG. 7

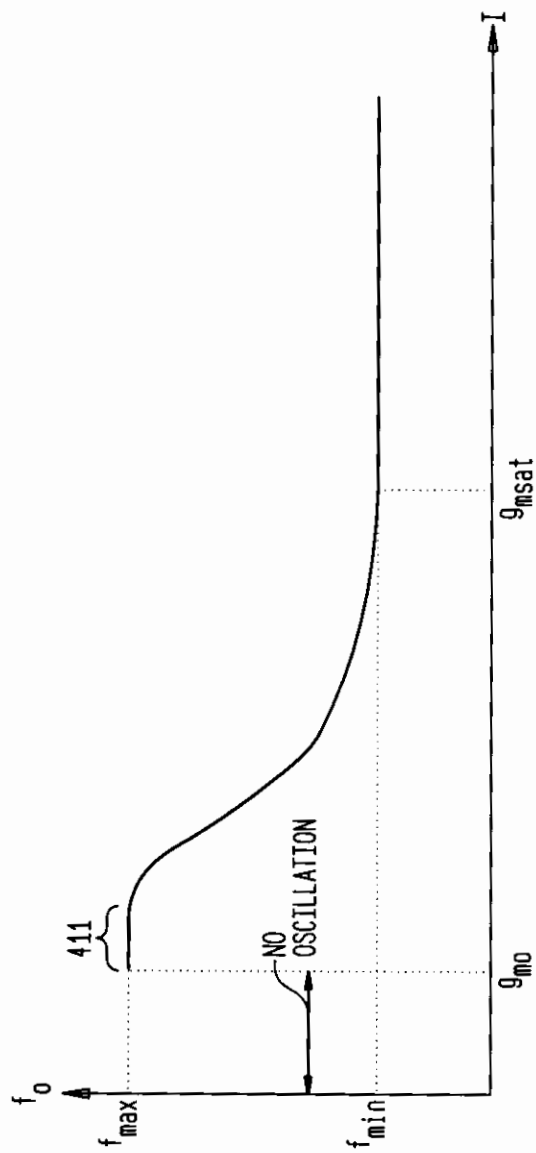


FIG. 8

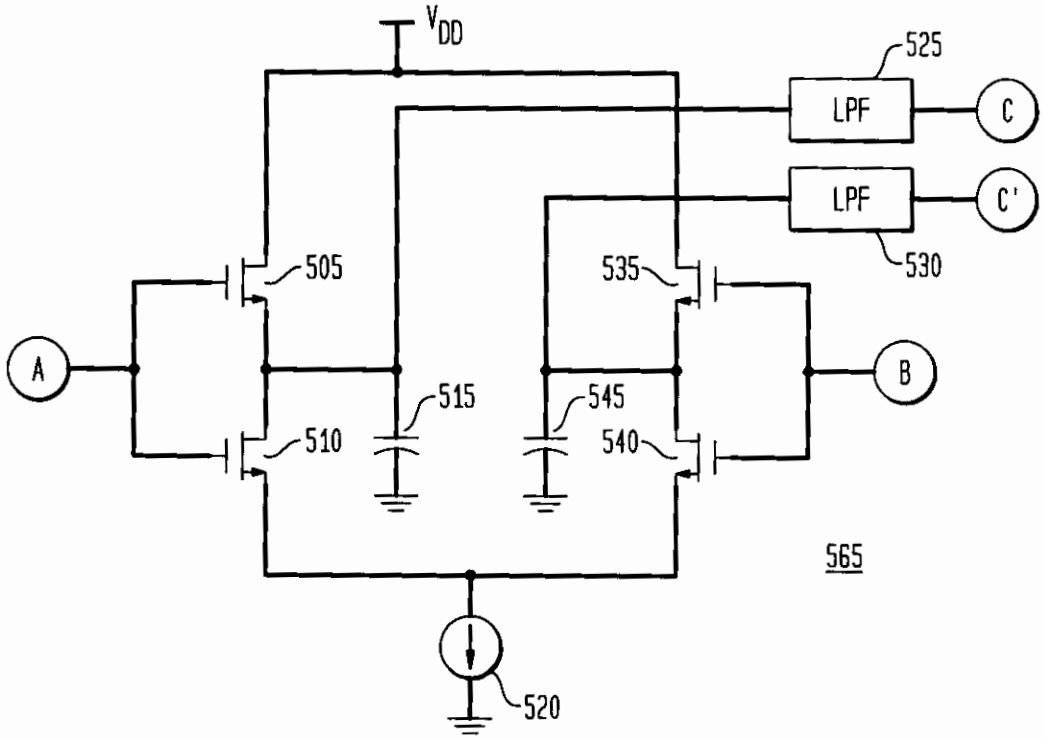

$V_{DD}$
525
LPF
C
LPF
C'
530
505
535
A
B
515
545
510
540
565
520

FIG. 9

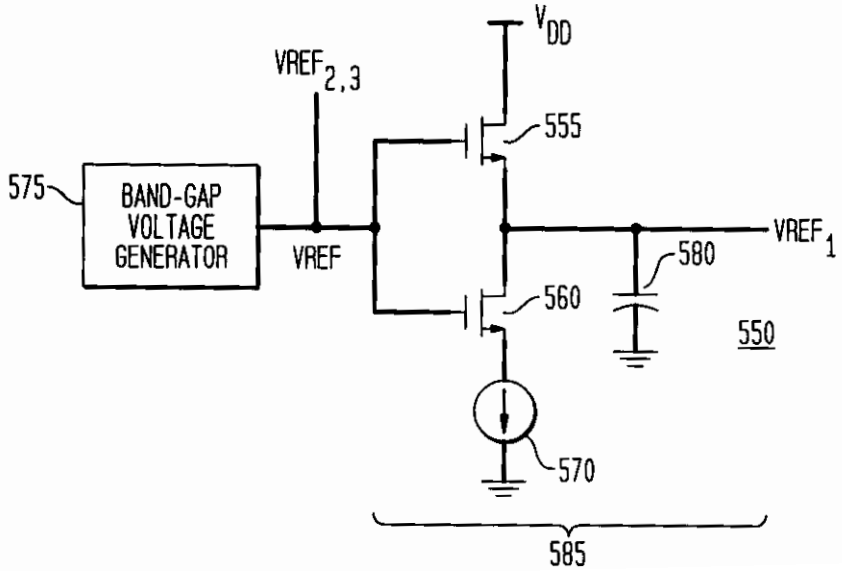

$V_{DD}$
$VREF_{2,3}$
555
575
BAND-GAP VOLTAGE GENERATOR
VREF
$VREF_1$
580
560
550
570
585

FIG. 10

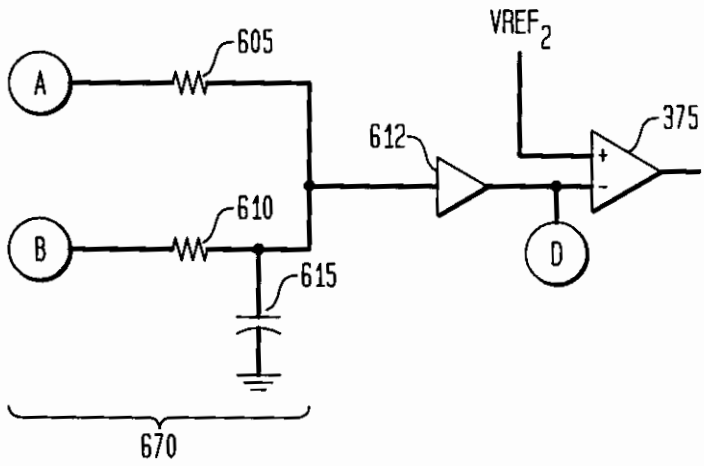



FIG. 11

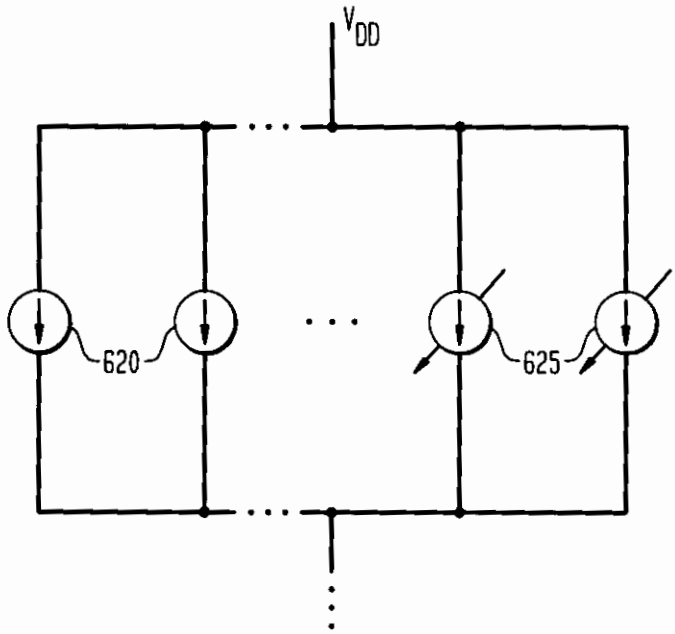


FIG. 12

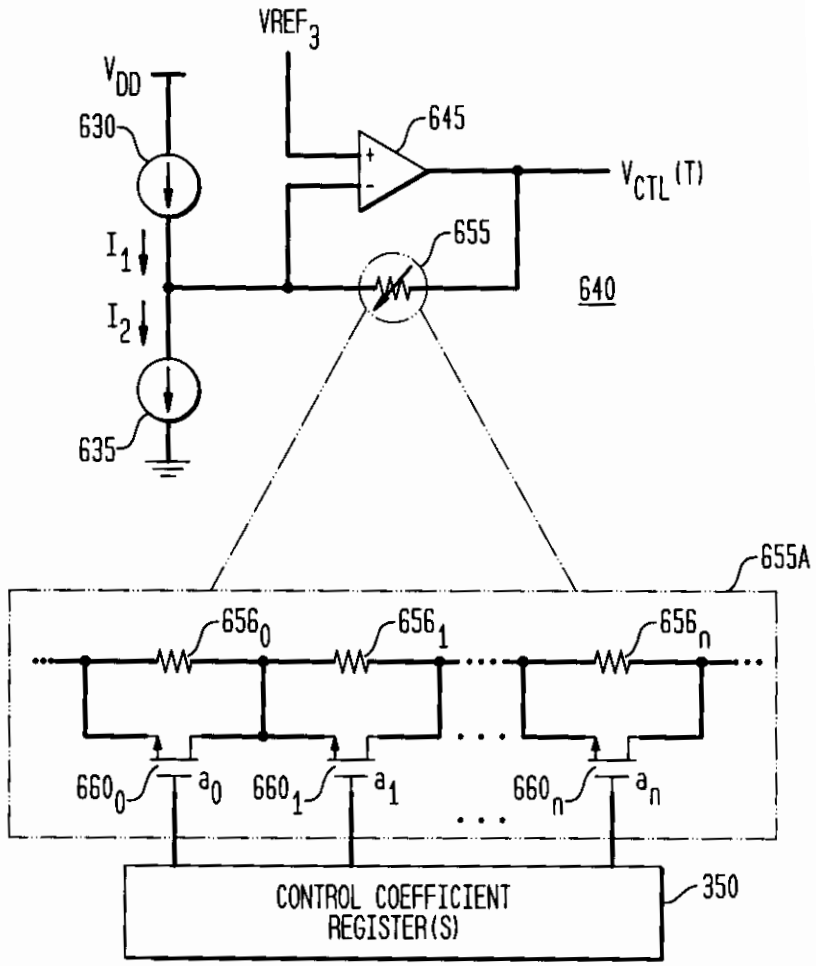

VREF3
VDD
630
645
VCTL(T)
I1
655
640
I2
635
655A
656₀
656₁
656n
660₀
a0
660₁
a1
660n
an
CONTROL COEFFICIENT REGISTER(S)
350

FIG. 13A

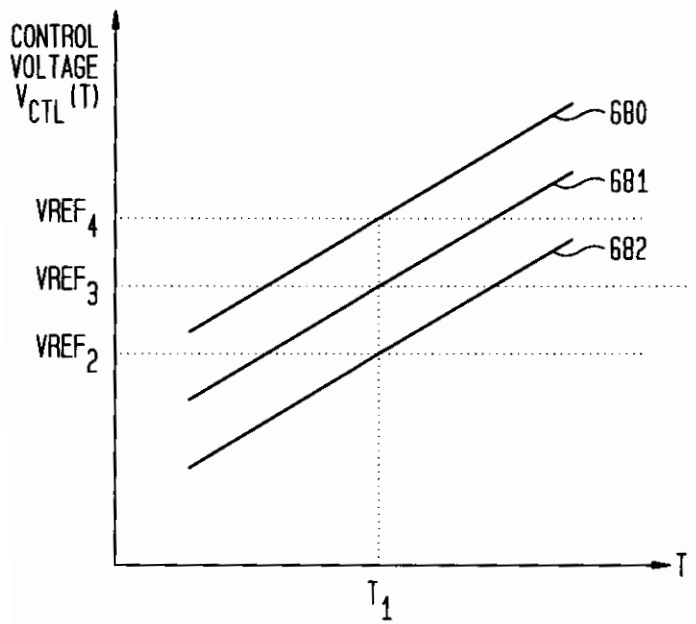



FIG. 13B

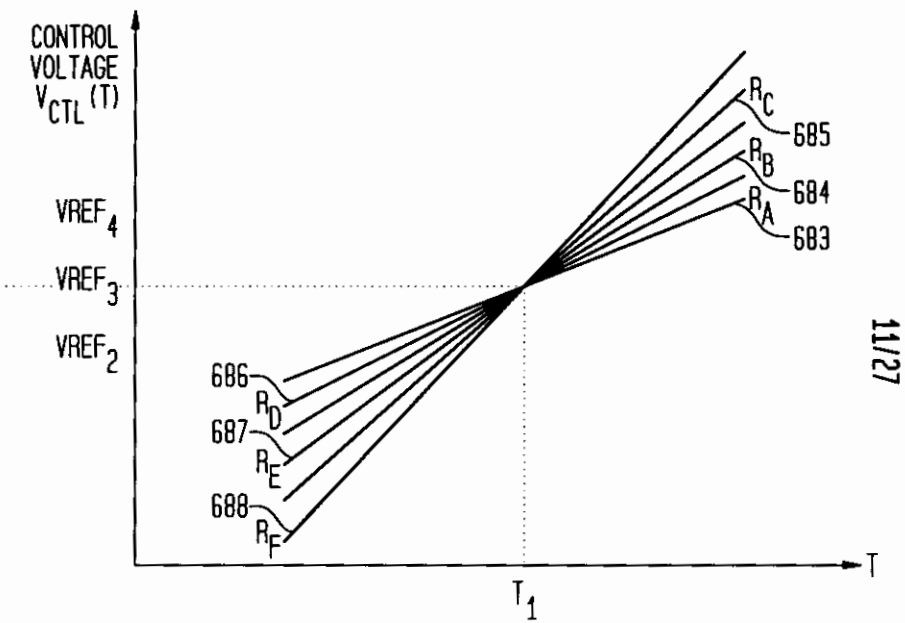


FIG. 14

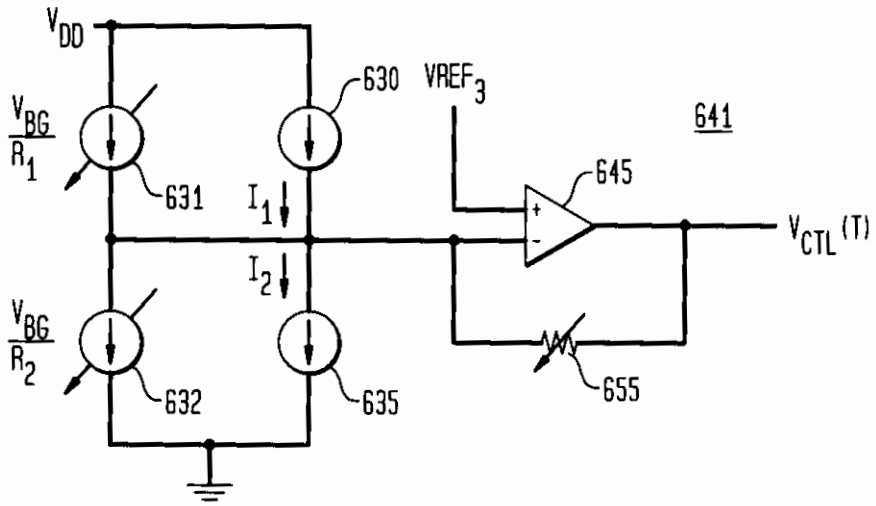

$V_{DD}$
$\frac{V_{BG}}{R_1}$
$\frac{V_{BG}}{R_2}$
630
631
632
635
$I_1$
$I_2$
$VREF_3$
641
645
655
$V_{CTL}(T)$

FIG. 15

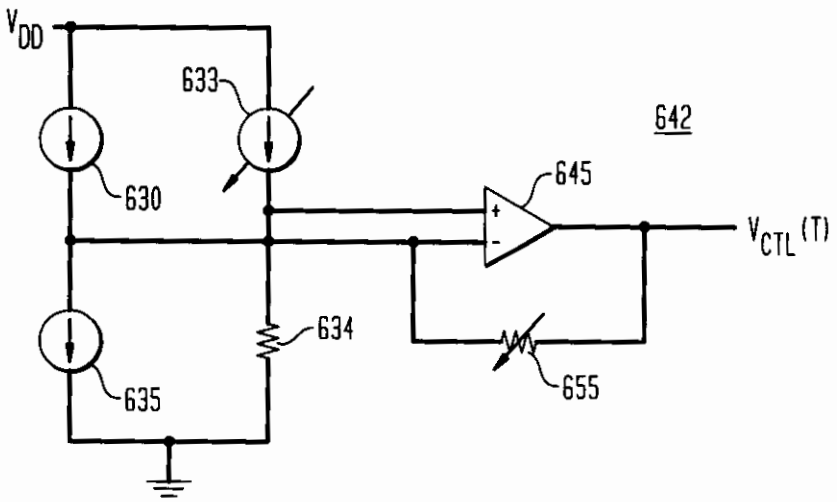

$V_{DD}$
633
630
634
635
642
645
655
$V_{CTL}(T)$

FIG. 16

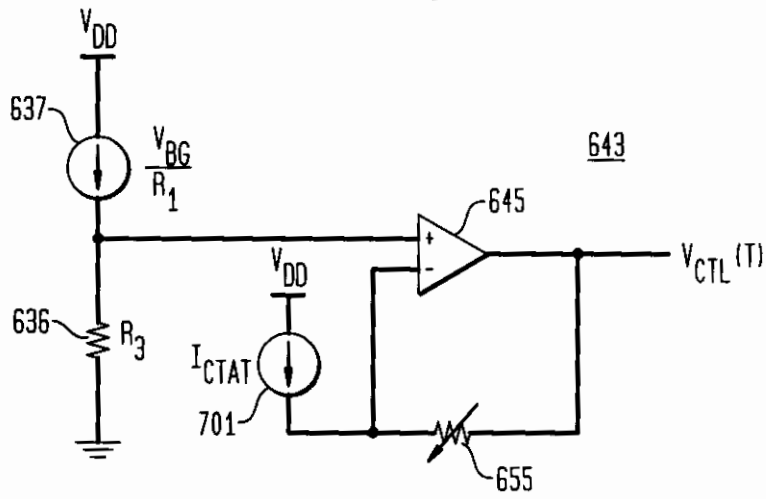

$V_{DD}$
637
$\frac{V_{BG}}{R_1}$
643
645
$V_{CTL}(T)$
$V_{DD}$
636
$R_3$
$I_{CTAT}$
701
655

FIG. 17

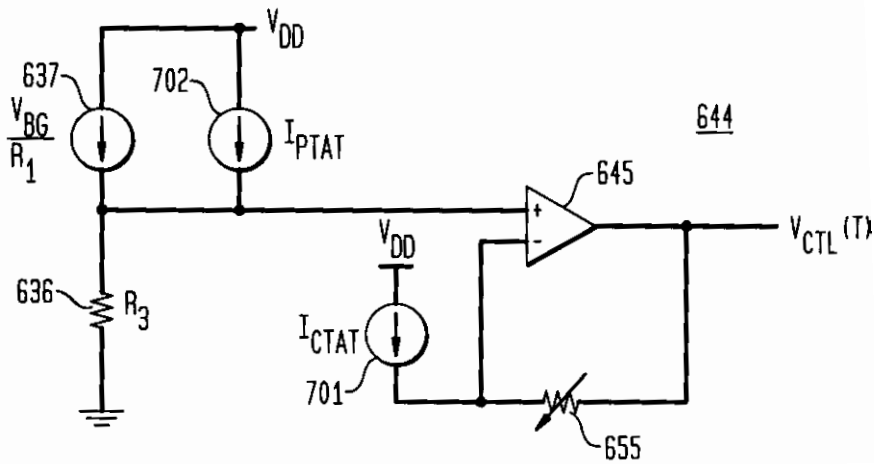

$V_{DD}$
637
702
$\frac{V_{BG}}{R_1}$
$I_{PTAT}$
644
645
$V_{CTL}(T)$
$V_{DD}$
636
$R_3$
$I_{CTAT}$
701
655

FIG. 18

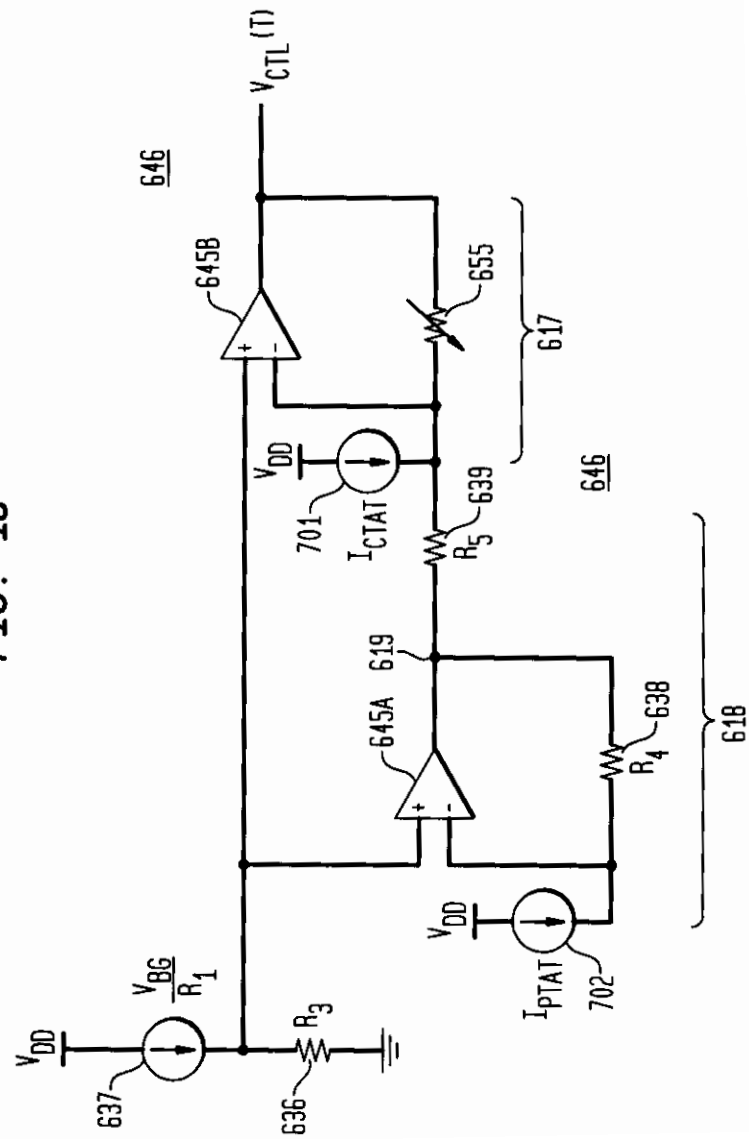

$V_{CTL}(T)$
646
645B
655
617
$V_{DD}$
701
$I_{CTAT}$
639
$R_5$
646
619
645A
638
$R_4$
618
$V_{DD}$
$I_{PTAT}$
702
$V_{DD}$
637
$\frac{V_{BG}}{R_1}$
636
$R_3$

FIG. 19

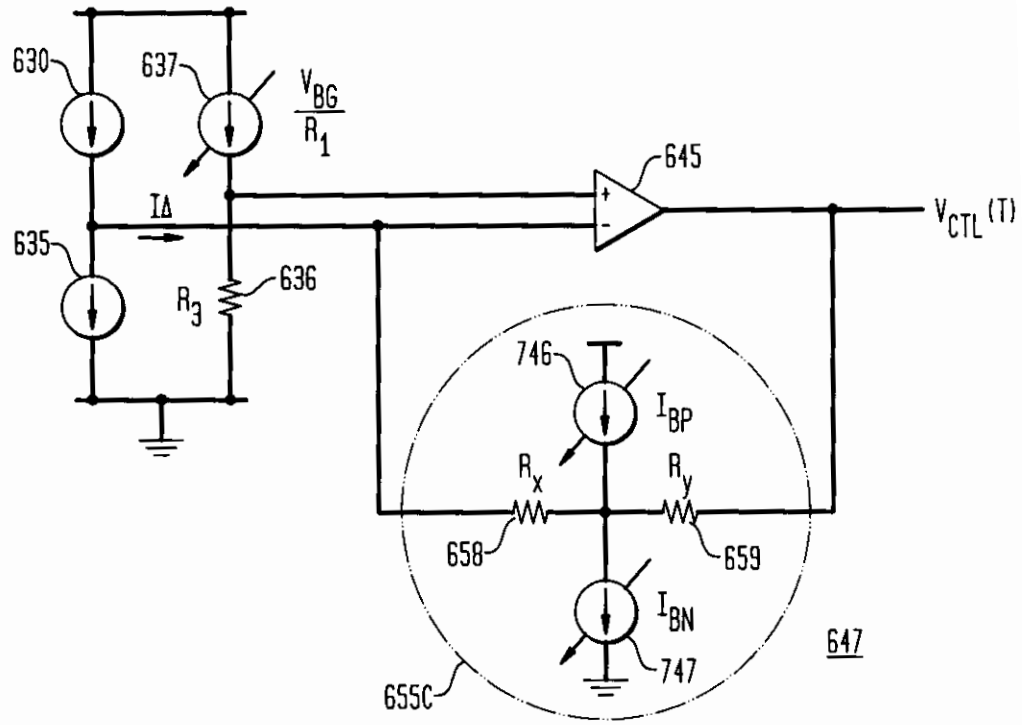

630
637
$\frac{V_{BG}}{R_1}$
645
$V_{CTL}(T)$
IΔ
635
636
$R_3$
746
$I_{BP}$
$R_x$
$R_y$
658
659
$I_{BN}$
747
647
655C

FIG. 20

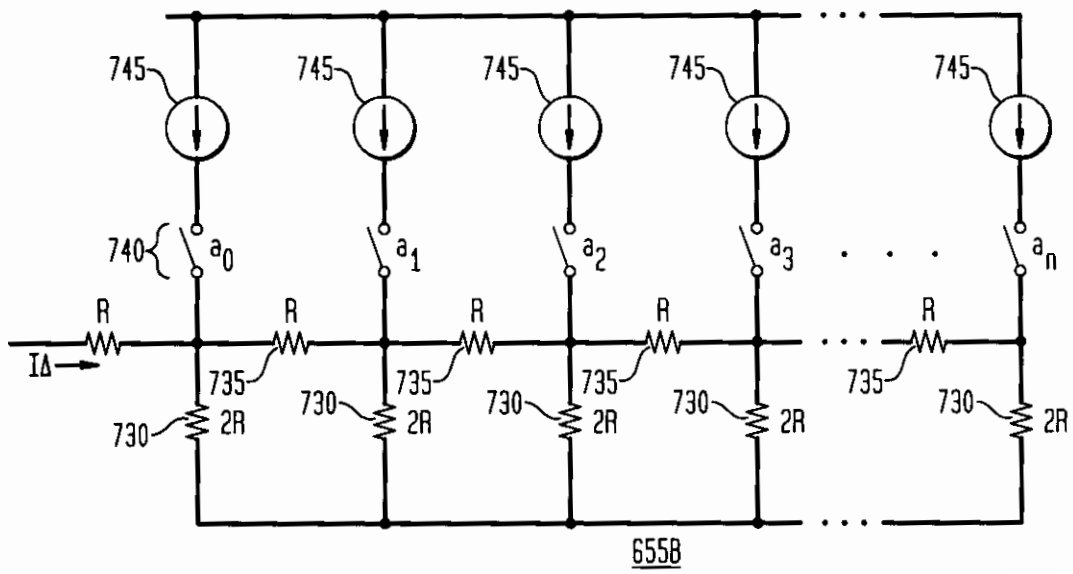

745
740
$a_0$
$a_1$
$a_2$
$a_3$
$a_n$
R
IΔ
735
730
2R
655B

FIG. 21

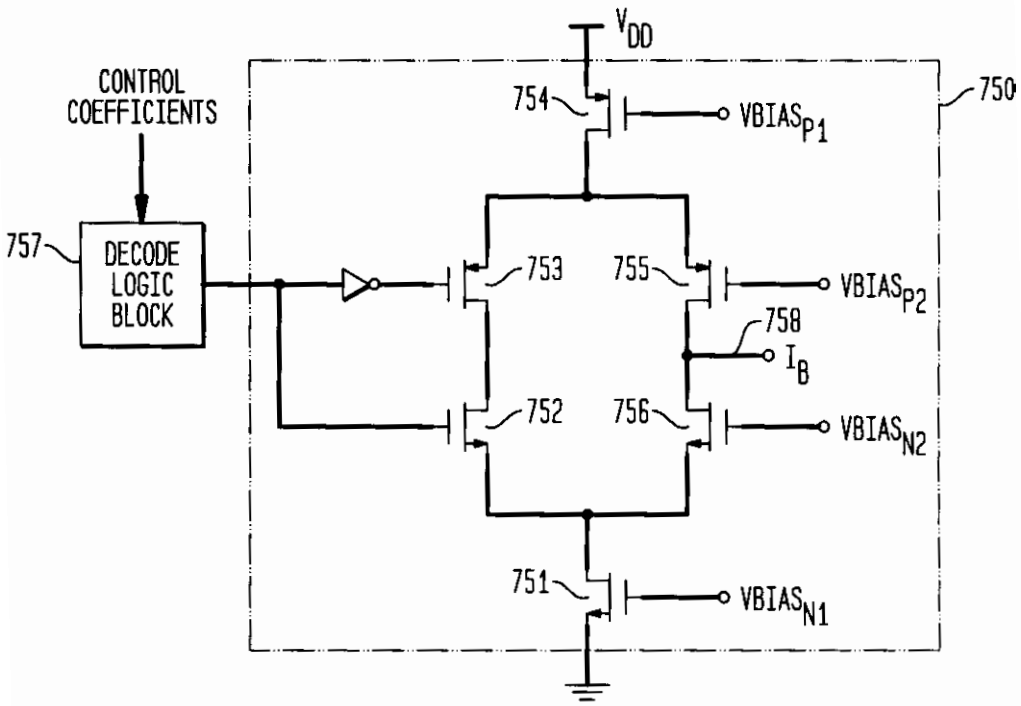

$V_{DD}$
CONTROL COEFFICIENTS
757
DECODE LOGIC BLOCK
754
$VBIAS_{P1}$
750
753
755
$VBIAS_{P2}$
758
$I_B$
752
756
$VBIAS_{N2}$
751
$VBIAS_{N1}$

FIG. 22

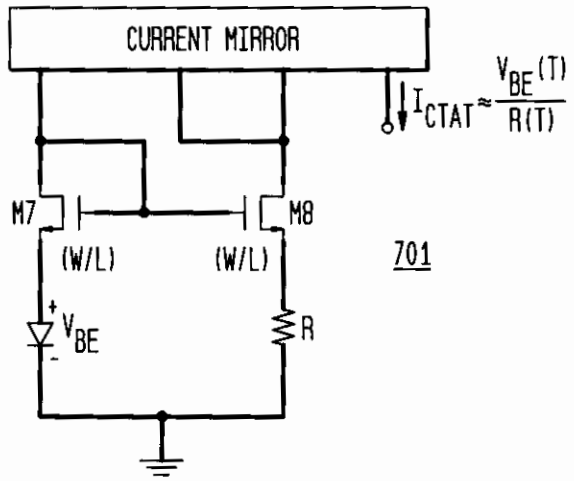

CURRENT MIRROR
$I_{CTAT} \approx \frac{V_{BE}(T)}{R(T)}$
M7
M8
(W/L)
(W/L)
701
$V_{BE}$
R

FIG. 23

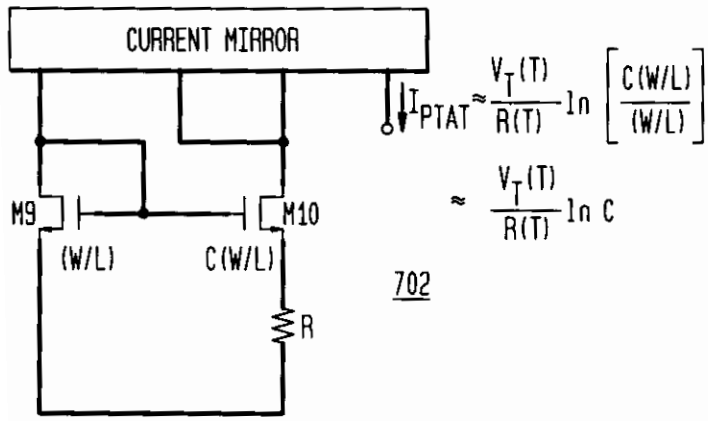

CURRENT MIRROR
$I_{PTAT} \approx \frac{V_T(T)}{R(T)} \ln \left[\frac{C(W/L)}{(W/L)}\right]$
$\approx \frac{V_T(T)}{R(T)} \ln C$
M9
M10
(W/L)
C(W/L)
702
R

FIG. 24

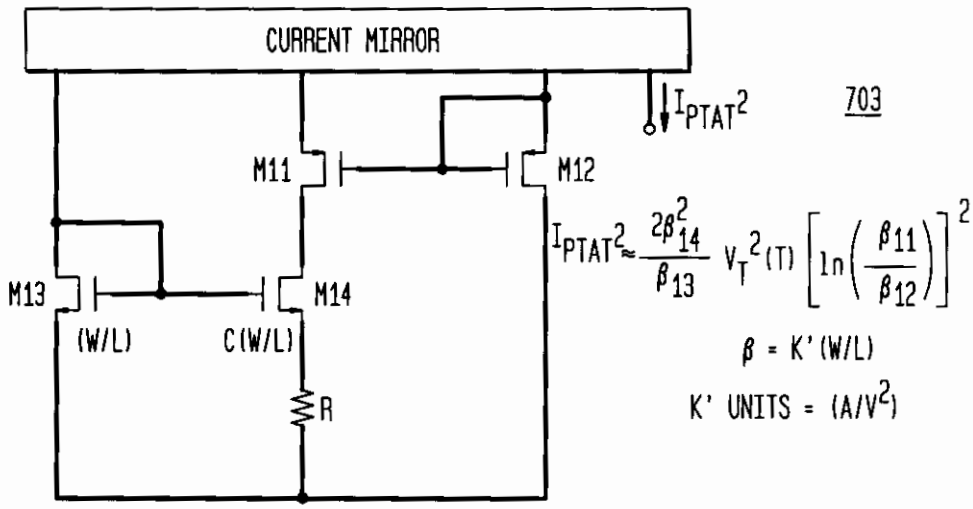

CURRENT MIRROR
$I_{PTAT}^2$
703
M11
M12
M13
M14
(W/L)
C(W/L)
R
$I_{PTAT}^2 \approx \frac{2\beta_{14}^2}{\beta_{13}} V_T^2(T) \left[\ln\left(\frac{\beta_{11}}{\beta_{12}}\right)\right]^2$
$\beta = K'(W/L)$
K' UNITS = $(A/V^2)$

FIG. 25

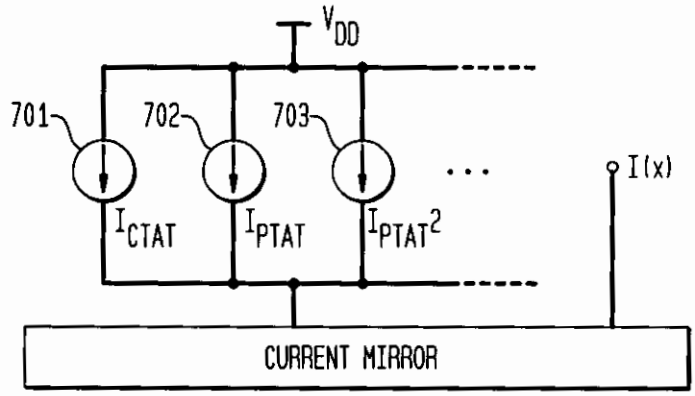

$V_{DD}$
701
702
703
$I_{CTAT}$
$I_{PTAT}$
$I_{PTAT}^2$
I(x)
CURRENT MIRROR

FIG. 26

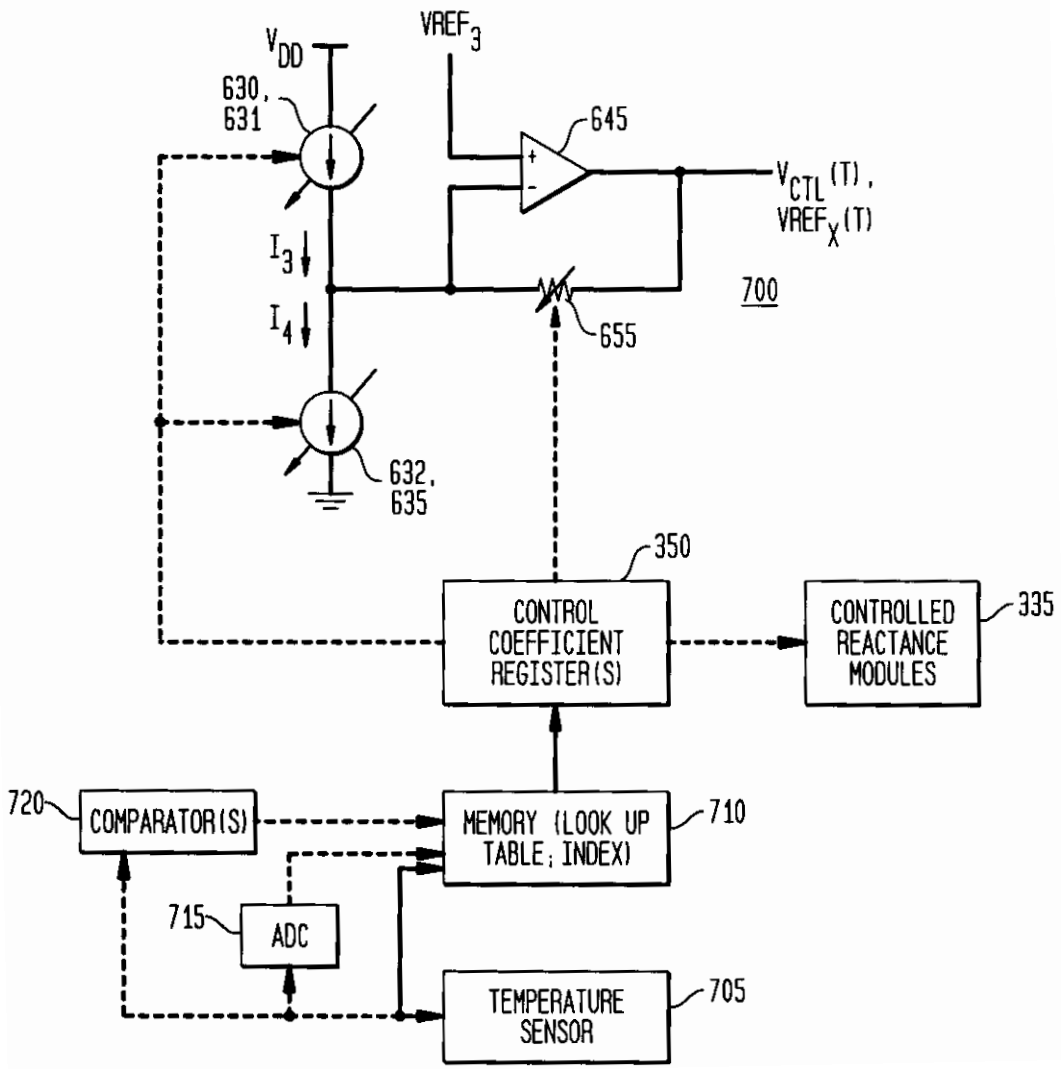

$V_{DD}$
$VREF_3$
630, 631
645
$V_{CTL}(T)$, $VREF_X(T)$
$I_3$
$I_4$
700
655
632, 635
350
CONTROL COEFFICIENT REGISTER(S)
CONTROLLED REACTANCE MODULES
335
720
COMPARATOR(S)
MEMORY (LOOK UP TABLE; INDEX)
710
715
ADC
TEMPERATURE SENSOR
705

FIG. 27

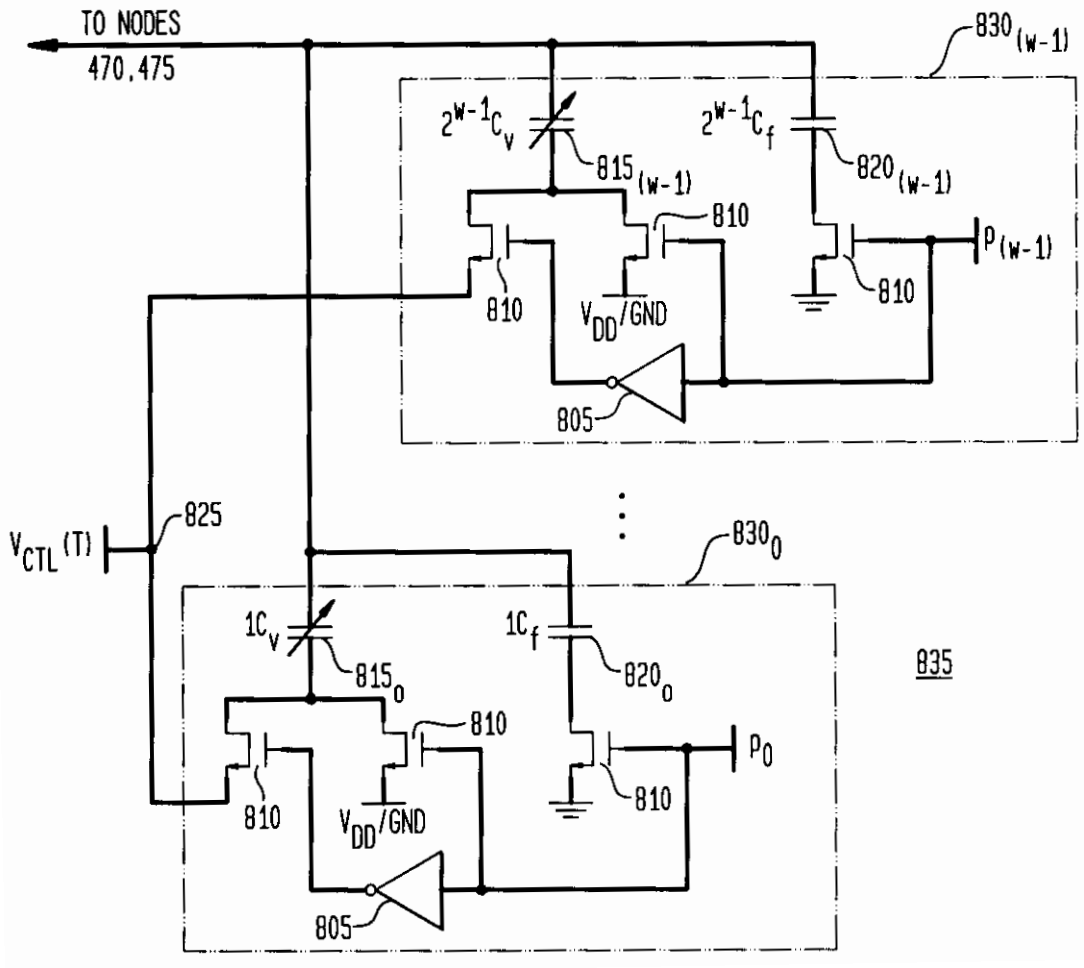

TO NODES
470,475
$830_{(w-1)}$
$2^{w-1}C_v$
$2^{w-1}C_f$
$815_{(w-1)}$
$820_{(w-1)}$
810
$P_{(w-1)}$
$V_{DD}/GND$
805
$V_{CTL}(T)$
825
$830_0$
$1C_v$
$1C_f$
$815_0$
$820_0$
$P_0$
835

FIG. 28

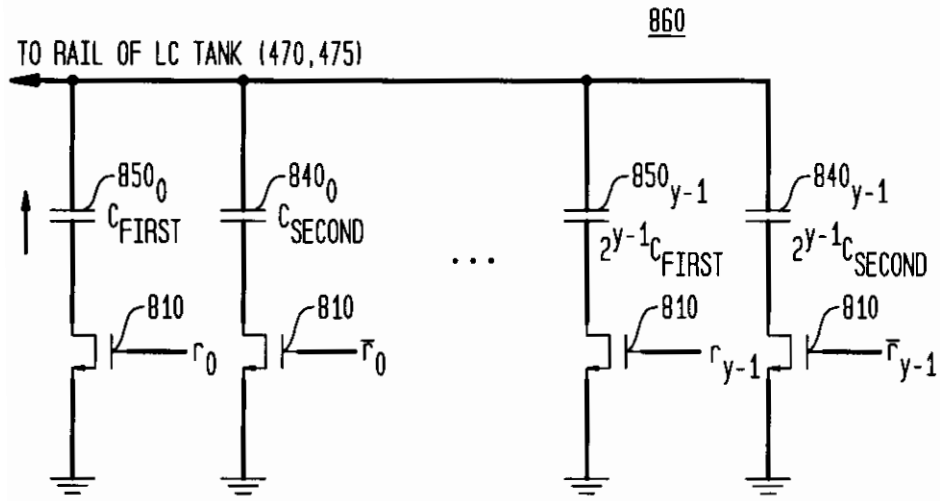

860
TO RAIL OF LC TANK (470,475)
$850_0$
$C_{FIRST}$
$840_0$
$C_{SECOND}$
$850_{y-1}$
$2^{y-1}C_{FIRST}$
$840_{y-1}$
$2^{y-1}C_{SECOND}$
810
$r_0$
$\overline{r}_0$
$r_{y-1}$
$\overline{r}_{y-1}$

FIG. 29

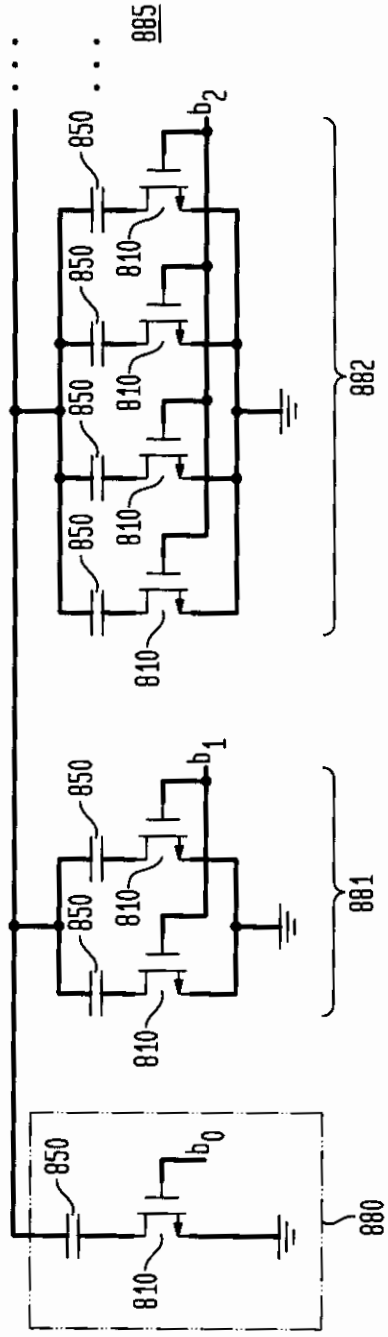

885
882
881
880
850
810
$b_2$
$b_1$
$b_0$

FIG. 30

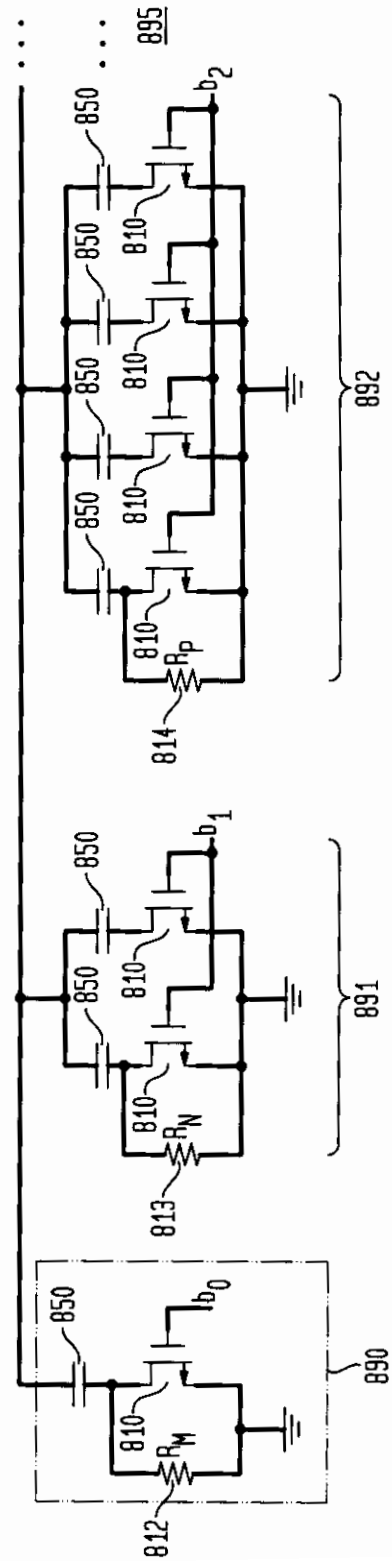

895
892
891
890
850
810
$b_2$
$b_1$
$b_0$
$R_P$
$R_N$
$R_M$
814
813
812

FIG. 31

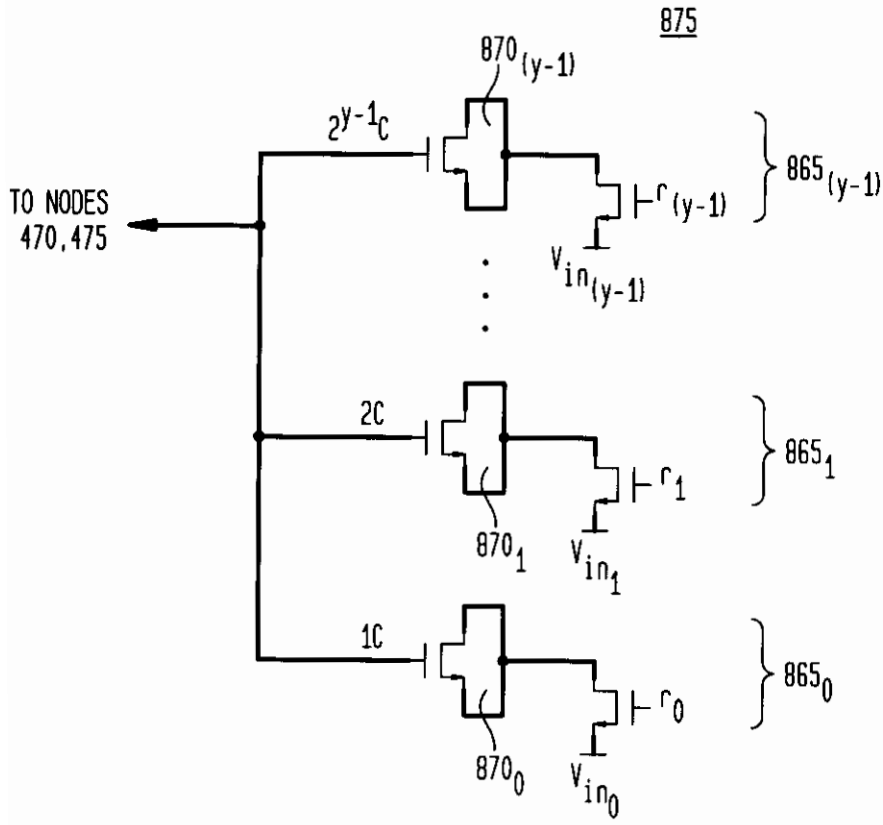

875
870(y-1)
2y-1C
TO NODES
470,475
r(y-1)
865(y-1)
Vin(y-1)
2C
r1
865 1
870 1
Vin1
1C
r0
865 0
870 0
Vin0

FIG. 32

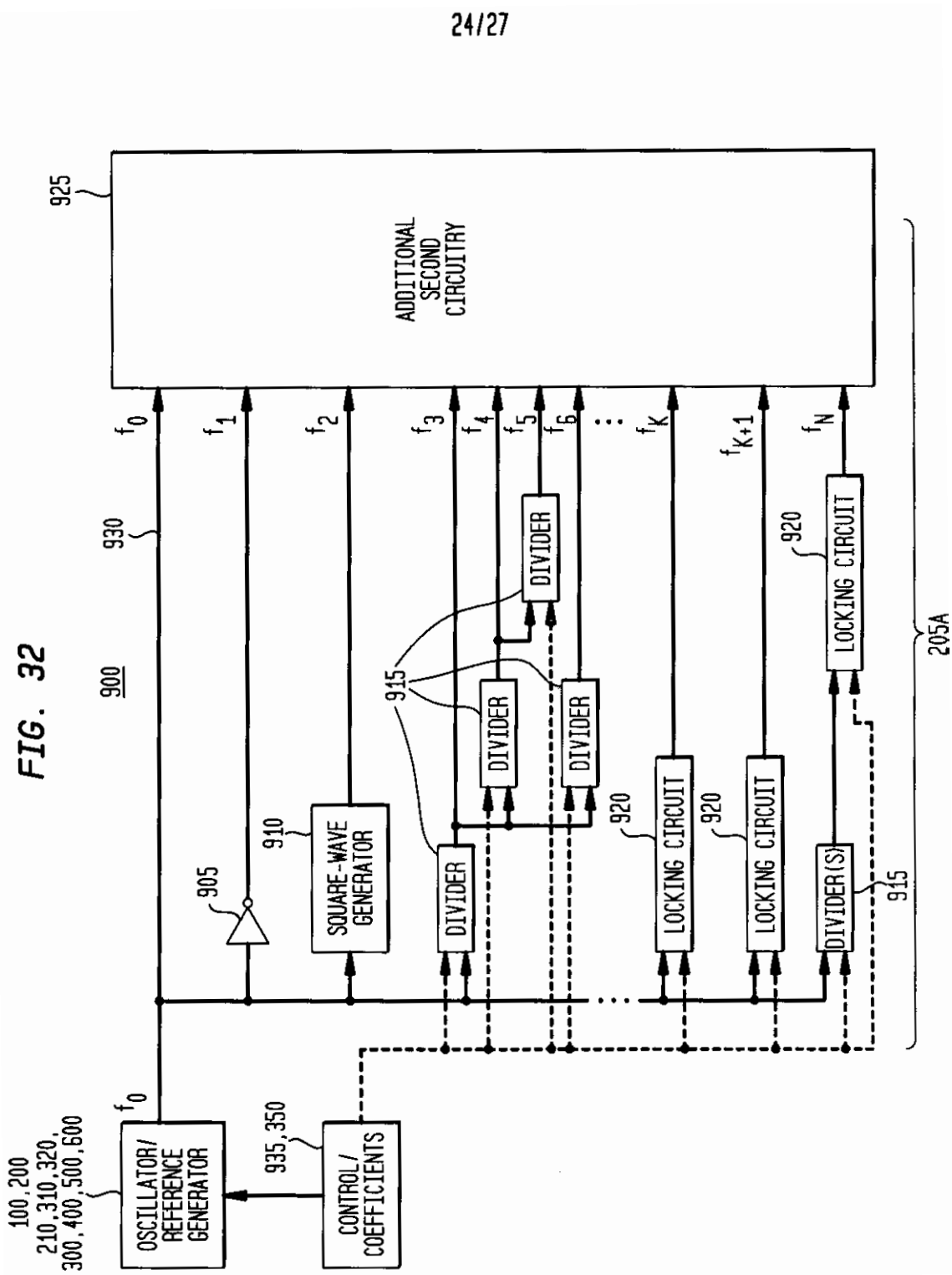

100, 200
210, 310, 320,
300, 400, 500, 600
OSCILLATOR/
REFERENCE
GENERATOR
$f_0$
935, 350
CONTROL/
COEFFICIENTS
900
930
905
910
SQUARE-WAVE
GENERATOR
915
DIVIDER
DIVIDER
DIVIDER
DIVIDER
DIVIDER(S)
920
LOCKING CIRCUIT
LOCKING CIRCUIT
LOCKING CIRCUIT
920
920
925
ADDITIONAL
SECOND
CIRCUITRY
$f_0$
$f_1$
$f_2$
$f_3$
$f_4$
$f_5$
$f_6$
$f_K$
$f_{K+1}$
$f_N$
205A

FIG. 33

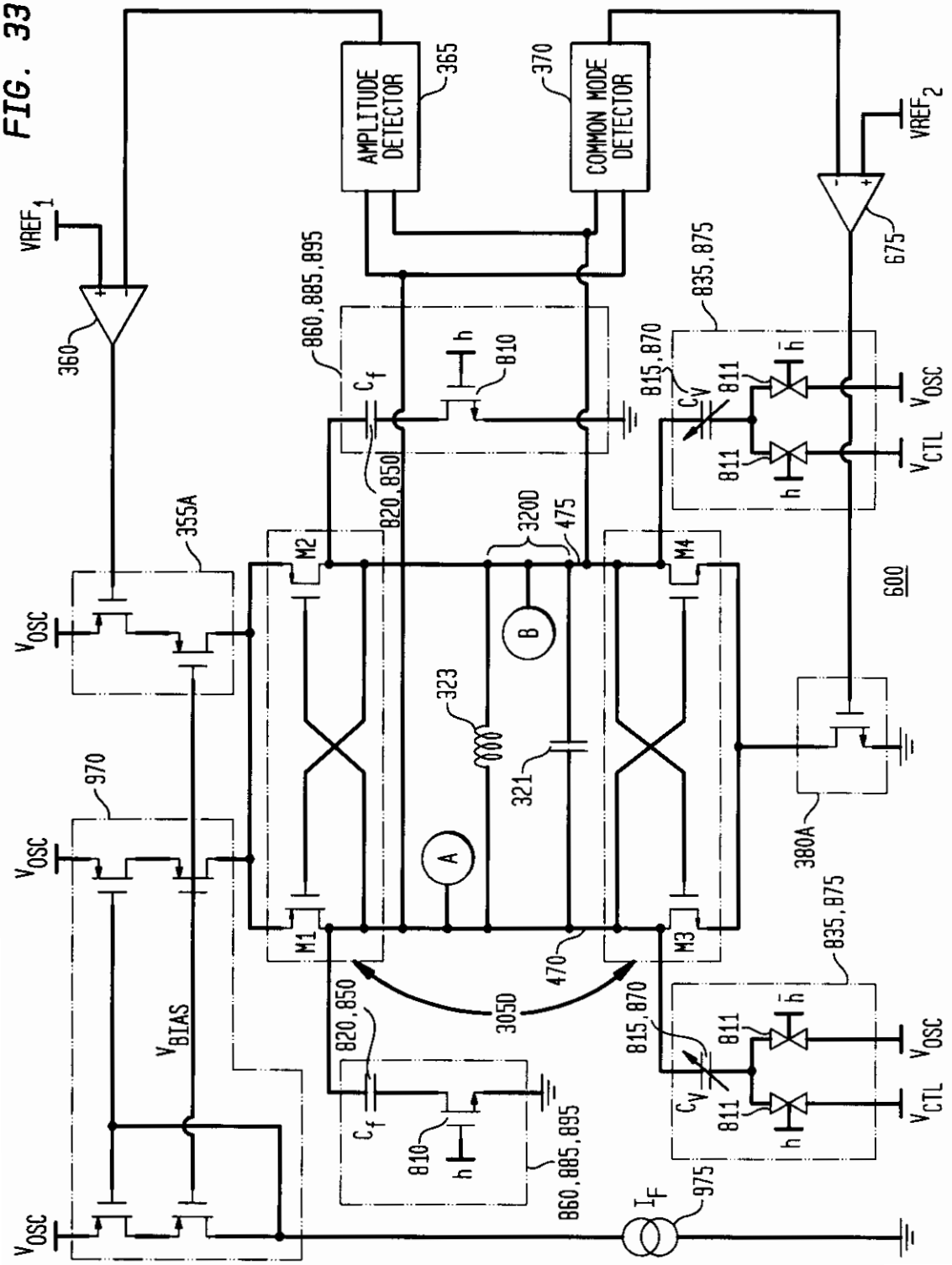

AMPLITUDE DETECTOR
365
COMMON MODE DETECTOR
370
VREF1
VREF2
360
675
860,885,895
835,875
815,870
820,850
810
811
355A
320D
475
M1
M2
M3
M4
600
323
321
A
B
970
380A
470
305D
VOSC
VCTL
VBIAS
IF
975

FIG. 34

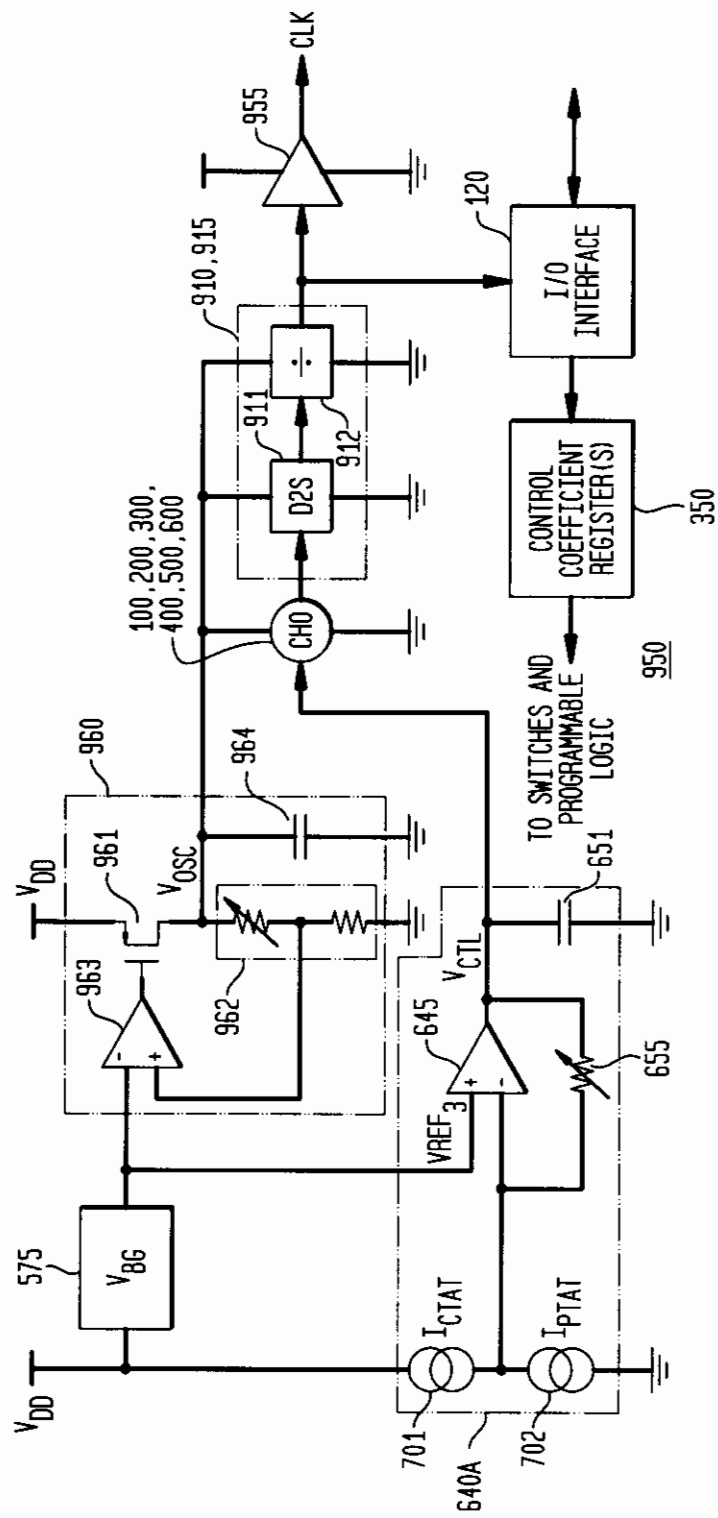
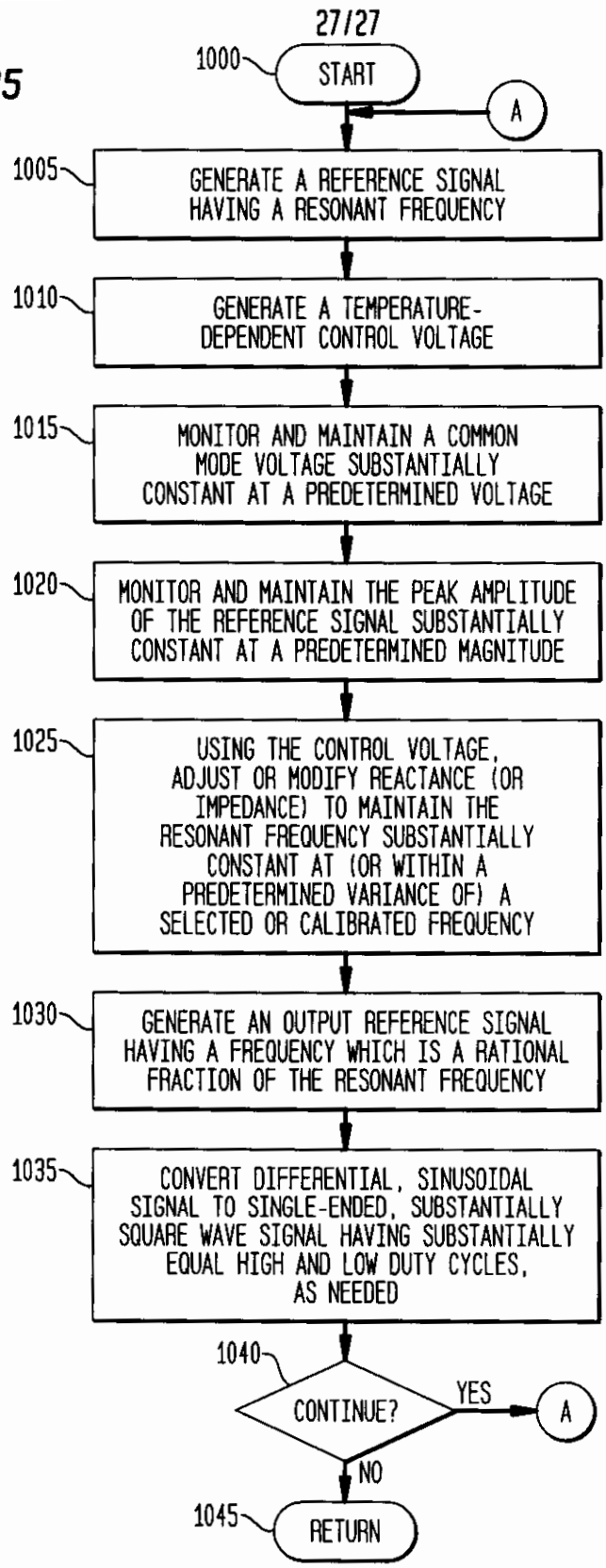

CLK
955
120
I/O INTERFACE
910,915
911
912
D2S
÷
100,200,300,
400,500,600
CH0
CONTROL COEFFICIENT REGISTER(S)
350
950
TO SWITCHES AND PROGRAMMABLE LOGIC
651
960
964
961
$V_{DD}$
$V_{OSC}$
963
962
$V_{CTL}$
645
655
$VREF_3$
575
$V_{BG}$
$I_{CTAT}$
$I_{PTAT}$
701
702
640A

FIG. 35


1000
START
A
1005
GENERATE A REFERENCE SIGNAL HAVING A RESONANT FREQUENCY
1010
GENERATE A TEMPERATURE-DEPENDENT CONTROL VOLTAGE
1015
MONITOR AND MAINTAIN A COMMON MODE VOLTAGE SUBSTANTIALLY CONSTANT AT A PREDETERMINED VOLTAGE
1020
MONITOR AND MAINTAIN THE PEAK AMPLITUDE OF THE REFERENCE SIGNAL SUBSTANTIALLY CONSTANT AT A PREDETERMINED MAGNITUDE
1025
USING THE CONTROL VOLTAGE, ADJUST OR MODIFY REACTANCE (OR IMPEDANCE) TO MAINTAIN THE RESONANT FREQUENCY SUBSTANTIALLY CONSTANT AT (OR WITHIN A PREDETERMINED VARIANCE OF) A SELECTED OR CALIBRATED FREQUENCY
1030
GENERATE AN OUTPUT REFERENCE SIGNAL HAVING A FREQUENCY WHICH IS A RATIONAL FRACTION OF THE RESONANT FREQUENCY
1035
CONVERT DIFFERENTIAL, SINUSOIDAL SIGNAL TO SINGLE-ENDED, SUBSTANTIALLY SQUARE WAVE SIGNAL HAVING SUBSTANTIALLY EQUAL HIGH AND LOW DUTY CYCLES, AS NEEDED
1040
CONTINUE?
YES
A
NO
1045
RETURN