A SEMICONDUCTOR DEVICE HAVING A NICKEL/COBALT SILICIDE REGION FORMED IN A SILICON REGION

FIELD OF THE PRESENT INVENTION

Generally, the present invention relates to the fabrication of integrated circuits and more particularly to the formation of metal silicide regions on silicon containing conductive circuit elements to decrease a sheet resistance thereof.

DESCRIPTION OF THE PRIOR ART

In modern ultrahigh density integrated circuits, device features are steadily decreasing to enhance device performance and functionality of the circuit. Shrinking the feature sizes, however, entails certain problems that may partially offset the advantages obtained by reducing the feature sizes. Generally, reducing the size of, for example, a transistor element such as a MOS transistor, may lead to superior performance characteristics due to a decreased channel length of the transistor element, resulting in a higher drive current capability and enhanced switching speed. Upon decreasing the channel length of the transistor elements, however, the electrical resistance of conductive lines and contact regions, i.e. of regions that provide electrical contact to the periphery of the transistor elements, becomes a major issue since the cross-sectional area of these lines and regions is also reduced. The cross-sectional area, however, determines in combination with the characteristics of the material comprising the conductive lines and contact regions the effective electrical resistance thereof.

Moreover, a higher number of circuit elements per unit area also requires an increased number of interconnections between these circuit elements, wherein commonly the number of required interconnects increases in a non-linear manner with the number of circuit elements so that the available real estate for interconnects becomes even more limited.

The majority of integrated circuits are based on silicon, that is, most of the circuit elements contain silicon regions, in crystalline, polycrystalline and amorphous form, doped and undoped, which act as conductive areas. An illustrative example in this context is a gate electrode of a MOS transistor element, which may be considered as a polysilicon line. Upon application of an appropriate control voltage to the gate electrode, a conductive channel is formed at the interface of a thin gate insulation layer and an active region of the semiconducting substrate. Although reducing the feature size of a transistor element improves device performance due to the reduced channel length, the shrinkage of the gate electrode (in the gate length direction), however, may result in significant delays in the signal propagation along the gate electrode, i.e. the formation of the channel along the entire extension (in the gate width direction) of the gate electrode. The issue of signal propagation delay

is even exacerbated for moderately elongated polysilicon lines connecting individual circuit elements or different chip regions. Therefore, it is extremely important to improve the sheet resistance of polysilicon lines and other silicon containing contact regions to allow further device scaling without compromising device performance. For this reason, it has become standard practice to reduce the sheet resistance of polysilicon lines and silicon contact regions by forming a metal silicide in and on appropriate portions of the respective silicon-containing regions.

With reference to Figs. 1a – 1d, a typical prior art process flow for forming metal silicide on a corresponding portion of a MOS transistor element will now be described as an illustrative example for demonstrating the reduction of the sheet resistance of silicon.

Fig. 1a schematically shows a cross-sectional view of a transistor element 100, such as a MOS transistor that is formed on a substrate 101 including a silicon-containing active region 102. The active region 102 is enclosed by an isolation structure 103, which in the present example is provided in the form of a shallow trench isolation usually used for sophisticated integrated circuits. Highly doped source and drain regions 104 including extension regions 105 are formed in the active region 102. The source and drain regions 104 including the extension regions 105 are laterally separated by a channel region 106. A gate insulation layer 107 electrically and physically isolates a gate electrode 108 from the underlying channel region 106. Spacer elements 109 are formed on sidewalls of the gate electrode 108. A refractory metal layer 110 is formed over the transistor element 100 with a thickness required for the further processing in forming metal silicide portions.

A typical conventional process flow for forming the transistor element 100, as shown in Fig. 1a, may include the following steps. After defining the active region 102 by forming the shallow trench isolations 103 by means of advanced photolithography and etch techniques, well established and well known implantation steps are carried out to create a desired dopant profile in the active region 102 and the channel region 106.

Subsequently, the gate insulation layer 107 and the gate electrode 108 are formed by sophisticated deposition, photolithography and anisotropic etch techniques to obtain a desired gate length, which is the horizontal extension of the gate electrode 108 i.e., in the plane of the drawing of Fig. 1a, as indicated by the double arrow 150. Thereafter, a first implant sequence may be carried out to form the extension regions 105 wherein, depending on design requirements, additional so-called halo implants may be performed.

Next, the spacer elements 109 are formed by depositing a dielectric material, such as silicon dioxide and/or silicon nitride and patterning the dielectric material by an anisotropic etch process. Thereafter, a further implant process may be carried out to form the source and drain regions 104, followed by anneal cycles to activate the dopants and at least partially cure lattice damage created during the implantation cycles.

Subsequently, the refractory metal layer 110 is deposited on the transistor element 100 by, for example, chemical vapor deposition (CVD) or physical vapor deposition (PVD). Preferably a refractory metal such as titanium, cobalt, nickel and the like is used for the metal layer 110. It turns out, however, that the characteristics of the various refractory metals during the formation of a metal silicide and afterwards in the form of a metal silicide significantly differ from each other. Consequently, selecting an appropriate metal depends on further design parameters of the transistor element 100 as well as on process requirements in following processes. For instance, titanium is frequently used for forming a metal silicide on the respective silicon containing portions. However, the electrical properties of the resulting titanium silicide strongly depend on the dimensions of the transistor element 100. Titanium silicide tends to agglomerate at grain boundaries of polysilicon and therefore may increase the total electrical resistance, wherein this effect is pronounced with decreasing feature sizes so that the use of titanium may not be acceptable for polysilicon lines, such as the gate electrode 108 having a lateral dimension, i.e. a gate length, of 0.2 micrometers and less.

For circuit elements having feature sizes of this order of magnitude, preferably cobalt is used as a refractory metal, since cobalt does substantially not exhibit a tendency for blocking grain boundaries of the polysilicon. However, cobalt silicide may show a significant deterioration in view of its sheet resistance for extremely scaled devices as will be explained in more detail later on. Another candidate that is frequently used in forming a metal silicide is nickel, which, however, may result in a degraded contact resistance in combination with local interconnects. In order to discuss the characteristics of cobalt that has superior contact characteristics and is therefore currently the preferred material for silicides, it is now assumed that the metal layer 110 is comprised of cobalt so as to allow the formation of the transistor element 100 as a sophisticated device having a gate length much less than 0.2μm.

A first anneal cycle is performed to initiate a reaction between the cobalt in the layer 110 and the silicon in the drain and source regions 104 and the polysilicon in the gate electrode 108. Optionally, a titanium nitride layer having a thickness in the range of approximately 10nm to 20 nm may be deposited above the refractory metal layer 110 prior to annealing the substrate 101 to decrease the finally obtained sheet resistance of the cobalt disilicide by reducing an oxidation of cobalt in the subsequent anneal cycles. Typically, the anneal temperature may range from approximately 450°C to 550°C to produce cobalt monosilicide. Thereafter, non-reacted cobalt is selectively etched away and then a second anneal cycle is performed with a higher temperature of approximately 700°C to convert cobalt monosilicide into low-ohmic phase comprised of cobalt disilicide

Fig. 1b schematically shows the transistor element 100 with cobalt disilicide regions 111 formed on the drain and source region 104 and a cobalt disilicide region 112 on the gate electrode 108. Although cobalt may successfully be used for feature sizes of approximately 0.2 micrometers and even less, it turns out that for further device scaling, requiring a gate length of well less than 100nm, the sheet resistance of the cobalt disilicide enhanced gate electrode 108 increases more rapidly than would be expected by merely taking into account the reduced feature size of the gate

electrode 108. It is believed that the increase of the resistivity of the region 112 is caused by tensile stress between individual cobalt disilicide grains, thereby significantly affecting the film integrity of the cobalt disilicide when the gate length is of the order of magnitude of a single grain.

Fig. 1c schematically shows the transistor element 100 with a reduced gate length 150A of approximately 50 to 80 nm after completion of the above-described silicide formation process. Irregularities 112A in the form of for instance voids and interruptions in the cobalt disilicide region 112 of the gate electrode 108 may occur and cause a significantly increase of the sheet resistance.

Fig. 1d and 1e schematically represent a top view of the gate electrodes 108 having a gate length 150 of approximately 200nm compared to the gate length 150A of approximately 50nm. Fig. 1d depicts the gate electrode 108 with the gate length 150, containing a plurality of single grains 113 arranged along the length 150, whereas, as is shown in Fig. 1e, only one single grain 113 is formed across the length 150A. While the thermal stress induced during the second anneal cycle in converting cobalt monosilicide into cobalt disilicide may be compensated for by the plurality of grains across the length 150, the single grain formed across the length 150A may not allow efficient absorption of the stress and may cause the interruption 112A of the cobalt disilicide film. As a consequence, the sheet resistance of the polysilicon gate electrode is drastically increased, thereby preventing aggressive device scaling without unduly degrading the transistor performance.

In view of the above-explained problems, therefore, a need exists for an improved silicide formation technique, enabling further device scaling while not unduly compromising production yield.

SUMMARY OF THE INVENTION

Generally, the present invention is directed to a technique that enables to combine the advantages of a nickel silicide, i.e., a superior behavior in combination with an underlying silicon, and the superior contact characteristics of cobalt silicide so as to provide the potential for further device scaling without unduly compromising the sheet resistance of a silicon feature including a metal silicide region. To this end, a layer of silicide that is substantially comprised of nickel silicide followed by a layer of metal silicide that is substantially comprised of cobalt silicide may be formed in a common formation process so that the problems occurring at a silicon cobalt silicide interface may be significantly reduced or even completely avoided.

According to one illustrative embodiment of the present invention, a method comprises forming a layer comprising metallic cobalt and metallic nickel over a silicon-containing region that is formed on a substrate. Thereafter, a heat treatment is performed with the substrate at a first temperature to allow nickel and cobalt to react with silicon to form a silicide in the silicon-containing region. Next, non-reacted nickel and cobalt are removed from the substrate and a further heat treatment is performed with the substrate at a second temperature that is higher than the first temperature to modify the silicide, which has formed during the heat treatment at the first temperature.

In a further embodiment the method further comprises controlling at least one of a temperature and a duration of the heat treatment for modifying the silicide to adjust an amount of cobalt disilicide in said silicon-containing region.

In a further embodiment said silicon containing region comprises a polysilicon line having a lateral dimension that is less than approximately 100 nanometers.

In a further embodiment said silicon containing region comprises a drain and a source region of a field effect transistor.

In a further embodiment said silicon containing region includes a first portion and a second portion and wherein the method further comprises forming a metal silicide over said first portion prior to forming said layer comprising metallic cobalt and metallic nickel.

In a further embodiment said first portion comprises a drain region and a source region of a field effect transistor.

In a further embodiment said second portion comprises a gate electrode of said field effect transistor covered by sidewall spacer elements and a cap layer and wherein said method further comprises removing said cap layer prior to forming said layer comprising metallic cobalt and metallic nickel.

In a further embodiment a gate length of said gate electrode is approximately 50 nanometer or less.

According to still a further illustrative embodiment of the present invention, a method of forming a field effect transistor comprises forming a polysilicon containing gate electrode on a gate insulation layer that is formed above a substrate. A drain region and a source region are formed in a silicon containing semiconductor region, wherein the drain and source regions are disposed adjacent to the gate electrode. Next, sidewall spacer elements are formed on sidewalls of the gate electrode and a layer comprising metallic cobalt and metallic nickel is formed over the gate electrode and the drain and source regions. Additionally, by means of said layer comprising the metallic cobalt and the metallic nickel, a region containing cobalt silicide and nickel silicide is formed at least in the gate electrode.

In a further embodiment said layer comprising metallic cobalt and metallic nickel is formed by depositing a first layer comprising metallic cobalt over said gate electrode and said drain and source regions and depositing a second layer comprising metallic nickel above said first layer.
In a further embodiment said layer comprising metallic cobalt and metallic nickel is formed by depositing a first layer comprising metallic nickel over said gate electrode and said drain and source regions and depositing a second layer comprising metallic cobalt above said first layer.

In accordance with yet another illustrative embodiment of the present invention a method of forming a field effect transistor comprises forming a layer stack, which includes at least a gate insulation layer, a polysilicon layer, and a cap layer, above a silicon region formed on a substrate. The layer stack is patterned so as to form a gate electrode having a top surface that is covered by at least the cap layer. Moreover, a drain region and a source region are formed adjacent to the gate electrode and silicide regions comprising a first metal are formed in the drain and source regions. Furthermore, the top surface of the gate electrode is exposed and a nickel silicide/cobalt silicide layer stack region is formed in the gate electrode.

In a further embodiment forming nickel silicide/cobalt silicide layer stack region includes forming a layer comprising metallic cobalt and metallic nickel; heat treating said substrate at a first temperature to allow nickel and cobalt to react with silicon to form a silicide in said gate electrode; selectively removing non-reacted nickel and cobalt from said substrate; and heat treating said substrate at a second temperature higher than said first temperature to modify said silicide formed during said heat treating at the first temperature.

In a further embodiment said layer comprising metallic cobalt and metallic nickel is formed by depositing a first layer comprising metallic cobalt over said gate electrode and depositing a second layer comprising metallic nickel above said first layer.

In a further embodiment said layer comprising metallic cobalt and metallic nickel is formed by depositing a first layer comprising metallic nickel over said gate electrode and depositing a second layer comprising metallic cobalt above said first layer.
In a further embodiment said first metal is comprised of cobalt.

According to another illustrative embodiment of the present invention, a field effect transistor comprises a silicon gate electrode formed on a gate insulation layer. The transistor further comprises a drain region and a source region formed adjacent to the gate electrode. Additionally, a nickel silicide region is formed on the silicon gate electrode and a cobalt silicide region is formed above the nickel silicide region.

In a further embodiment the field effect transistor further comprises a cobalt silicide region formed in said drain and source regions.

In a further embodiment the field effect transistor further comprises in said drain and source regions a second cobalt silicide region that is formed above a second nickel silicide region.

In a further embodiment a thickness of said nickel silicide region is less than a thickness of said cobalt silicide region.

BRIEF DESCRIPTION OF THE DRAWINGS

Further advantages, objects and embodiments of the present invention are defined in the appended claims and will become more apparent with the following detailed description when taken with reference to the accompanying drawings, in which:

Figs. 1a, 1b and 1c schematically show cross-sectional views of a conventional field effect transistor during different stages of manufacture;

Figs. 1d and 1e schematically show top views of gate electrodes of different gate length, wherein an unduly increased gate resistance may be observed at a gate length of less than 100 nm; and

Figs 2a-2d schematically show cross-sectional views of a field effect transistor during varying manufacturing stages in accordance with illustrative embodiments of the present invention.

DETAILED DESCRIPTION

While the present invention is described with reference to the embodiments as illustrated in the following detailed description as well as in the drawings, it should be understood that the following detailed description as well as the drawings are not intended to limit the present invention to the particular illustrative embodiments disclosed, but rather the described illustrative embodiments merely exemplify the various aspects of the present invention, the scope of which is defined by the appended claims.

It should be noted that the present invention is particularly advantageous when applied to the formation of field effect transistors of extremely reduced feature sizes, as the issues [problems? concerns?] associated with cobalt silicide at feature sizes of well below 100nm may significantly be reduced or avoided by providing a stacked nickel silicide/cobalt silicide region. The nickel silicide formed adjacent to the silicon allows a reduction of line width without unduly compromising the silicide film characteristics, whereas cobalt silicide is an approved and well-established silicide material providing superior contact resistance to other contact materials such as tungsten and the like, thereby providing a high degree of compatibility with standard CMOS process techniques. However, the present invention should not be considered as being restricted to critical dimensions of 100nm and less unless such restrictions are explicitly set forth in the appended claims.

With reference to Figs. 2a-2d, further illustrative embodiments of the present invention will now be described in more detail.

In Fig. 2a a field effect transistor 200 is illustrated so as to represent any silicon-containing region which is intended to receive a silicide portion so as to reduce the sheet resistance thereof. As previously explained, gate electrodes, drain and source regions, polysilicon lines and the like need

to be modified in terms of their conductivity, especially as the critical dimensions of these silicon features are steadily reduced to a size of currently 50nm and even less. Unless otherwise specified in the appended claims, the field effect transistor 200 is to be considered as a representative of any silicon containing circuit feature requiring the formation therein of a metal silicide region. The field effect transistor 200 comprises a substrate 201, which may be any appropriate substrate, such as a silicon wafer, an SOI (silicon on insulator) substrate, and the like. A transistor active region 202 is formed in the substrate 201 and the dimensions thereof are defined by an isolation structure 203, which may be provided in the form of a trench isolation structure. Highly doped drain and source regions 204 including respective extension regions 205 are formed in the active region 202 and are separated from each other by a channel region 206. A polysilicon gate electrode 208 is formed above the channel region 206 and is separated therefrom by a gate insulation layer 207. Moreover, sidewall spacer elements 209 are formed on sidewalls of the polysilicon gate electrode 208. In one embodiment, as shown in Fig. 2a, a cap layer 230 may be located above the gate electrode 208 so as to cover a top surface of the gate electrode 208. The cap layer 230 may be comprised of silicon nitride, silicon dioxide, silicon oxynitride, and the like, and may advantageously be comprised of a material exhibiting optical characteristics that enable the cap layer 230 to be used as a bottom anti-reflective coating during the patterning of the gate electrode 208.

A typical process flow for forming the field effect transistor 200 as shown in Fig. 208 may comprise substantially the same process as previously described with reference to Fig. 1a. Regarding the embodiment of the field effect transistor 200 including the cap layer 230, it is to be noted that during the patterning of the gate electrode 208 by means of sophisticated photolithography a bottom anti-reflective coating is used that is typically removed after the patterning process. In some embodiments of the present invention, contrary to the conventional process flow the bottom anti-reflective coating may be preserved as the cap layer 230. The cap layer 230 provides the possibility to independently form metal silicide regions in the drain and source regions 204 on the one hand and, after completion of the metal silicides in the drain and source regions 204 in the gate electrode 208, on the other hand by subsequently removing the cap layer 230 and performing a process sequence as will be described with reference to Figs. 2b-2d. That is, in some embodiments, for instance, a cobalt silicide region may be formed in the drain and source regions 204, wherein substantially the same process sequence may be performed as is previously described with reference to Figs. 1a-1c, wherein, however, the cap layer 230 prevents a formation of cobalt silicide in the gate electrode 208. Thus, applying the process sequence described in Figs. 1a-1c to the field effect transistor 200 having the cap layer 230 results in the formation of cobalt silicide regions 211a, indicated by dashed lines. Thereafter, the cap layer 230 may be removed for forming a nickel silicide/cobalt silicide region in the gate electrode 208. For convenience, in the further description it is now referred to the field effect transistor 200 lacking the cap layer 230, since essentially the same process steps may be applied to the transistor 200 as shown in Fig. 2a, thereby forming a nickel silicide/cobalt silicide region in the gate electrode 208 only.

Fig. 2b schematically shows the field effect transistor 200 with a metal layer 240 formed thereon, wherein the metal layer 240 comprises metallic cobalt and metallic nickel. In one particular embodiment, the metal layer 240 may comprise a first sublayer 241 and a second sublayer 242, wherein the first sublayer 241 comprises cobalt and the second sublayer 242 comprises nickel. In other embodiments, the first sublayer 241 may be comprised of nickel and the second sublayer 242 may be comprised of cobalt. In one illustrative embodiment, the metal layer 240 may be provided as a substantially continuous layer comprised of a mixture of metallic cobalt and metallic nickel.

The metal layer 240 may be formed by chemical vapor deposition and/or physical vapor deposition. For instance, when the metal layer 240 comprises at least the two sublayers 241, 242, these sublayers may be individually deposited by a specific deposition process, such as a CVD process or a PVD process. In other embodiments, when the metal layer 240 is provided in the form of a mixture of metallic cobalt and metallic nickel, a common deposition process may be performed, for instance by commonly sputtering cobalt and nickel onto the field effect transistor 200. During the deposition process, irrespective of the type of deposition process, the ratio of cobalt to nickel may be controlled, for instance by controlling the layer thicknesses of the sublayers 241 and 242, or by controlling sputter process parameters when cobalt and nickel are deposited in a common process. In one particular embodiment, the deposition process is controlled such that the amount of cobalt, in terms of volume percentages, is higher than the amount of nickel. For instance, to this end, in one embodiment the respective sublayer 241, 242 including the cobalt may be selected [to be?] greater than the corresponding thickness of the other sublayer 241, 242, including the metallic nickel. For example, a thickness of the sublayer 241, for instance comprised of cobalt, may be selected in a range of approximately 10-50nm, whereas the thickness of the sublayer 242 may be selected in a range of approximately 10-30nm. If, however, other ratios and/or layer thicknesses of the finally obtained nickel silicide and cobalt silicide are required, the corresponding thicknesses of the sublayers 241, 242 may correspondingly be adapted. The same holds true for the case when the metal layer 240 is provided in a substantially continuous manner, wherein the ratio of cobalt and nickel and the thickness of the continuous layer 240 determine the finally obtained nickel silicide and cobalt silicide thicknesses and their ratio.

Thereafter, a heat treatment is performed, such as a rapid thermal annealing, at moderately low temperatures compared to a conventional cobalt silicidation process, as is described with reference to Fig. 1a. For instance, a temperature in the range of approximately 300°C-308°C may be applied for a time interval of approximately 20-60 seconds so as to initiate metal diffusion and the formation of silicides with the underlying silicon. In one particular embodiment, an arrangement with the first sublayer 241 comprised of cobalt and the second sublayer 242 comprised of nickel surprisingly results in the formation of nickel silicide immediately on the underlying silicon, for instance, on the silicon gate electrode 208 and the drain and source regions 204, unless not covered by the previously formed metal silicide 211a (cf. Fig. 2a). Without restricting the present invention to the following explanation, it is believed that the moderate temperature during the heat treatment creates a significantly higher diffusion activity of the nickel compared to the cobalt so that at an

initial phase nickel penetrates into the cobalt, while the reduced temperature significantly slows down a reaction of cobalt with the underlying silicon. During the progress of the heat treatment, nickel increasingly diffuses into silicon and readily forms silicon silicide while the cobalt silicide formation is still significantly lower. Finally, a nickel silicide layer is formed on the underlying silicon, such as the gate electrode 208 and the drain and source regions 204, followed by a cobalt silicide layer.

Fig. 2c schematically shows the field effect transistor 200 after completion of the heat treatment as described above, thereby forming a nickel silicide layer 260 and above thereof a cobalt silicide layer 261. Similarly, a nickel silicide layer 270 may be formed in the drain and source regions 204 followed by a cobalt silicide layer 271. In case the field effect transistor comprises a metal silicide region 211a, for example in the form of a cobalt silicide, the formation of the nickel silicide layer 271 and of the cobalt silicide layer 270 may substantially be avoided or at least significantly be reduced so that in this case the formation process for the nickel silicide 260 and the cobalt silicide 261 in the gate electrode 208 may be specifically tailored so as to meet the requirements especially for an optimum conductivity of the gate electrode 208. On the other hand, when the metal silicide regions 211a (cf. Fig. 2a) have previously been formed by means of the cap layer 230, the process parameters involved in forming the metal silicide regions 211a may be specifically designed so as to optimize these regions in view of junction depth and the like. After the completion of the heat treatment for forming the silicide layers 260, 261, 270, 271, any non-reacted metal may be removed from the sidewall spacers 209 and the isolation structure 203 by a selective wet chemical etch process, as is well established in the art.

Thereafter, a second heat treatment is formed, for instance, in the form of a rapid thermal annealing, at a temperature that is higher than the temperature of the previous heat treatment. In some embodiments, the temperature is selected in a range of approximately 450°C-650°C, whereas in other embodiments the temperature range is selected from approximately 500°C-600°C. Moreover, the duration of the heat treatment is selected to approximately 10-60 seconds. During this heat treatment, the conversion of the cobalt silicide in the regions 261 and 271 into a low ohmic cobalt disilicide is initiated. During this heat treatment, the nickel silicide may also be converted into a nickel disilicide which exhibits excellent interface characteristics with the underlying silicon and acts thereby as a "buffer" to the overlying cobalt disilicide, in this way significantly reducing or eliminating stress-induced irregularities of the cobalt disilicide layer when the gate length of the gate electrode 208 is of the order of magnitude of a single grain of cobalt disilicide, as previously explained with reference to Figs. 1c, 1d and 1e. By controlling at least one process parameter of the heat treatment, that is, the temperature and the duration, the process of transforming the monosilicides into disilicides may be adjusted. For instance, in view of the desired low sheet resistance, an optimum of the finally obtained conductivity may be determined on the basis of experiments, wherein for a given thickness ratio of the nickel silicide layer 260 and the cobalt silicide layer 261 at least one process parameter of the heat treatment may be varied to identify the dependency of the finally obtained sheet resistance on this process parameter. These

measurements may be performed for a plurality of different thickness ratios so as to establish a plurality of measurement data from which the process parameters of the heat treatment may be derived. A corresponding control of the heat treatment may be necessary since nickel disilicide may exhibit an increased resistance compared to nickel monosilicide, whereas cobalt silicide shows the opposite behavior.

Fig. 2d schematically shows the field effect transistor 200 after completion of the second heat treatment with a modified nickel silicide layer 260a, followed by a modified cobalt silicide layer 261a formed in the gate electrode 208, and with a modified nickel silicide layer 270a and a modified cobalt silicide layer 271a formed in the drain and source regions 204, unless these regions are not covered by the previously formed metal silicide region 211a (cf. Fig. 2a). Due to the combination of the superior characteristics of cobalt silicide in view of its resistance to a contact metal and the characteristics of nickel silicide with respect to an interface with an underlying silicon, a low overall sheet resistance may be obtained for the gate electrode 208, while at the same time the resistivity to local interconnects (not shown) formed during a further manufacturing step for the field effect transistor 200 is also maintained at a low level.

As a result, the present invention provides a technique that enables the formation of a buried nickel silicide layer on silicon containing circuit features with a cobalt silicide layer formed on the buried nickel silicide layer, thereby preserving the excellent characteristics of cobalt silicide with respect to contact resistance, while significantly reducing or avoiding sheet resistant degradation caused by a cobalt silicide/silicon interface. The cobalt silicide layer and the buried nickel silicide layer may be formed in a common formation process, wherein the characteristics such as the thickness of the individual silicide layers, the overall sheet resistance, and the morphology of the layers may be controlled by deposition parameters, such as layer thickness and composition ratio, and by the process parameters of a heat treatment, respectively. Surprisingly, the formation of a cobalt layer followed by a nickel layer leads to a redistribution of these materials during the formation of respective silicides, so that in some embodiments undesired nickel diffusion during the silicidation process may be reduced.

Further modifications and variations of the present invention will be apparent to those skilled in the art in view of this description. Accordingly, the description is to be construed as illustrative only and is for the purpose of teaching those skilled in the art the general manner of carrying out the present invention. It is to be understood that the forms of the invention shown and described herein are to be taken as the presently preferred embodiments.

Industrial applicability

The present invention relates to devices and fabrication methods of microelectronic components and therefore meets the requirement of industrial applicability.

CLAIMS

1. A method comprising:

forming a layer (240) comprising metallic cobalt (241) and metallic nickel (242) over a silicon-containing region (202, 208) formed on a substrate (201);

heat treating said substrate (201) at a first temperature to allow nickel (242) and cobalt (241) to react with silicon to form a silicide (260, 261, 270, 271) in said silicon containing region (208, 202);

selectively removing non-reacted nickel and cobalt from said substrate (201), and

heat treating said substrate (201) at a second temperature higher than said first temperature to modify said silicide formed during said heat treating at the first temperature.

2. The method of claim 1, wherein said layer comprising metallic cobalt and metallic nickel is formed by depositing a layer of metallic cobalt above said silicon containing region and depositing a layer of metallic nickel above said layer of metallic cobalt.

3. The method of claim 1, wherein said layer comprising metallic cobalt and metallic nickel is formed by depositing a layer of metallic nickel above said silicon containing region and depositing a layer of metallic cobalt above said layer of metallic cobalt.

4. The method of claim 1, further controlling a thickness of modified silicide formed in said silicon containing region by adjusting a thickness of said layer. .

5. The method of claim 4, wherein the thickness of said layer is adjusted by depositing a first layer comprised of metallic cobalt with a predefined first thickness and a second layer comprised of metallic nickel with a predefined second thickness.

6. The method of claim 5, wherein said second thickness is less than said first thickness.

7. A method of forming a field effect transistor, the method comprising:

forming a polysilicon containing gate electrode (208) on a gate insulation layer (207) formed above a substrate (201);

forming a drain region (204) and a source region (204) in a silicon-containing semiconductor area (202), the drain and source regions (204) being disposed adjacent to the gate electrode (208);

forming sidewall spacer elements (209) on sidewalls of said gate electrode (208);

forming a layer (240) comprising metallic cobalt (241) and metallic nickel (242) over said gate electrode (208) and said drain and source regions (204); and

forming with said layer (240) a cobalt silicide (261, 261a) and nickel silicide-containing region (260, 260a) at least in said gate electrode.

8. The method of claim 7, wherein forming said cobalt silicide and nickel silicide containing region includes heat-treating said substrate at a first temperature to allow nickel and cobalt to react with silicon to form a silicide at least in said gate electrode;

selectively removing non-reacted nickel and cobalt from said substrate, and

Heat-treating said substrate at a second temperature higher than said first temperature to modify said silicide formed during said heat-treating at the first temperature.

9. A method of forming a field effect transistor, the method comprising:

forming a layer stack including at least a gate insulation layer (209), a polysilicon layer and a cap layer (230) above a silicon region (202) formed on a substrate (201);

patterning said layer stack to form a gate electrode (208) having a top surface covered by at least said cap layer (230);

forming a drain and a source region (204) adjacent to said gate electrode (208);

forming silicide regions (270) comprising a first metal in the drain and source regions (204);

exposing said top surface of the gate electrode (208); and

forming a nickel silicide/cobalt silicide layer stack region (260, 261) in said gate electrode (208).

10. A field effect transistor comprising:

a silicon gate electrode (208) formed on a gate insulation layer (209);

a drain region (204) and a source region (204) formed adjacent to said gate electrode (208);

a nickel silicide region (260a) formed on said silicon gate electrode (208);

and

a cobalt silicide region (261a) formed above said nickel silicide region (260a).

5