

SEMICONDUCTOR CHIP

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This patent application is based on and claims priority to Korean Patent Application No. 10-2024-0181964, filed on 09 December 2024, in the Korean Intellectual Property Office, the disclosure of which is incorporated by reference herein in its entirety.

TECHNICAL FIELD

[0002] The inventive concept relates to a semiconductor chip, and more particularly, to a semiconductor chip including a through-silicon via.

BACKGROUND

[0003] Recently, with the active development of three-dimensional (3D) semiconductor packages, in which a plurality of semiconductor chips are mounted within a single semiconductor package, through-silicon vias are being utilized to establish vertical electrical connections through substrates or dies. Accordingly, there is a need for technologies capable of increasing the degree of integration of semiconductor chips while ensuring electrical reliability of connection structures between the plurality of semiconductor chips.

SUMMARY

[0004] The inventive concept provides a semiconductor chip, wherein, in a bonding structure of a memory cell structure and a peripheral circuit structure, a degree of integration of the semiconductor chip may be improved by reducing an area of a keep out zone in which through-vias are arranged, while securing electrical reliability of a connection structure.

[0005] The objects of the inventive concept are not limited to the object mentioned above, but other objects not described herein will be clearly understood by those skilled in the art from the following description.

[0006] According to an aspect of the inventive concept, there is provided a semiconductor chip including a memory cell structure and a peripheral circuit structure disposed on the memory cell structure, wherein the memory cell structure includes a memory cell substrate, a memory

cell layer disposed on the memory cell substrate, a memory cell wiring layer electrically connected to the memory cell layer, a memory cell insulating layer covering the memory cell layer and the memory cell wiring layer, on the memory cell substrate, and a first through-via passing through the memory cell insulating layer and the memory cell substrate, and wherein the peripheral circuit structure includes a peripheral circuit substrate having a first trench isolation layer, a peripheral circuit layer disposed on the peripheral circuit substrate, a first peripheral circuit wiring layer electrically connected to the peripheral circuit layer, a first peripheral circuit insulating layer covering the peripheral circuit layer and the first peripheral circuit wiring layer, on the peripheral circuit substrate, and a second through-via passing through the first peripheral circuit insulating layer and the first trench isolation layer and being in contact with the first through-via, wherein a first width of the first through-via in a horizontal direction is greater than a second width of the second through-via in the horizontal direction, and a first length of the first through-via in a vertical direction is greater than a second length of the second through-via in the vertical direction.

[0007] According to another aspect of the inventive concept, there is provided a semiconductor chip including a memory cell structure and a peripheral circuit structure disposed on the memory cell structure, wherein the memory cell structure includes a memory cell substrate, a memory cell layer disposed on the memory cell substrate, a memory cell wiring layer electrically connected to the memory cell layer, a memory cell insulating layer covering the memory cell layer and the memory cell wiring layer, on the memory cell substrate, and a first through-via passing through the memory cell insulating layer and the memory cell substrate, and wherein the peripheral circuit structure includes a peripheral circuit substrate having a trench isolation layer, a peripheral circuit layer disposed on the peripheral circuit substrate, a peripheral circuit wiring layer electrically connected to the peripheral circuit layer, a peripheral circuit insulating layer covering the peripheral circuit layer and the peripheral circuit wiring layer, on the peripheral circuit substrate, and a plurality of second through-vias passing through the peripheral circuit insulating layer and the trench isolation layer, wherein lower surfaces of the plurality of second through-vias are in contact with an upper surface of the first through-via, and a first width of the first through-via in a horizontal direction is greater than a second width of each of the plurality of second through-vias in the horizontal direction.

[0008] According to another aspect of the inventive concept, there is provided a semiconductor chip including a memory cell structure and a peripheral circuit structure disposed on the memory cell structure, wherein the memory cell structure includes a memory cell substrate, a memory cell layer disposed on the memory cell substrate, a memory cell wiring layer

electrically connected to the memory cell layer, and a memory cell insulating layer covering the memory cell layer and the memory cell wiring layer, on the memory cell substrate, and wherein the peripheral circuit structure includes a peripheral circuit substrate having a trench isolation layer, a peripheral circuit layer disposed on the peripheral circuit substrate, a first peripheral circuit wiring layer electrically connected to the peripheral circuit layer, a first peripheral circuit insulating layer covering the peripheral circuit layer and the first peripheral circuit wiring layer, on the peripheral circuit substrate, a second peripheral circuit wiring layer electrically connected to the first peripheral circuit wiring layer, and a second peripheral circuit insulating layer covering the second peripheral circuit wiring layer, on the first peripheral circuit insulating layer, wherein the semiconductor chip further includes a through-via, and the through-via passes through the first peripheral circuit insulating layer, the trench isolation layer, the memory cell insulating layer, and the memory cell substrate, and is in contact with the second peripheral circuit wiring layer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] Embodiments will be more clearly understood from the following detailed description taken in conjunction with the accompanying drawings in which:

[0010] FIG. 1 is a cross-sectional view illustrating main components of a semiconductor chip according to an embodiment;

[0011] FIG. 2 is an enlarged view of region CX1 of FIG. 1;

[0012] FIG. 3 is an enlarged view of region CX2 of FIG. 1;

[0013] FIGS. 4 and 5 are cross-sectional views illustrating main components of semiconductor chips according to other embodiments;

[0014] FIGS. 6, 7, 8, 9, 10, 11, 12, 13, 14 and 15 are cross-sectional views showing a method of manufacturing a semiconductor chip in a process sequence, according to an embodiment;

[0015] FIGS. 16, 17 and 18 are cross-sectional views showing a method of manufacturing a semiconductor chip in a process sequence, according to another embodiment; and

[0016] FIGS. 19 and 20 are diagrams illustrating a semiconductor package including a semiconductor chip according to an embodiment.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0017] Hereinafter, an embodiment is described in detail with reference to the accompanying drawings.

[0018] FIG. 1 is a cross-sectional view illustrating main components of a semiconductor chip 10 according to an embodiment. FIG. 2 is an enlarged view of region CX1 of FIG. 1. FIG. 3 is an enlarged view of region CX2 of FIG. 1.

[0019] Referring to FIGS. 1 to 3 together, the semiconductor chip 10 according to the embodiment may include a peripheral circuit structure 100 and a memory cell structure 200.

[0020] The peripheral circuit structure 100 is stacked above the memory cell structure 200, and the peripheral circuit structure 100 and the memory cell structure 200 may be in contact with each other via a bonding interface BI.

[0021] The peripheral circuit structure 100 may include a core region or a peripheral circuit region of a dynamic random-access memory (DRAM) device, and the memory cell structure 200 may include an array region of a volatile memory cell of the DRAM device. For example, the peripheral circuit structure 100 may include a peripheral circuit transistor PT for transmitting signals and/or power to a memory cell transistor 300 in the memory cell structure 200.

[0022] First, the peripheral circuit structure 100 is described below.

[0023] The peripheral circuit structure 100 may include a first substrate 101 in which a first trench isolation layer 101LD and a second trench isolation layer 101SD are formed.

[0024] The first substrate 101 may include a wafer that contains silicon (Si). In some embodiments, the first substrate 101 may include a wafer that contains a semiconductor element, such as germanium (Ge), or a compound semiconductor, such as silicon carbide (SiC), gallium arsenide (GaAs), indium arsenide (InAs), and indium phosphide (InP). Also, the first substrate 101 may include a conductive region, for example, a well doped with impurities and a source/drain doped with impurities.

[0025] In the first substrate 101, an active region may be defined by the first trench isolation layer 101LD and the second trench isolation layer 101SD that are insulating regions. The width of the first trench isolation layer 101LD in the horizontal direction may be greater than the width of the second trench isolation layer 101SD in the horizontal direction. That is, the first trench isolation layer 101LD may be wide and the second trench isolation layer 101SD may be narrow. As described below, a second through-via TSV2 may pass through the first trench isolation layer 101LD having a large width.

[0026] In the peripheral circuit structure 100, a peripheral circuit layer CP may be disposed on the first substrate 101. The peripheral circuit layer CP may represent a region including a

peripheral circuit transistor PT. In some embodiments, the peripheral circuit layer CP may constitute various circuits, such as a command decoder, control logic, an address buffer, a row decoder, a column decoder, a sense amplifier, and a data input/output circuit.

[0027] The peripheral circuit transistor PT may include a gate dielectric layer and a gate electrode that are sequentially stacked on the active region. The gate dielectric layer may include at least one selected from a group consisting of silicon oxide, silicon nitride, silicon oxynitride, or a high-k dielectric material having a higher dielectric constant than the silicon oxide. The gate electrode may include doped polysilicon, TiN, TiSiN, W, tungsten silicide, or a combination thereof. In some embodiments, both sidewalls of the gate electrode may be covered with a gate spacer (not shown). The gate spacer may include, for example, silicon oxide, silicon nitride, or a combination thereof.

[0028] A first peripheral circuit connector 110 may be disposed on the peripheral circuit layer CP. The first peripheral circuit connector 110 may include a first peripheral circuit insulating layer 111 and a first peripheral circuit wiring layer 113. Specifically, the peripheral circuit transistor PT may be electrically connected to the first peripheral circuit wiring layer 113, and the first peripheral circuit insulating layer 111 may cover the peripheral circuit transistor PT and the first peripheral circuit wiring layer 113 on the first substrate 101. Also, the first peripheral circuit connector 110 may include a first contact via 115. This is described below in detail.

[0029] A second peripheral circuit connector 120 may be disposed on the first peripheral circuit connector 110. The second peripheral circuit connector 120 may include a second peripheral circuit insulating layer 121 and a second peripheral circuit wiring layer 123. Specifically, the first peripheral circuit wiring layer 113 may be electrically connected to the second peripheral circuit wiring layer 123, and the second peripheral circuit insulating layer 121 may cover the second peripheral circuit wiring layer 123 on the first peripheral circuit insulating layer 111.

[0030] A third peripheral circuit connector 130 may be disposed on the second peripheral circuit connector 120. The third peripheral circuit connector 130 may include a third peripheral circuit insulating layer 131 and a third peripheral circuit wiring layer 133. Specifically, the second peripheral circuit wiring layer 123 may be electrically connected to the third peripheral circuit wiring layer 133, and the third peripheral circuit insulating layer 131 may cover the third peripheral circuit wiring layer 133 on the second peripheral circuit insulating layer 121.

[0031] Here, the first peripheral circuit insulating layer 111, the second peripheral circuit insulating layer 121, and the third peripheral circuit insulating layer 131 may include, for example, silicon oxide, silicon nitride, or silicon oxynitride. Also, the first peripheral circuit

wiring layer 113, the first contact via 115, the second peripheral circuit wiring layer 123, and the third peripheral circuit wiring layer 133 may include, for example, a copper layer, an aluminum layer, or a tungsten layer.

[0032] Next, the memory cell structure 200 is described below.

[0033] In the memory cell structure 200, a memory cell layer MC may be disposed on a second substrate 201. The memory cell layer MC may include the memory cell transistor 300. Since materials constituting the second substrate 201 may be substantially the same as materials constituting the first substrate 101 described above, a detailed description thereof is omitted.

[0034] The memory cell transistor 300 may include a lower insulating layer 310, a first conductive line 320, a vertical channel layer 330, a gate electrode layer 340, a gate insulating layer 350, a capacitor contact 360, an upper insulating pattern 370, and a capacitor structure 380.

[0035] In the semiconductor chip 10 according to the inventive concept, the memory cell transistor 300 may represent a DRAM device including a vertical channel transistor. The vertical channel transistor may refer to a structure in which a length of a channel of the vertical channel layer 330 extends from the second substrate 201 in a vertical direction Z.

[0036] The memory cell transistor 300 may include the lower insulating layer 310, and a plurality of first conductive lines 320 on the lower insulating layer 310 may be spaced apart from each other in a first horizontal direction X and extend in a second horizontal direction Y. A plurality of first insulating patterns 322 may be arranged on the lower insulating layer 310 to fill spaces between the plurality of first conductive lines 320. The plurality of first conductive lines 320 may correspond to a bit line of the memory cell transistor 300. The plurality of first conductive lines 320 may include doped polysilicon, metal, conductive metal nitride, conductive metal silicide, conductive metal oxide, or a combination thereof.

[0037] The vertical channel layer 330 may be disposed on the plurality of first conductive lines 320 in an island form in which vertical channel layers 330 are spaced apart from each other in the first horizontal direction X and the second horizontal direction Y. The vertical channel layer 330 may have a width in the first horizontal direction X and a vertical length in the vertical direction Z, and the vertical length of the vertical channel layer 330 may be greater than the width of the vertical channel layer 330. A lower portion of the vertical channel layer 330 may function as a first source/drain region, and an upper portion of the vertical channel layer 330 may function as a second source/drain region. Also, a portion of the vertical channel layer 330 between the first and second source/drain regions may function as a channel region.

[0038] The gate electrode layer 340 may surround a sidewall of the vertical channel layer 330 and extend in the first horizontal direction X. In some embodiments, the gate electrode layer 340 may be of a gate all-around type in which the sidewall of the vertical channel layer 330 is completely surrounded. The gate electrode layer 340 may correspond to a word line of the memory cell transistor 300. The gate electrode layer 340 may include doped polysilicon, metal, conductive metal nitride, conductive metal silicide, conductive metal oxide, or a combination thereof.

[0039] The gate insulating layer 350 may surround the sidewall of the vertical channel layer 330 and be located between the vertical channel layer 330 and the gate electrode layer 340. In some embodiments, the gate insulating layer 350 may include silicon oxide, silicon oxynitride, a high-k dielectric material, or a combination thereof.

[0040] A first buried insulating layer 342 surrounding a lower portion of the sidewall of the vertical channel layer 330 may be disposed on the plurality of first insulating patterns 322, and a second buried insulating layer 344 surrounding the lower sidewall of the vertical channel layer 330 and covering the gate electrode layer 340 may be disposed above the first buried insulating layer 342.

[0041] The capacitor contact 360 may be disposed on the vertical channel layer 330. The capacitor contact 360 may overlap the vertical channel layer 330 in the vertical direction Z and be arranged in a matrix form in which capacitor contacts 360 are spaced apart from each other in the first horizontal direction X and the second horizontal direction Y. An upper insulating layer 362 may surround the sidewall of the capacitor contact 360 on the second buried insulating layer 344. The upper insulating pattern 370 may be disposed on the upper insulating layer 362, and the capacitor structure 380 may be disposed on the upper insulating pattern 370.

[0042] The capacitor structure 380 may include a plurality of lower electrodes 381, a capacitor dielectric layer 383, an upper electrode 385, and a metal plate layer 387. The capacitor structure 380 may face the upper surface of the second substrate 201. This may be a specific feature of the inventive concept according to a manufacturing process of the semiconductor chip 10, which is described below.

[0043] A plurality of metal contacts 390 may extend in the vertical direction Z through the interlayer insulating layer 391. A bottom portion of each of the plurality of metal contacts 390 may be in contact with and electrically connected to the metal plate layer 387. The plurality of metal contacts 390 may each include a conductive barrier layer 392 and a contact conductive layer 394.

[0044] A memory cell connector 210 may be disposed on the memory cell layer MC. The memory cell connector 210 may include a memory cell insulating layer 211 and a memory cell wiring layer 213. Specifically, the memory cell transistor 300 may be electrically connected to the memory cell wiring layer 213, and the memory cell insulating layer 211 may cover the memory cell transistor 300 and the memory cell wiring layer 213 on the second substrate 201.

[0045] In the semiconductor chip 10 according to the embodiment, the peripheral circuit structure 100 and the memory cell structure 200 may form a bonded structure. In some embodiments, a heat treatment process may be utilized to form a structure in which the peripheral circuit structure 100 is bonded to the memory cell structure 200. Here, the heat treatment process may be performed at a temperature that is sufficient to form bonding coupling between an insulating material of the peripheral circuit structure 100 and an insulating material of the memory cell structure 200. Accordingly, the bonding interface BI may be formed between the peripheral circuit structure 100 and the memory cell structure 200.

[0046] In the semiconductor chip 10 according to the embodiment, depending on the bonded structure of the peripheral circuit structure 100 and the memory cell structure 200, a conductive structure capable of electrically connecting the peripheral circuit structure 100 to the memory cell structure 200 is required. That is, the semiconductor chip 10 includes the first contact via 115 electrically connecting the peripheral circuit structure 100 to the memory cell structure 200.

[0047] The first contact via 115 may be provided as part of the first peripheral circuit wiring layer 113 and electrically connect the first peripheral circuit wiring layer 113 to the memory cell wiring layer 213. Specifically, the first contact via 115 may extend in the vertical direction Z from the first peripheral circuit wiring layer 113 and pass through the second trench isolation layer 101SD having a small width and located in the first substrate 101, and may then pass through the bonding interface BI and extend to the memory cell wiring layer 213.

[0048] Through the first contact via 115, the peripheral circuit transistor PT of the peripheral circuit structure 100 may transmit signals and/or power to the memory cell transistor 300 of the memory cell structure 200.

[0049] In addition, recently, a single semiconductor package (see 40 in FIG. 19 or 50 in FIG. 20) includes a plurality of semiconductor chips 10 and employs a stack structure in which the plurality of semiconductor chips 10 are stacked vertically. Accordingly, there is a need for a conductive structure capable of electrically connecting one semiconductor chip 10 to another semiconductor chip 10 and/or a package substrate. That is, the semiconductor chip 10 includes first and second through-vias TSV1 and TSV2 that are electrically connected to the peripheral

circuit structure 100 and the memory cell structure 200 and also connected to the outside of the semiconductor chip 10.

[0050] In the semiconductor chip 10 according to the embodiment, the first and second through-vias TSV1 and TSV2 may each be referred to as a through-silicon via.

[0051] The first through-via TSV1 may extend in the vertical direction Z from the bonding interface BI toward the lower surface of the second substrate 201. That is, the first through-via TSV1 may pass through both the memory cell connector 210 and the second substrate 201. Here, the first through-via TSV1 may have a first width W1. In some embodiments, the first width W1 may be from several micrometers (μm) to several tens of μm . In some embodiments, the first width W1 may refer to a width of an uppermost portion of the first through-via TSV1 according to the view orientation shown in FIG. 1; however, the definition of the first width W1 may not be limited thereto. Also, the first through-via TSV1 may have a first vertical length H1. In some embodiments, the first vertical length H1 may be several tens of μm . A first through-insulating layer may be located around the first through-via TSV1.

[0052] The second through-via TSV2 may extend in the vertical direction Z from the uppermost surface of the first peripheral circuit connector 110 toward the bonding interface BI. That is, the second through-via TSV2 may pass through both the first peripheral circuit connector 110 and the first trench isolation layer 101LD having a large width in the first substrate 101. Here, the second through-via TSV2 may have a second width W2. In some embodiments, the second width W2 may be from several μm to several tens of μm . In some embodiments, the second width W2 may refer to a width of an uppermost portion of the second through-via TSV2 according to the view orientation shown in FIG. 1; however, the definition of the second width W2 may not be limited thereto. Also, the second through-via TSV2 may have a second vertical length H2. In some embodiments, the second vertical length H2 may be several tens of μm . A second through-insulating layer may be located around the second through-via TSV2.

[0053] The first width W1 of the first through-via TSV1 may be greater than the second width W2 of the second through-via TSV2, and the first vertical length H1 of the first through-via TSV1 may be greater than the second vertical length H2 of the second through-via TSV2. That is, depending on the sizes thereof, the first through-via TSV1 may be referred to as a large through-via and the second through-via TSV2 may be referred to as a small through-via. Also, depending on the locations thereof, the first through-via TSV1 may be referred to as a lower through-via and the second through-via TSV2 may be referred to as an upper through-via. In

some embodiments, one first through-via TSV1 may be positioned to correspond to one second through-via TSV2, but the embodiment is not limited thereto.

[0054] In the semiconductor chip 10 according to the embodiment, the vertical level of the uppermost surface of the first through-via TSV1 may be substantially the same as the vertical level of the bonding interface BI, and the vertical level of the lowermost surface of the second through-via TSV2 may be substantially the same as the vertical level of the bonding interface BI. Also, the first through-via TSV1 may have the first width W1 that decreases with increasing distance from the bonding interface BI, and the second through-via TSV2 may have the second width W2 that increases with increasing distance from the bonding interface BI. This may be a specific feature of the inventive concept according to a manufacturing process of the semiconductor chip 10, which is described below.

[0055] In the semiconductor chip 10 according to the embodiment, the first trench isolation layer 101LD having a large width may pass through the first substrate 101, and an inclined sidewall of the first trench isolation layer 101LD may be inclined in the same direction as an inclined sidewall of the second through-via TSV2 passing through the first trench isolation layer 101LD.

[0056] Also, the second trench isolation layer 101SD having a small width may pass through the first substrate 101, and an inclined sidewall of the second trench isolation layer 101SD may be inclined in the same direction as an inclined sidewall of the first contact via 115 passing through the second trench isolation layer 101SD. That is, the inclined sidewall of the second through-via TSV2 may be inclined in the same direction as the inclined sidewall of the first contact via 115.

[0057] In addition, the first through-via TSV1 may include an upper region having the inclined sidewall and a lower region having the vertical sidewall, and the inclined sidewall of the upper region of the first through-via TSV1 may be inclined in the same direction as the inclined sidewall of the second through-via TSV2.

[0058] Here, inclining in the same direction may mean having a tapered shape that decreases in width downwards in the vertical direction Z, but the embodiment is not limited thereto. This equally applies to the following description.

[0059] In the semiconductor chip 10 according to the embodiment, the second through-via TSV2 is formed through the first peripheral circuit connector 110 and the first trench isolation layer 101LD, and then the second peripheral circuit connector 120 is formed on the first peripheral circuit connector 110 and the second through-via TSV2. Accordingly, the vertical level of the lowermost surface of the second peripheral circuit connector 120 may be

substantially the same as the vertical level of the uppermost surface of the second through-via TSV2.

[0060] Recently, with the active development of three-dimensional (3D) semiconductor packages, where a plurality of semiconductor chips 10 are mounted within a single semiconductor package (see 40 in FIG. 19 or 50 in FIG. 20), through-silicon vias are utilized to establish vertical electrical connections by passing through substrates or dies. Accordingly, there is a need for technologies capable of ensuring electrical reliability of connection structures between the plurality of semiconductor chips 10.

[0061] In general, a region in which a through-silicon via is located is referred to as a keep out zone KOZ. That is, in the semiconductor chip 10, the keep out zone KOZ may represent a region in which the peripheral circuit layer CP is not formed, and the peripheral circuit layer CP may be formed around the keep out zone KOZ. Therefore, in designing the semiconductor chip 10 that requires a high degree of integration, a method of reducing the keep out zone KOZ is required.

[0062] In the semiconductor chip 10 according to the inventive concept to satisfy the requirement above, the second through-via TSV2 passing through the first substrate 101 is formed through the inside of the first trench isolation layer 101LD. Accordingly, the keep out zone KOZ may have a minimal area while achieving complete isolation from the peripheral circuit transistor PT. Also, the first through-via TSV1 in contact with the second through-via TSV2 may be formed larger than the second through-via TSV2, thereby securing a process margin during the formation of the second through-via TSV2.

[0063] Ultimately, the inventive concept provides the semiconductor chip 10, wherein, in the bonding structure of the peripheral circuit structure 100 and the memory cell structure 200, the degree of integration may be improved by arranging the first and second through-vias TSV1 and TSV2 so as to reduce the area of the keep out zone KOZ while securing electrical reliability of the connection structure.

[0064] FIGS. 4 and 5 are cross-sectional views illustrating main components of semiconductor chips 20 and 30, respectively, according to other embodiments.

[0065] Most of components constituting the semiconductor chips 20 and 30 described below and materials constituting the components are substantially the same as or similar to those described above in FIGS. 1 to 3. Therefore, for convenience of description, the description focuses on differences from the semiconductor chip 10 described above.

[0066] Referring to FIG. 4, the semiconductor chip 20 may include a plurality of third through-vias TSV3 in contact with one first through-via TSV1 according to the embodiment.

[0067] In the semiconductor chip 20 according to the embodiment, the first and third through-vias TSV1 and TSV3 may each be referred to as a through-silicon via.

[0068] The first through-via TSV1 may extend in the vertical direction Z from the bonding interface BI toward the lower surface of the second substrate 201. That is, the first through-via TSV1 may pass through both the memory cell connector 210 and the second substrate 201. Here, the first through-via TSV1 may have the first width W1. In some embodiments, the first width W1 may be from several μm to several tens of μm . In some embodiments, the first width W1 may refer to a width of an uppermost portion of the first through-via TSV1 according to the view orientation shown in FIG. 4; however, the definition of the first width W1 may not be limited thereto. Also, the first through-via TSV1 may have the first vertical length H1. In some embodiments, the first vertical length H1 may be several tens of μm . The first through-insulating layer may be located around the first through-via TSV1.

[0069] The plurality of third through-vias TSV3 may extend in the vertical direction Z from the uppermost surface of the first peripheral circuit connector 110 toward the bonding interface BI. That is, the plurality of third through-vias TSV3 may pass through both the first peripheral circuit connector 110 and the first trench isolation layer 101LD having a large width in the first substrate 101. Here, the plurality of third through-vias TSV3 may each have a third width W3. In some embodiments, the third width W3 may be from several μm to several tens of μm . In some embodiments, the third width W3 may refer to a width of an uppermost portion of the third through-via TSV3 according to the view orientation shown in FIG. 4; however, the definition of the third width W3 may not be limited thereto. Also, the plurality of third through-vias TSV3 may each have a third vertical length H3. In some embodiments, the third vertical length H3 may be several tens of μm . A third through-insulating layer may be located around each of the plurality of the third through-vias TSV3.

[0070] The first width W1 of the first through-via TSV1 may be greater than the third width W3 of each of the plurality of third through-vias TSV3, and the first vertical length H1 of the first through-via TSV1 may be greater than the third vertical length H3 of each of the plurality of third through-vias TSV3. That is, the first through-via TSV1 may be referred to as a large through-via, and each of the plurality of third through-vias TSV3 may be referred to as a small through-via. The plurality of third through-vias TSV3 may be arranged to correspond to one first through-via TSV1. Although the diagram shows that one first through-via TSV1 corresponds to two third through-vias TSV3, the embodiment is not limited thereto. For example, one first through-via TSV1 may correspond to three or more third through-vias TSV3.

[0071] In the semiconductor chip 20 according to the embodiment, the vertical level of the uppermost surface of the first through-via TSV1 may be substantially the same as the vertical level of the bonding interface BI, and the vertical level of the lowermost surface of the plurality of third through-vias TSV3 may be substantially the same as the vertical level of the bonding interface BI. Also, the first through-via TSV1 may have the first width W1 that decreases with increasing distance from the bonding interface BI, and the plurality of third through-vias TSV3 may have the third width W3 that increases with increasing distance from the bonding interface BI.

[0072] In the semiconductor chip 20 according to the embodiment, the first trench isolation layer 101LD having a large width may pass through the first substrate 101, and the inclined sidewall of the first trench isolation layer 101LD may be inclined in the same direction as an inclined sidewall of the plurality of third through-vias TSV3 passing through the first trench isolation layer 101LD.

[0073] Also, the second trench isolation layer 101SD having a small width may pass through the first substrate 101, and the inclined sidewall of the second trench isolation layer 101SD may be inclined in the same direction as the inclined sidewall of the first contact via 115 passing through the second trench isolation layer 101SD. That is, the inclined sidewall of the plurality of third through-vias TSV3 may be inclined in the same direction as the inclined sidewall of the first contact via 115.

[0074] In addition, the first through-via TSV1 may include the upper region having the inclined sidewall and the lower region having the vertical sidewall, and the inclined sidewall of the upper region of the first through-via TSV1 may be inclined in the same direction as the inclined sidewall of the plurality of third through-vias TSV3.

[0075] In the semiconductor chip 20 according to the embodiment, the plurality of third through-vias TSV3 are formed through the first peripheral circuit connector 110 and the first trench isolation layer 101LD, and then the second peripheral circuit connector 120 is formed on the first peripheral circuit connector 110 and the plurality of third through-vias TSV3. Accordingly, the vertical level of the lowermost surface of the second peripheral circuit connector 120 may be substantially the same as the vertical level of the uppermost surface of the plurality of third through-vias TSV3.

[0076] Referring to FIG. 5, the semiconductor chip 30 according to the embodiment may include a fourth through-via TSV4.

[0077] In the semiconductor chip 30 according to the embodiment, the fourth through-via TSV4 may be referred to as a through-silicon via.

[0078] The fourth through-via TSV4 may extend in the vertical direction Z from the uppermost surface of the first peripheral circuit connector 110 toward the lower surface of the second substrate 201. That is, the fourth through-via TSV4 may pass through all of the first peripheral circuit connector 110, the first trench isolation layer 101LD having a large width in the first substrate 101, the bonding interface BI, the memory cell connector 210, and the second substrate 201. Here, the fourth through-via TSV4 may have a fourth width W4. In some embodiments, the fourth width W4 may be from several μm to several tens of μm . In some embodiments, the fourth width W4 may refer to a width of an uppermost portion of the fourth through-via TSV4 according to the view orientation shown in FIG. 5; however, the definition of the fourth width W4 may not be limited thereto. Also, the fourth through-via TSV4 may have a fourth vertical length H4. In some embodiments, the fourth vertical length H4 may be several tens of μm . A fourth through-insulating layer may be located around the fourth through-via TSV4.

[0079] In the semiconductor chip 30 according to the embodiment, the fourth through-via TSV4 is formed that passes through all of the first peripheral circuit connector 110, the first trench isolation layer 101LD having a large width in the first substrate 101, the memory cell connector 210, and the second substrate 201, and then the second peripheral circuit connector 120 is formed on the first peripheral circuit connector 110 and the fourth through-via TSV4. Accordingly, the vertical level of the lowermost surface of the second peripheral circuit connector 120 may be substantially the same as the vertical level of the uppermost surface of the fourth through-via TSV4.

[0080] In the semiconductor chip 30 according to the embodiment, the fourth through-via TSV4 may include an upper region having an inclined sidewall and a lower region having a vertical sidewall, and the inclined sidewall of the upper region of the fourth through-via TSV4 may be inclined in the same direction as the inclined sidewall of the first trench isolation layer 101LD. Also, the inclined sidewall of the upper region of the fourth through-via TSV4 may be inclined in the same direction as the inclined sidewall of the first contact via 115. Also, the upper region of the fourth through-via TSV4 may have the fourth width W4 that decreases toward the second substrate 201.

[0081] FIGS. 6 to 15 are cross-sectional views showing a method of manufacturing a semiconductor chip in a process sequence, according to an embodiment.

[0082] Referring to FIG. 6, the first trench isolation layer 101LD and the second trench isolation layer 101SD may be formed in the first substrate 101.

[0083] Specifically, the width of the first trench isolation layer 101LD in the horizontal direction may be greater than the width of the second trench isolation layer 101SD in the horizontal direction. That is, the first trench isolation layer 101LD may be wide and the second trench isolation layer 101SD may be narrow. In some embodiments, the vertical length of the first trench isolation layer 101LD may be substantially the same as the vertical length of the second trench isolation layer 101SD.

[0084] Next, the peripheral circuit layer CP including the peripheral circuit transistor PT may be formed on the active region of the first substrate 101. The peripheral circuit transistor PT may include the gate dielectric layer and the gate electrode that are sequentially stacked on the active region. In some embodiments, both sidewalls of the gate electrode may be covered with a gate spacer (not shown).

[0085] Next, the first peripheral circuit insulating layer 111 may be formed to cover the first substrate 101, the first trench isolation layer 101LD, the second trench isolation layer 101SD, and the peripheral circuit layer CP.

[0086] Referring to FIG. 7, the resulting structure of FIG. 6 may be turned over in the vertical direction Z, and a carrier substrate 101S may be attached to the first peripheral circuit insulating layer 111. A bonding layer 101B may be formed between the first peripheral circuit insulating layer 111 and the carrier substrate 101S.

[0087] Referring to FIG. 8, a thinning process may be performed on the resulting structure of FIG. 6 to reduce the thickness of the first substrate 101.

[0088] In some embodiments, the thinning process to reduce the thickness of the first substrate 101 may include a polishing process utilizing a grinder. The polishing process may include a chemical or mechanical polishing process. In other embodiments, the thinning process to reduce the thickness of the first substrate 101 may include an etching process utilizing an etch back process. The etching process may include a dry etching process or a wet etching process.

[0089] Next, the first peripheral circuit insulating layer 111 may extend to an exposed surface of the first substrate 101 and cover the first substrate 101. Accordingly, the first substrate 101 may be surrounded by the first peripheral circuit insulating layer 111.

[0090] Referring to FIG. 9, the memory cell layer MC including the memory cell transistor 300 may be formed on a semiconductor substrate 201S.

[0091] The memory cell transistor 300 may be substantially the same as that described above, and thus, detailed descriptions thereof are omitted.

[0092] Next, the memory cell insulating layer 211 may be formed to cover the semiconductor substrate 201S and the memory cell layer MC.

[0093] Referring to FIG. 10, the resulting structure of FIG. 9 may be turned over in the vertical direction Z, and the second substrate 201 may be attached to the memory cell insulating layer 211. A bonding layer (not shown) may be formed between the memory cell insulating layer 211 and the second substrate 201.

[0094] Referring to FIG. 11, the semiconductor substrate 201S located in an upper region of the resulting structure of FIG. 10 may be removed therefrom.

[0095] Next, the memory cell wiring layer 213 connected to the memory cell transistor 300 is formed, and the memory cell insulating layer 211 extends to cover the memory cell wiring layer 213. Accordingly, the memory cell connector 210 may be formed on the memory cell layer MC.

[0096] Referring to FIG. 12, a first through-hole may be formed that passes through the resulting structure of FIG. 11 from the uppermost surface of the memory cell connector 210 to the lowermost surface of the second substrate 201.

[0097] Next, the first through-insulating layer may be formed on an inner wall of the first through-hole, and the first through-via TSV1 may fill the inside of the first through-hole.

[0098] That is, the first through-via TSV1 may be formed prior to performing a bonding process between the first peripheral circuit insulating layer 111 and the memory cell insulating layer 211. Also, the first through-via TSV1 may include an upper region having an inclined sidewall and a lower region having a vertical sidewall, and the upper region of the first through-via TSV1 may have a tapered shape that decreases in width downwards in the vertical direction Z.

[0099] Referring to FIG. 13, the resulting structure of FIG. 8 may be turned over in the vertical direction Z and bonded onto the resulting structure of FIG. 12 via a heat treatment process.

[0100] The heat treatment process may be performed at a temperature sufficient to form bonding coupling between the first peripheral circuit insulating layer 111 and the memory cell insulating layer 211. Accordingly, the bonding interface BI may be formed between the first peripheral circuit insulating layer 111 and the memory cell insulating layer 211.

[0101] Next, the carrier substrate 101S and the bonding layer 101B located in the upper region of the diagram may be removed.

[0102] Referring to FIG. 14, the first peripheral circuit wiring layer 113 and the first contact via 115 may be formed in the resulting structure of FIG. 13.

[0103] Specifically, the first peripheral circuit wiring layer 113 may include the first contact via 115, and the first contact via 115 may pass through the second trench isolation layer 101SD having a small width and be electrically connected to the memory cell wiring layer 213. Also,

the first peripheral circuit wiring layer 113 may be electrically connected to the peripheral circuit transistor PT.

[0104] Referring to FIG. 15, in the resulting structure of FIG. 14, a second through-hole may be formed from the uppermost surface of the first peripheral circuit insulating layer 111 to the bonding interface BI. The second through-hole may pass through the first peripheral circuit insulating layer 111 and the first trench isolation layer 101LD.

[0105] Accordingly, the upper surface of the first through-via TSV1 may be exposed via the second through-hole.

[0106] Next, the second through-insulating layer may be formed on an inner wall of the second through-hole, and the second through-via TSV2 may fill the inside of the second through-hole.

[0107] That is, the second through-via TSV2 may be formed after performing the bonding process between the first peripheral circuit insulating layer 111 and the memory cell insulating layer 211. Also, the second through-via TSV2 may have an inclined sidewall, and the second through-via TSV2 may have a tapered shape that decreases in width downwards in the vertical direction Z.

[0108] Referring back to FIG. 1, in the resulting structure of FIG. 15, the second peripheral circuit connector 120 may be formed on the second through-via TSV2 and the first peripheral circuit connector 110. Next, the third peripheral circuit connector 130 may be formed on the second peripheral circuit connector 120.

[0109] Through the manufacturing processes described above, the semiconductor chip 10 according to an embodiment may be manufactured.

[0110] FIGS. 16 to 18 are cross-sectional views showing a method of manufacturing a semiconductor chip in a process sequence, according to another embodiment.

[0111] Referring to FIG. 16, after performing the manufacturing processes of FIGS. 6 to 10, the semiconductor substrate 201S may be removed from the resulting structure of FIG. 10.

[0112] The manufacturing processes of FIGS. 6 to 10 may be substantially the same as those described above, and thus, detailed descriptions thereof are omitted.

[0113] Next, the memory cell wiring layer 213 connected to the memory cell transistor 300 is formed, and the memory cell insulating layer 211 extends to cover the memory cell wiring layer 213. Accordingly, the memory cell connector 210 may be formed on the memory cell layer MC.

[0114] Referring to FIG. 17, the resulting structure of FIG. 8 may be turned over in the vertical direction Z and bonded onto the resulting structure of FIG. 16 via a heat treatment process.

[0115] The heat treatment process may be performed at the temperature sufficient to form the bonding coupling between the first peripheral circuit insulating layer 111 and the memory cell insulating layer 211. Accordingly, the bonding interface BI may be formed between the first peripheral circuit insulating layer 111 and the memory cell insulating layer 211.

[0116] Next, the carrier substrate 101S and the bonding layer 101B located in the upper region of the diagram may be removed.

[0117] Next, the first peripheral circuit wiring layer 113 and the first contact via 115 may be formed. Specifically, the first peripheral circuit wiring layer 113 may include the first contact via 115, and the first contact via 115 may pass through the second trench isolation layer 101SD having a small width and be electrically connected to the memory cell wiring layer 213. Also, the first peripheral circuit wiring layer 113 may be electrically connected to the peripheral circuit transistor PT.

[0118] Referring to FIG. 18, in the resulting structure of FIG. 17, a fourth through-hole may be formed from the uppermost surface of the first peripheral circuit insulating layer 111 to the lower surface of the second substrate 201. The fourth through-hole may pass through the first peripheral circuit insulating layer 111, the first trench isolation layer 101LD having a wide width in the first substrate 101, the bonding interface BI, the memory cell insulating layer 211, and the second substrate 201.

[0119] Next, the fourth through-insulating layer may be formed on an inner wall of the fourth through-hole, and the fourth through-via TSV4 may fill the inside of the fourth through-hole.

[0120] That is, the fourth through-via TSV4 may be formed after performing the bonding process between the first peripheral circuit insulating layer 111 and the memory cell insulating layer 211. Also, the fourth through-via TSV4 may include an upper region having an inclined sidewall and a lower region having a vertical sidewall, and the upper region of the fourth through-via TSV4 may have a tapered shape that decreases in width downwards in the vertical direction Z.

[0121] Referring again to FIG. 5, in the resulting structure of FIG. 18, the second peripheral circuit connector 120 may be formed on the fourth through-via TSV4 and the first peripheral circuit connector 110. Next, the third peripheral circuit connector 130 may be formed on the second peripheral circuit connector 120.

[0122] Through the manufacturing processes described above, the semiconductor chip 30 according to an embodiment may be manufactured.

[0123] Although a method of manufacturing the semiconductor chip 20 is not described herein, it is not difficult for a person skilled in the art to understand the method of manufacturing the

semiconductor chip 20 with reference to the methods of manufacturing the semiconductor chips 10 and 30.

[0124] FIGS. 19 and 20 are diagrams illustrating a semiconductor package including a semiconductor chip according to an embodiment.

[0125] Referring to FIG. 19, a semiconductor package 40 may include a stacked semiconductor chip 440 mounted on a package substrate 400.

[0126] The package substrate 400 may include a printed circuit board. A solder bump 403, which is an external connection terminal, may be formed on the lower surface of the package substrate 400.

[0127] The stacked semiconductor chip 440 may include a first semiconductor chip 410 and second semiconductor chips 420 mounted on the first semiconductor chip 410. The second semiconductor chips 420 may be sequentially stacked on the first semiconductor chip 410 in the vertical direction Z. The width of the first semiconductor chip 410 may be greater than the width of each of the second semiconductor chips 420.

[0128] The diagram illustrates that the stacked semiconductor chip 440 includes four second semiconductor chips 420, but the embodiment is not limited thereto. The first semiconductor chip 410 and the second semiconductor chips 420 may include any of the semiconductor chips 10, 20, and 30 according to the embodiments described above.

[0129] For example, the first semiconductor chip 410 may include a first pad 412a and a second pad 412b on both surfaces of a first semiconductor substrate 411. The first pad 412a may be electrically connected to the second pad 412b by using a first through-via structure 413a, a first via connection level VL1, a second through-via structure 413b, and a second via connection level VL2.

[0130] The first through-via structure 413a may be electrically connected to the first via connection level VL1. The second through-via structure 413b may be electrically connected to the second via connection level VL2. Although the diagram illustrates that the first via connection level VL1 and the second via connection level VL2 have the same vertical level for convenience of illustration, the vertical levels of the first via connection level VL1 and the second via connection level VL2 may be different from each other.

[0131] The first pad 412a may be electrically connected to the package substrate 400 via a solder bump 405 that is an external connection terminal. The first semiconductor chip 410 may have an active surface 411a located on the bottom side thereof. Here, the first pad 412a may be referred to as an upper surface pad and the second pad 412b may be referred to as a lower surface pad.

[0132] Each of the second semiconductor chips 420 may include a third pad 422a and a fourth pad 422b on both surfaces of a second semiconductor substrate 421. The third pad 422a may be electrically connected to the fourth pad 422b by using a third through-via structure 423a, a third via connection level VL3, a fourth through-via structure 423b, and a fourth via connection level VL4.

[0133] The third through-via structure 423a may be electrically connected to the third via connection level VL3. The fourth through-via structure 423b may be electrically connected to the fourth via connection level VL4. Although the diagram illustrates that the third via connection level VL3 and the fourth via connection level VL4 have the same vertical level for convenience of illustration, the vertical levels of the third via connection level VL3 and the fourth via connection level VL4 may be different from each other.

[0134] The third pad 422a electrically connects the second semiconductor chips 420 to each other by using an inner connection terminal 424. The inner connection terminal 424 may include an inner connection pad 424a and an inner bump 424b.

[0135] Each of the second semiconductor chips 420 may have an active surface 421a located on the bottom side thereof. The third pad 422a may be referred to as an upper surface pad and the fourth pad 422b may be referred to as a lower surface pad. The second semiconductor chips 420 of the stacked semiconductor chip 440 may be bonded to each other by an adhesive layer 435. The second semiconductor chips 420 may be molded by a molding layer 430 on the first semiconductor chip 410.

[0136] Referring to FIG. 20, a semiconductor package 50 may include a stacked memory device 510, a system-on-chip 520, an interposer 530, and a package substrate 540.

[0137] The stacked memory device 510 may include a buffer die 511 and core dies 512 to 515. Each of the core dies 512 to 515 may include a memory cell for storing data. The buffer die 511 may include a first physical layer 506 and a direct access region 508. The first physical layer 506 may be electrically connected to a second physical layer 521 of the system-on-chip 520 via the interposer 530. The stacked memory device 510 may receive signals from the system-on-chip 520 or transmit signals to the system-on-chip 520 via the first physical layer 506.

[0138] The direct access region 508 may provide an access path through which the stacked memory device 510 may be tested without passing through the system-on-chip 520. The direct access region 508 may include a conductive means for directly communicating with an external test device. Test signals received via the direct access region 508 may be transmitted to the core dies 512 to 515 via through-via structures. For testing the core dies 512 to 515, data read

from the core dies 512 to 515 may be transmitted to a test device via the through-via structures and the direct access region 508. Accordingly, the direct access test on the core dies 512 to 515 may be performed.

[0139] The buffer die 511 and the core dies 512 to 515 may be electrically connected to each other via first to fourth through-via structures 531a, 531b, 533a, and 533b and bumps 535. The buffer die 511 and the core dies 512 to 515 may include semiconductor chips 10, 20, and 30 according to the embodiments described above.

[0140] For example, the buffer die 511 may include the first through-via structure 531a, the first via connection level VL1, the second through-via structure 531b, and the second via connection level VL2. The first through-via structure 531a may be electrically connected to the first via connection level VL1. The second through-via structure 531b may be electrically connected to the second via connection level VL2. Although the diagram illustrates that the first via connection level VL1 and the second via connection level VL2 have the same vertical level for convenience of illustration, the vertical levels of the first via connection level VL1 and the second via connection level VL2 may be different from each other.

[0141] The core dies 512 to 515 each may include the third through-via structure 533a, the third via connection level VL3, the fourth through-via structure 533b, and the fourth via connection level VL4. The third through-via structure 533a may be electrically connected to the third via connection level VL3. The fourth through-via structure 533b may be electrically connected to the fourth via connection level VL4. Although the diagram illustrates that the third via connection level VL3 and the fourth via connection level VL4 have the same vertical level for convenience of illustration, the vertical levels of the third via connection level VL3 and the fourth via connection level VL4 may be different from each other.

[0142] The buffer die 511 may receive, from the system-on-chip 520, signals that are respectively provided to channels via the bumps 502 assigned to the respective channels, or may transmit signals to the system-on-chip 520 via the bumps 502. For example, the bumps 502 may include micro bumps.

[0143] The system-on-chip 520 may utilize the stacked memory device 510 to execute applications supported by the semiconductor package 50. The system-on-chip 520 may control all operations of the stacked memory device 510. The system-on-chip 520 may include the second physical layer 521. The second physical layer 521 may include an interface circuit for transmitting and receiving signals to and from the first physical layer 506 of the stacked memory device 510. The system-on-chip 520 may provide various signals to the first physical layer 506 via the second physical layer 521. The signals provided to the first physical layer 506

may be transmitted to the core dies 512 to 515 via an interface circuit of the first physical layer 506 and the first to fourth through-via structures 531a, 531b, 533a, and 533b.

[0144] The interposer 530 may connect the stacked memory device 510 to the system-on-chip 520. The interposer 530 may connect the first physical layer 506 of the stacked memory device 510 to the second physical layer 521 of the system-on-chip 520 and may provide a physical path formed by using a conductive material. Accordingly, the stacked memory device 510 and the system-on-chip 520 may be stacked on the interposer 530 and may transmit and receive signals to and from each other.

[0145] Bumps 503 may be attached to the upper portion of the package substrate 540, and solder ball 504 may be attached to the lower portion thereof. For example, the bumps 503 may include flip-chip bumps. The interposer 530 may be stacked above the package substrate 540 via the bumps 503. The semiconductor package 50 may transmit and receive signals to and from other external packages or electronic devices via the solder ball 504. For example, the package substrate 540 may include a printed circuit board.

[0146] While the inventive concept has been particularly shown and described with reference to embodiments thereof, it will be understood that various changes in form and details may be made therein without departing from the spirit and scope of the following claims.

WHAT IS CLAIMED IS:

1. A semiconductor chip comprising a memory cell structure and a peripheral circuit structure disposed on the memory cell structure,
wherein the memory cell structure comprises:
 - a memory cell substrate;
 - a memory cell layer disposed on the memory cell substrate;
 - a memory cell wiring layer electrically connected to the memory cell layer;
 - a memory cell insulating layer covering the memory cell layer and the memory cell wiring layer, on the memory cell substrate; and
 - a first through-via passing through the memory cell insulating layer and the memory cell substrate, andwherein the peripheral circuit structure comprises:
 - a peripheral circuit substrate having a first trench isolation layer;
 - a peripheral circuit layer disposed on the peripheral circuit substrate;
 - a first peripheral circuit wiring layer electrically connected to the peripheral circuit layer;
 - a first peripheral circuit insulating layer covering the peripheral circuit layer and the first peripheral circuit wiring layer, on the peripheral circuit substrate; and
 - a second through-via passing through the first peripheral circuit insulating layer and the first trench isolation layer and being in contact with the first through-via,wherein a first width of the first through-via in a horizontal direction is greater than a second width of the second through-via in the horizontal direction, and
a first length of the first through-via in a vertical direction is greater than a second length of the second through-via in the vertical direction.
2. The semiconductor chip of claim 1, further comprising a bonding interface at which the memory cell structure is in contact with and bonded to the peripheral circuit structure,
wherein a vertical level of an uppermost surface of the first through-via is substantially the same as a vertical level of the bonding interface, and
a vertical level of a lowermost surface of the second through-via is substantially the same as the vertical level of the bonding interface.

3. The semiconductor chip of claim 2, wherein the first width of the first through-via decreases with increasing distance from the bonding interface, and
the second width of the second through-via increases with increasing distance from the bonding interface.

4. The semiconductor chip of any one of claims 1 to 3, wherein the first trench isolation layer passes through the peripheral circuit substrate, and
an inclined sidewall of the first trench isolation layer is inclined in a same direction as an inclined sidewall of the second through-via.

5. The semiconductor chip of any one of claims 1 to 3, further comprising a second trench isolation layer passing through the peripheral circuit substrate and having a smaller width in the horizontal direction than the first trench isolation layer,
wherein the first peripheral circuit wiring layer is connected to the memory cell wiring layer via a contact via passing through the second trench isolation layer.

6. The semiconductor chip of claim 5, wherein an inclined sidewall of the second through-via is inclined in a same direction as a sidewall of the contact via.

7. The semiconductor chip of any one of claims 1 to 6, further comprising:
a second peripheral circuit wiring layer on the first peripheral circuit wiring layer; and
a second peripheral circuit insulating layer covering the second peripheral circuit wiring layer, on the first peripheral circuit insulating layer,
wherein a vertical level of a lowermost surface of the second peripheral circuit wiring layer is substantially the same as a vertical level of an uppermost surface of the second through-via.

8. The semiconductor chip of any one of claims 1 to 3, wherein the first through-via comprises: an upper region having an inclined sidewall; and a lower region having a vertical sidewall, and
the inclined sidewall of the upper region of the first through-via is inclined in a same direction as an inclined sidewall of the second through-via.

9. The semiconductor chip of any one of claims 1 to 8, wherein the memory cell layer comprises a plurality of vertical channel transistors.

10. The semiconductor chip of claim 9, wherein a capacitor structure is located between the plurality of vertical channel transistors and the memory cell substrate, and the memory cell layer comprises dynamic random-access memory (DRAM).