INTEGRATING N-TYPE AND P-TYPE METAL GATE TRANSISTORS

FIELD

[0001] Embodiments of the invention relate to the manufacturing of complementary metal-oxide-semiconductor (CMOS) devices. More particularly, embodiments of the invention relate to integrating n-type and p-type metal gate transistors within a single CMOS device.

BACKGROUND

[0002] Prior art CMOS devices manufactured with prior art semiconductor processes typically have polysilicon gate structures. Polysilicon, however, can be susceptible to depletion effects, which can add to the overall gate dielectric thickness in the CMOS device. Furthermore, as the effective physical gate dielectric thickness decreases, the polysilicon depletion contributes proportionally to the total dielectric thickness. It is, therefore, desirable to eliminate polysilicon depletion in order to scale gate oxide thickness.

[0003] Metal gates, on the other hand, are not as susceptible to depletion as polysilicon and are in many ways preferable to polysilicon for forming gate structures. Typical prior art semiconductor processes, however, do not incorporate n-type and p-type metal gates within the same device or integrated circuit. This is due, in part, to the complexity and cost of developing a semiconductor process that can reliably deposit metal gate structures of differing types into the same semiconductor device or integrated circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] Embodiments of the invention are illustrated by way of example and not limitation in the figures of the accompanying drawings, in which like references indicate similar elements and in which:

[0005] Figure 1 illustrates the state of transistors after depositing ILD0 according to one embodiment.

[0006] Figure 2 illustrates the state of transistors after ILD0 polish-back to expose polysilicon gate structures according to one embodiment.

[0007] Figure 3 illustrates the state of transistors after selective n-type poly etch according to one embodiment.

[0008] Figure 4 illustrates the state of transistors after depositing n-type metal according to one embodiment.

[0009] Figure 5 illustrates the state of transistors after polishing the n-type metal according to one embodiment.

[0010] Figure 6 illustrates the state of transistors after selectively etching p-type polysilicon according to one embodiment.

[0011] Figure 7 illustrates the state of transistors after depositing p-type metal according to one embodiment.

[0012] Figure 8 illustrates the state of transistors after polishing the p-type metal according to one embodiment.

[0013] Figure 9 illustrates the completed transistors according to one embodiment.

[0014] Figure 10 illustrates the state of transistors after an optional implant patterning according to one embodiment.

[0015] Figure 11 illustrates the state of transistors after n-type implant and optional ash.

[0016] Figure 12 illustrates the state of transistors after a second selective n-type polysilicon etch.

DETAILED DESCRIPTION

[0017] Embodiments of the invention described herein relate to semiconductor manufacturing. More particularly, embodiments of the invention described relate to integrating n-type and p-type metal gate transistors within the same complementary metal-oxide-semiconductor (CMOS) device or integrated circuit.

[0018] In order to manufacture CMOS devices and integrated circuits that can avoid the effects of gate depletion, embodiments of the invention incorporate n-type and p-type metal gates into the same CMOS device or integrated circuits.

[0019] Figure 1 illustrates a cross-section of a CMOS device containing a p-type transistor and an n-type transistor after depositing ILD0 ("Inter-layer dielectric") according to one embodiment. In Figure 1, poly-silicon gate transistors 105, 110 are fabricated using standard CMOS processing techniques modified in order to prevent silicide formation on the poly-silicon gate electrode. The nitride hard masks 115 are to protect the gate structures during silicidation and ILD0 120 is deposited on the structure.

[0020] The ILD0 is polished back to expose the doped polysilicon gates in Figure 2. The ILD0 polishing also removes residual silicide around the nitride masking layer. After the polysilicon gates 205, 210 are exposed, an ammonium hydroxide etch is used to selectively etch away 305 the n-type polysilicon. The ammonium hydroxide etch is low temperature (e.g., <40 deg. Celsius), uses

sonication, and has a concentration of approximately 2 – 29%. The result of the polysilicon etch is illustrated in Figure 3.

[0021] Removal of the n-type polysilicon above the gate dielectric creates a damascene-like "trench" which is filled with an n-type metal 405, such as Hf, Zr, Ti, Ta, or Al, as illustrated in Figure 4. Alternatively, the trench can be filled with an alloy containing an n-type component using PVD ("Physical vapor deposition"), CVD ("Chemical vapor deposition"), or ALD ("Atomic Layer deposition"). CVD and ALD may use an organometallic or halide precursor, and a reducing atmosphere. Furthermore, the thickness of the n-type metal or alloy can be such that the trench is only partially filled. For example, the thickness of the n-type metal or alloy can vary from approximately 50 angstroms to approximately 1000 angstroms in various embodiments. If the trenches are not completely filled, they may be filled with an easily polished metal, such as W ("Tungsten") or Al ("Aluminum").

[0022] The n-type metal is polished back to create the n-type metal gates 505 and to expose the p-type polysilicon gate 510 as illustrated in Figure 5.

[0023] Figure 6 illustrates the transistors after a selective dry etch is performed to remove the p-type polysilicon without removing the n-type metal gate. The selective dry etch can be performed using a parallel plate or ECR ("Electron cyclotron resonance") etcher and SF6 ("Sulfur hexafluoride"), HBr ("Hydrogen Bromide"), HI ("Hydrogen Iodide"), Cl2 ("Chlorine"), Ar ("Argon"), and/or He ("Helium"). Alternatively, a wet etch, such as approximately 20 – 30 % TMAH ("Tetramethylammonium Hydroxide") at approximately 60 – 90 degrees Celsius with or without sonication may also be used to remove the p-type polysilicon gate.

[0024] A p-type metal, such as Ru ("Ruthenium") , Pd ("Palladium"), Pt ("Platinum"), Co ("Cobalt"), Ni ("Nickel"), TiAlN ("Titanium Aluminum Nitride"), or

WCN ("Tungsten Carbon Nitride") can be used to fill the gate trench created by etching the p-type polysilicon gate 605. Alternatively, an alloy using p-type metal can be deposited in the trench using chemical vapor deposition or atomic layer deposition with an organometallic precursor and a reducing atmosphere. Furthermore, the thickness of the p-type metal or alloy can be such that the trench is only partially filled. Figure 7 illustrates the transistors after the p-type metal or alloy has been deposited in the gate trench 710.

[0025] The p-type metal or alloy is polished back, as illustrated in Figure 8, to create the p-type and n-type gate structures 805, 810, and ILD0 is again deposited to provide room for the contact layer.

[0026] Contacts 903 are etched and deposited, as illustrated in Figure 9, resulting in the final transistor structure.

[0027] Rather than using a dry etch to remove the p-type polysilicon as described above, the p-type polysilicon gate can be converted to n-type in order to allow a gentler wet etch to remove the polysilicon rather than a dry etch. For example, after the p-type polysilicon 1010 has been exposed, rather than using a selective dry etch to remove the polysilicon, an n-type implant 1015 is performed to change the doping of the polysilicon in order to allow an ammonium hydroxide etch to be performed, as illustrated in Figure 10.

[0028] The result of the implant and ash (if required) is illustrated in Figure 11. An ammonium hydroxide etch removes the remaining polysilicon gate structure 1210 resulting in the structure illustrated in Figure 12. A p-type metal or alloy may then be deposited in the trench left by removing the p-type polysilicon gate as described above.

[0029] While the invention has been described with reference to illustrative embodiments, this description is not intended to be construed in a limiting sense. Various modifications of the illustrative embodiments, as well as other embodiments, which are apparent to persons skilled in the art to which the invention pertains are deemed to lie within the spirit and scope of the invention.

CLAIMS

1. A process comprising: forming sidewalls and dielectrics of transistors within a complementary metal-oxide-semiconductor (CMOS) integrated circuit upon a semiconductor substrate; forming an n-type and a p-type metal gate structure within trenches formed by the sidewalls and dielectrics, wherein the n-type and p-type metal gate structures are formed by implanting n-type and p-type material into the n-type and p-type metal gate structures, respectively.

2. The process of claim 1 wherein a trench is formed by a first etch of a polysilicon gate structure corresponding to one of the n-type and p-type metal gate structures, the first etch leaving substantially un-etched a polysilicon gate structure corresponding to the other of the n-type and p-type metal gate structures.

3. The process of claim 2 further comprising depositing a metal of a first type into a trench formed by the first etch and performing a second etch of the polysilicon gate structure corresponding to the other of the n-type and p-type metal gate structures.

4. The process of claim 3 further comprising depositing a metal of a second type into a trench formed by the second etch, the second type being different from the first type of metal.

5. The process of claim 4 wherein the first and second etches are a dry etch.

6. The process of claim 4 wherein the first and second etches are a wet etch.

7. The process of claim 4 wherein the metal of the first type is an n-type metal and the metal of the second type is a p-type metal.

8. The process of claim 4 wherein the metal of the first type is a p-type metal and the metal of the second type is an n-type metal.

9. A process comprising:

forming an n-type and a p-type transistor upon a semiconductor substrate, the n-type and p-type transistors comprising n-type and p-type polysilicon gates, respectively;

forming an interlayer dielectric layer (ILDO) on a top of the n-type and p-type transistors;

removing an ILDO layer from the top of the n-type and p-type polysilicon gates;

etching the n-type polysilicon gate to form a first trench bound in part by substantially vertical lateral side-wall spacers and a gate dielectric on the bottom of the first trench;

depositing n-type metal into the first trench;

removing excess n-type gate material to expose the top of the n-type metal gate and the p-type polysilicon gate;

etching the p-type polysilicon gate to form a second trench bound in part by substantially vertical lateral side-wall spacers and a gate dielectric on the bottom of the second trench;

depositing a p-type metal gate within the second trench;

removing excess p-type gate material to expose the top of the n-type metal gate and the p-type metal gate;

implanting n-type material in the n-type metal in the first trench; and

implanting p-type material in the p-type metal in the second trench.

10. The process of claim 9 further comprising forming ILDO on top of the n- type and p-type transistors.

11. The process of claim 10 further comprising forming source, gate, and drain contacts to the n-type and p-type transistors.

12. The process of claim 9 wherein the n-type metal gate is selected from a group consisting of Hf, Zr, Ti, Ta, and Al.

13. The process of claim 9 wherein the p-type metal gate is selected from a group consisting of Ru, Pd, Pt, Co, Ni, TiAlN and WCN.

14. The process of claim 9 wherein the p-type metal gate and the n-type metal gate is at least 50 angstroms and no greater than 1000 angstroms thick.

15. The process of claim 9 wherein etching the n-type and p-type polysilicon gates is an ammonium hydroxide etch.

16. The process of claim 9 wherein etching the n-type and p-type polysilicon gates is performed by using a wet etch.

17. The process of claim 9 wherein the n-type metal gate is doped by implanting n-type material after the metal gate has been deposited into the first trench.

18. The process of claim 9 wherein the p-type metal gate is doped by implanting the metal gate with p-type material after the metal gate has been deposited into the second trench.

19. A process comprising:

forming an n-type and a p-type transistor upon a semiconductor substrate, the n-type and p-type transistors comprising n-type and p-type polysilicon gates, respectively;

removing an n-type polysilicon gate from a n-type transistor formed on a semiconductor substrate to form a first trench bound in part by substantially vertical lateral side-wall spacers and a gate dielectric on a bottom of the first trench, while maintaining a p-type polysilicon gate of a p-type transistor formed on the semiconductor substrate;

depositing n-type metal into the first trench to form a n-type metal gate and removing excess n-type metal to expose a top of the n-type metal gate and the p-type polysilicon gate;

removing the p-type polysilicon gate to form a second trench bound in part by substantially vertical lateral side-wall spacers and a gate dielectric on a bottom of the second tench;

depositing p-type metal into the second trench to form a p-type metal gate and removing excess p-type metal to expose the top of the n-type metal gate and the p-type metal gate;

implanting n-type material in the n-type metal in the first trench; and

implanting p-type material in the p-type metal in the second trench.

20. The process of claim 19 further comprising removing an interlayer dielectric layer from a top of the n-type and p-type polysilicon gates.

21. The process of claim 19 further comprising forming source, gate, and drain contacts to the n-type and p-type transistors.

22. The process of claim 19, wherein removing the p-type polysilicon gate comprises converting the p-type polysilicon gate to an n-type polysilicon gate, and using a wet etch to remove the converted polysilicon gate.