Abstract

Illustratively, the present invention includes a method of integrated circuit manufacturing which includes forming a raised topological feature (31) upon a first substrate (40). A portion of the raised feature is removed, thereby exposing a cross sectional view of the raised feature with the substrate remaining substantially undamaged. The cross sectional view has a critical dimension. The critical dimension of the cross sectional view is measured using a first measuring instrument. Then the critical dimension is measured using a second measuring instrument. The measurements of the first and second measuring instruments are correlated. Then, using the second measuring instrument, raised features on a plurality of second substrates are measured.

This Sheet Has Been Replaced

