

PID FILTER CIRCUIT AND FIFO CIRCUIT

ABSTRACT

A PID (Packet Identifier) filter circuit and an FIFO (First-in, First-out) circuit in which there is implemented a filtering of an input packet data in answer to the PID included in the packet data, it can cope with corresponding length of the word of the PID or position of the PID in the packet without enlarging circuit scale. There is provided with a comparison value table (13) for storing therein comparison value beforehand, a comparator (12) for taking out comparison value successively from the comparison value table, (13) and for comparing value of the PID in the input packet data with the comparison value taken out in every one word, and an FIFO (First-in, First-out) memory (11) for storing therein the input packet data through first-in first out

Fig.4