WHAT IS CLAIMED IS:

1. A three-dimensional memory, comprising:

array areas and a step area, the step area being between the array areas;

a stack structure comprising a gate layer and a dielectric layer disposed alternately and comprising a plurality of steps in the step area;

an etch stop layer disposed on the plurality of steps and in contact with the dielectric layer;

a protective layer covering the stack structure and the etch stop layer;

a plurality of connection pillars, wherein each of the connection pillars penetrates through the protective layer and the etch stop layer on a corresponding step and is connected with the gate layer of the corresponding step; and

an isolation structure penetrating through the stack structure and the protective layer and comprising a first insulation layer, wherein a material of the first insulation layer is different from that of the etch stop layer.

2. The three-dimensional memory of claim 1, wherein the etch stop layer comprises a plurality of etch stop portions, the etch stop portion is provided on each of the steps, and the plurality of etch stop portions are disposed as being spaced apart from each other.

3. The three-dimensional memory of claim 1, wherein the etch stop layer is a continuous film layer covering the plurality of steps.

4. The three-dimensional memory of claim 3, wherein the etch stop layer comprises an insulation material.

5. The three-dimensional memory of claim 1, further comprising a first dielectric layer and a second dielectric layer, the first dielectric layer is disposed around the gate layer, and the second dielectric layer is disposed around the etch stop layer

6. The three-dimensional memory of claim 1, wherein the isolation structure further comprises a filling layer, and the first insulation layer is located between the filling layer and the stack structure.

7. The three-dimensional memory of claim 2, further comprising:

an isolation structure penetrating through the stack structure and the protective layer and comprising a second insulation layer, wherein a material of the second insulation layer is the same as that of the etch stop layer.

8. The three-dimensional memory of claim 7, wherein the isolation structure further comprises a filling layer, and the second insulation layer is located between the filling layer and the stack structure.

9. The three-dimensional memory of claim 8, wherein the isolation structure further comprises a third insulation layer located between the filling layer and the second insulation layer.

10. The three-dimensional memory of claim 1, wherein a thickness of the etch stop layer is greater than a thickness of the gate layer.

11. A three-dimensional memory, comprising:

array areas and a step area, the step area being between the array areas;

a stack structure comprising a gate layer and a dielectric layer disposed alternately and comprising a plurality of steps in the step area;

an insulation layer disposed on the plurality of steps and in contact with the dielectric layer;

a protective layer covering the stack structure and the insulation layer;

a plurality of connection pillars, wherein each of the connection pillars penetrates through the protective layer and the insulation layer on a corresponding step and is connected with the gate layer of the corresponding step; and

an isolation structure penetrating through the stack structure and the protective layer and comprising a first insulation layer, wherein a material of the first insulation layer is different from that of the insulation layer.

12. The three-dimensional memory of claim 11, wherein the insulation layer is a continuous film layer covering the plurality of steps, and wherein a thickness of the insulation layer is greater than a thickness of the gate layer.

13. A method of fabricating a three-dimensional memory, comprising:

forming an initial stack structure comprising a first sacrificial layer and a dielectric layer disposed alternately and comprising a plurality of initial steps, wherein the initial stack structure comprises array areas and a step area between the array areas, and the plurality of initial steps are in the step area;

forming a second sacrificial layer on the initial stack structure;

forming a gate line slit penetrating through the second sacrificial layer and the initial stack structure, and removing the first sacrificial layer to form a first cavity and removing the second sacrificial layer to form a second cavity through the gate line slit;

forming a gate layer in the first cavity;

forming an etch stop layer in the second cavity, wherein the etch stop layer is in contact with the dielectric layer; and

forming an isolation structure in the gate line slit, wherein the isolation structure comprises a first insulation layer, and a material of the first insulation layer is different from that of the etch stop layer.

14. The method of claim 13, further comprising:

after forming the second sacrificial layer on the initial stack structure, etching the second sacrificial layer to form a plurality of sacrificial portions, wherein one of the sacrificial portions is provided on each of the initial steps, and the plurality of sacrificial portions are disposed as being spaced apart from each other.

15. The method of claim 13, wherein the forming the gate layer in the first cavity and forming the etch stop layer in the second cavity comprise:

filling the first cavity with a gate material and filling the second cavity partially with the gate material through the gate line slit;

removing the gate material in the second cavity; and

forming the etch stop layer in the second cavity.

16. The method of claim 15, wherein the forming the etch stop layer in the second cavity comprises: filling the second cavity with a dielectric material through the gate line slit, wherein the dielectric material in the second cavity forms the etch stop layer.

17. The method of claim 15, wherein the forming the etch stop layer in the second cavity

comprises:

filling the second cavity with a semiconductor material through the gate line slit; and

removing the semiconductor material covering a sidewall of the gate line slit, to form the etch stop layer.

18. The method of claim 15, further comprising:

before forming the gate layer in the first cavity and forming the etch stop layer in the second cavity, forming a first dielectric layer in the first cavity, and forming a second dielectric layer in the second cavity, wherein the first dielectric layer covers a sidewall of the first cavity, and the second dielectric layer covers a sidewall of the second cavity.

19. The method of claim 13, further comprising:

forming a protective layer covering the initial stack structure and the second sacrificial layer, wherein the gate line slit also penetrates through the protective layer.

20. The method of claim 19, further comprising:

forming a plurality of initial contact holes penetrating through the protective layer;

etching the etch stop layer exposed by the initial contact hole, to form a contact hole; and

filling the contact hole with a conductive material to form a connection pillar, wherein the connection pillar is electrically connected with the gate layer of the corresponding step.