

TELEVISION RECEIVER WITH NON-LINEAR PROCESSING SELECTIVELY DISABLED
DURING DISPLAY OF MULTI-IMAGE VIDEO SIGNAL

Abstract

A picture in picture (PIP) video signal is applied to a display device (112) via a non-linear processor (202) that is enabled during display of a main picture component and disabled during display of an inset picture component responsive to a PIP identification signal (S7). The non-linear processor is formed in an integrated circuit (200) which includes a pin (214) for connection to a capacitor (C1) that stores peak levels of the PIP video signal.

0 The PIP identification signal (S7) is subjected to a voltage level translation for varying the pin voltage over a range of values, ΔV , for facilitating ON/OFF operation of the non-linear processor (202) and is applied to a selected plate of the capacitor (C1) for varying the pin (214) voltage without substantial alternation of charge

5 stored within the capacitor (C1) whereby only a single pin is required for both capacitor storage and on/off control of the non-linear processor and undesirable visual artifacts, such as "trailing contrast bars" (504), are avoided.

0 Fig 2