SIMPLIFIED PITCH DOUBLING PROCESS FLOW

FIELD OF THE INVENTION

[0001] The present invention relates generally to integrated circuit fabrication, and more specifically to simplified processes for forming pitch doubled integrated circuit features.

BACKGROUND OF THE INVENTION

[0002] Integrated circuits are continuously being made smaller as demand for portability, computing power, memory capacity and energy efficiency in modern electronics grows. Therefore, the size of the integrated circuit constituent features, such as electrical devices and interconnect line widths, is also decreasing continuously. The trend of decreasing feature size is evident in memory circuits or devices such as dynamic random access memory ("DRAM"), flash memory, nonvolatile memory, static random access memory ("SRAM"), ferroelectric ("FE") memory, logic gate arrays and so forth.

[0003] For example, DRAM typically comprises millions of identical circuit elements, known as memory cells. A typical memory cell consists of two electrical devices: a storage capacitor and an access field effect transistor. Each memory cell is an addressable location that can store one binary digit ("bit") of data. A bit can be written to a memory cell through the transistor and read by sensing charge on the reference electrode of the storage capacitor. By decreasing the sizes of these constituent electrical devices and the conducting lines that interconnect them, the sizes of the memory devices incorporating memory cells can likewise be decreased. In similar fashion, the storage capacities of these devices can be increased by fitting more memory cells into the memory devices.

[0004] As another example, flash memory (for example, electrically erasable programmable read only memory or "EEPROM") is a type of memory that is typically erased and reprogrammed in blocks instead of one byte at a time. A typical flash memory comprises a memory array, which includes a large number of

memory cells. The memory cells include a floating gate field effect transistor capable of holding a charge. The data in a memory cell is determined by the presence or absence of charge on the floating gate. The cells are usually grouped into sections called "erase blocks." The memory cells of a flash memory array are typically arranged into a "NOR" architecture (in which each memory cell is directly coupled to a bit line) or a "NAND" architecture (in which memory cells are coupled into "strings" of cells, such that each cell is coupled indirectly to a bit line and requires activating the other cells of the string for access). The memory cells within an erase block can be electrically programmed on a random basis by charging the floating gate. The charge can be removed from the floating gate by a block erase operation, wherein all floating gate memory cells in the erase block are erased in a single operation.

[0005] As is evident from the examples provided here, memory devices typically include large patterns or arrays of electrical devices and conductors that are used to interconnect the electrical devices. The "pitch" of such a pattern is defined as the distance between an identical point in two neighboring features in the pattern. These features are typically defined by openings in, and are spaced apart from each other by, a material such as an insulator or conductor. Thus, pitch can be understood as the sum of the width of a feature and the width of the space separating that feature from a neighboring feature.

BRIEF SUMMARY OF THE INVENTION

[0006] In one embodiment of the present invention, a method for fabricating a semiconductor device comprises patterning a layer of photoresist material to form a plurality of mandrels. The method further comprises using an atomic layer deposition technique to deposit an oxide material onto the plurality of mandrels. The method further comprises anisotropically etching the oxide material from exposed horizontal surfaces. The method further comprises etching the photoresist material selectively with respect to the oxide material, thereby forming a plurality of oxide spacers.

[0007] In another embodiment of the present invention, a method of forming a memory device comprises forming a plurality of mandrels over a substrate. The mandrels are separated by exposed portions of the substrate. The method further comprises depositing a spacer material over the mandrels and over the exposed portions of the substrate using an atomic layer deposition technique conducted at a temperature less than about 100°C. The method further comprises anisotropically etching the spacer material from (a) exposed horizontal surfaces of the plurality of mandrels and (b) the exposed portions of the substrate. Spacer material is left remaining on vertical sidewalls of the plurality of mandrels.

[0008] In another embodiment of the present invention, a method of forming an integrated circuit comprises forming a plurality of mandrels on a hard mask layer. The mandrels comprise a photosensitive material. The method further comprises depositing a spacer material using an atomic layer deposition technique. The spacer material covers the plurality of mandrels. The method further comprises anisotropically etching the spacer material from horizontal surfaces, thereby exposing photosensitive material. The method further comprises removing exposed photosensitive material after anisotropically etching the spacer material, thereby leaving a pattern of spacers on the hard mask layer. The method further comprises transferring the pattern of spacers to the hard mask layer. The method further comprises etching the pattern of spacers from the hard mask layer.

[0009] In another embodiment of the present invention, a method of integrated circuit fabrication comprises using a lithographic technique to define a plurality of elongate mandrels over a hard mask layer. The mandrels comprise a photoresist material. The method further comprises forming a pattern of spacers around the mandrels. The pattern of spacers has a pitch that is smaller than a minimum resolvable pitch of the lithographic technique. The pattern of spacers is formed from an oxide material. The pattern of spacers is deposited using an atomic layer deposition technique at a temperature less than about 100°C.

[0010] In another embodiment of the present invention, a method for fabricating a semiconductor device comprises patterning a layer of photoresist material to form a plurality of mandrels in a device array region. The method further

comprises depositing an oxide material over the plurality of mandrels and over a device peripheral region. The method further comprises anisotropically etching the oxide material from exposed horizontal surfaces in the device array region. The method further comprises forming a pattern of photoresist material over the oxide material in the device peripheral region. The method further comprises selectively etching photoresist material from the device array region and from the device peripheral region.

[0011] In another embodiment of the present invention, a method of forming a memory device comprises forming a plurality of mandrels over a substrate in an array region of the memory device. The mandrels optionally comprise a photoresist material. The mandrels are separated by exposed portions the substrate. The method further comprises depositing a spacer material over the mandrels, over the exposed portions of the substrate, and over a peripheral region of the memory device. The method further comprises depositing a peripheral mask over the spacer material in the peripheral region of the memory device. The method further comprises anisotropically etching the spacer material from exposed horizontal surfaces. Spacer material is left remaining (a) on vertical sidewalls of the mandrels in the array region, and (b) between the substrate and the peripheral mask in the peripheral region.

[0012] In another embodiment of the present invention, a method of forming an integrated circuit comprises forming a plurality of mandrels on a hard mask layer in an array region. The mandrels comprise a photoresist material. The method further comprises depositing an oxide material over the array region and over a peripheral region that surrounds the array region. The oxide material covers the plurality of mandrels. The method further comprises forming a pattern of photoresist material over the oxide material in the peripheral region. The method further comprises anisotropically etching the oxide material from horizontal surfaces in the array region. The method further comprises removing exposed photoresist material from the array region and the peripheral region after anisotropically etching the oxide material.

[0013] In another embodiment of the present invention, a method of integrated circuit fabrication comprises using a lithographic technique to define a plurality of elongate mandrels over a hard mask layer in an integrated circuit array region. The mandrels comprise a photoresist material. The method further comprises forming a pattern of spacers around the plurality of elongate mandrels. The pattern of spacers have a pitch that is smaller than a minimum resolvable pitch of the lithographic technique. The spacers are formed from an oxide material that is deposited at a temperature less than about 100°C.

[0014] In another embodiment of the present invention, a partially formed integrated circuit comprises a substrate. The partially formed integrated circuit further comprises a hard mask layer positioned over the substrate. The partially formed integrated circuit further comprises a plurality of spacer loops that are formed directly over the hard mask layer, and that are at least partially positioned in an array region of the partially formed integrated circuit. The partially formed integrated circuit further comprises a mask at least partially defined in a peripheral region of the partially formed integrated circuit, wherein the mask is also directly formed over the hard mask layer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] Exemplary embodiments of the integrated circuits and integrated circuit fabrication techniques disclosed herein are illustrated in the accompanying drawings, which are for illustrative purposes only, and which are not necessarily drawn to scale. The drawings comprise the following figures, in which like numerals indicate like parts.

[0016] Figure 1A is a schematic cross-sectional view of a substrate having a plurality of mask lines formed thereon.

[0017] Figure 1B is a schematic cross-sectional view of the substrate of Figure 1A after performing an anisotropic etch process that transfers the mask pattern into a temporary layer.

[0018] Figure 1C is a schematic cross-sectional view of the substrate of Figure 1B after removing the mask lines and performing an isotropic "shrink" etch.

[0019] Figure 1D is a schematic cross-sectional view of the substrate of Figure 1C after blanket depositing a spacer material over mandrels left in the temporary layer.

[0020] Figure 1E is a schematic cross-sectional view of the substrate of Figure 1D after performing a directional spacer etch to leave pitch-multiplied features or spacers.

[0021] Figure 1F is a schematic cross-sectional view of the substrate of Figure 1E after removing the mandrels.

[0022] Figure 2A is a schematic cross-sectional view of an example partially formed integrated circuit.

[0023] Figure 2B is a schematic top view of the partially formed integrated circuit of Figure 2A.

[0024] Figure 3A is a schematic cross-sectional view of the example partially formed integrated circuit of Figure 2A after forming lines in an array region in a photoresist layer.

[0025] Figure 3B is a schematic top view of the partially formed integrated circuit of Figure 3A.

[0026] Figure 4A is a schematic cross-sectional view of the example partially formed integrated circuit of Figure 3A after performing a trim etch.

[0027] Figure 4B is a schematic top view of the partially formed integrated circuit of Figure 4A.

[0028] Figure 5A is a schematic cross-sectional view of the example partially formed integrated circuit of Figure 4A after blanket depositing a low temperature spacer material over photoresist mandrels.

[0029] Figure 5B is a schematic top view of the partially formed integrated circuit of Figure 5A.

[0030] Figure 6A is a schematic cross-sectional view of the example partially formed integrated circuit of Figure 5A after defining features in the peripheral region.

[0031] Figure 6B is a schematic top view of the partially formed integrated circuit of Figure 6A, wherein a periphery photoresist layer is blanket deposited over substantially the entire peripheral region.

[0032] Figure 6C is a schematic top view of the partially formed integrated circuit of Figure 6A, wherein a periphery photoresist layer is patterned to define periphery features.

[0033] Figure 6D is a schematic top view of the partially formed integrated circuit of Figure 6A, wherein a periphery photoresist layer partially overlaps the low temperature spacer material.

[0034] Figure 7A is a schematic cross-sectional view of the example partially formed integrated circuit of Figure 6A after performing an anisotropic etch of the low temperature spacer material.

[0035] Figure 7B is a schematic top view of the partially formed integrated circuit of Figure 7A.

[0036] Figure 8A is a schematic cross-sectional view of the example partially formed integrated circuit of Figure 7A after removing exposed photoresist material.

[0037] Figure 8B is a schematic top view of the partially formed integrated circuit of Figure 8A.

[0038] Figure 9A is a schematic cross-sectional view of the example partially formed integrated circuit of Figure 8A after transferring the pattern of spacers into underlying hard mask layers.

[0039] Figure 9B is a schematic top view of the partially formed integrated circuit of Figure 9A.

DETAILED DESCRIPTION OF THE INVENTION

[0040] As the size of the electrical devices and the conductors that comprise a memory device are made smaller and smaller, ever greater demands are placed on the techniques used to form these features. For example, photolithography is commonly used to pattern device features, such as conductive lines, on a substrate. The concept of pitch can be used to describe the size of these

features. Due to optical factors such as light or radiation wavelength, however, photolithography techniques have a minimum pitch below which features cannot be formed reliably. Thus, the minimum pitch of a photolithographic technique can limit feature size reduction.

[0041] One technique proposed for extending the capabilities of photolithographic techniques beyond their minimum pitch is the "pitch doubling" technique. This technique is illustrated in Figures 1A–1F, and is described in U.S. Patent 5,328,810 (issued 12 July 1994), the entire disclosure of which is incorporated herein by reference. With reference to Figure 1A, photolithography is first used to form a pattern of lines 10 in a photoresist layer overlying a layer of a temporary or expendable material 20 and a substrate 30. Common wavelengths which are used in performing the photolithography include, but are not limited to, 157 nm, 193 nm, 248 nm or 365 nm. Before performing subsequent processing steps, the lines 10 are optionally shrunk using an isotropic etch. As shown in Figure 1B, the pattern is then transferred by an etch step, such as an anisotropic etch step, to the layer of expendable material 20, thereby forming placeholders or mandrels 40. The photoresist lines 10 can be stripped and the mandrels 40 can be isotropically etched to increase the distance between neighboring mandrels 40, as shown in Figure 1C. A layer of spacer material 50 is subsequently deposited over the mandrels 40, as shown in Figure 1D. Spacers 60 are then formed on the sides of the mandrels 40 by preferentially etching the spacer material from the horizontal surfaces in a directional spacer etch, as shown in Figure 1E. The remaining mandrels 40 are then removed, leaving behind only the spacers 60, which together act as a mask for patterning, as shown in Figure 1F. Thus, where a given pattern area formerly defined one feature and one space (each having a width F, for a pitch of $2F$), the same pattern area now includes two features and two spaces, as defined by spacers 60 (each having a width $\frac{1}{2}F$, for a pitch of F). Consequently, the smallest feature size possible with a photolithographic technique is effectively decreased by using the pitch doubling technique.

[0042] While pitch is actually reduced using these techniques, this reduction in pitch is conventionally referred to as "pitch doubling", or more generally,

"pitch multiplication". This is because these techniques allow the number of features in a given region of the substrate to be doubled, or more generally, multiplied. Thus, using the conventional terminology, "multiplication" of pitch by a certain factor actually involves reducing the pitch by that factor. The conventional terminology is retained herein. By forming multiple layers of spacers upon each other, the definable feature size can be made even smaller. Thus, the terms "pitch multiplication" and "pitch doubling" refer to the process generally, regardless of the number of times the spacer formation process is employed.

[0043] Some proposed methods for forming patterns in the periphery and in the array of a memory device involve use of two separate carbon layers. For example, in one such method, the mandrels used to define spacer loops are formed in an upper carbon layer. After pitch doubling and periphery patterning processes are performed, the array pattern is transferred to a lower carbon layer. While this process does allow features of different sizes to be formed in the array and periphery regions, use of a low temperature oxide material to define the spacer loops allows mandrels to be formed from the existing photoresist layer. This advantageously allows the top carbon layer to be omitted, thereby simplifying production.

[0044] In accordance with the foregoing, simplified and improved techniques have been developed for forming pitch doubled features in a semiconductor or integrated circuit device.

[0045] In certain embodiments, the feature pattern to be transferred to a substrate has a pitch below the minimum pitch of the photolithographic technique used for processing the substrate. Additionally, certain embodiments can be used to form arrays of features, including logic or gate arrays and volatile and non-volatile memory devices such as DRAM, phase change memory ("PCM"), programmable conductor random access memory ("PCRAM"), read only memory ("ROM"), flash memory. In such devices, pitch multiplication is usable to form, for example, transistor gate electrodes and conductive lines in the array region of the devices. Optionally, conventional photolithography can be combined in a particular sequence with the aforementioned simplified pitch doubling technique to simultaneously

process larger features useful for logic circuits, such as local interconnects and complementary metal oxide semiconductor ("CMOS") circuits, in the peripheral region of the devices. For example, the logic array can be a field programmable gate array ("FPGA") having a core array similar to a memory array and a periphery with supporting logic circuits. Exemplary masking steps in the course of fabricating a memory device are illustrated in the figures and are described herein.

[0046] Figures 2A and 2B illustrate schematic cross-sectional and top views, respectively, of an example partially fabricated integrated circuit 100, such as a memory device. Figure 2B illustrates that the integrated circuit 100 comprises a central array region 102 that is surrounded by a peripheral region 104. It will be appreciated that, after the integrated circuit 100 is fabricated, the array region 102 will typically be densely populated with conducting lines and electrical devices such as transistors and capacitors. Pitch multiplication can be used to form features in the array region 102, as discussed herein.

[0047] On the other hand, the peripheral region 104 optionally can include features more complicated and/or larger than those in the array region 102. Conventional photolithography, rather than pitch multiplication, is typically used to pattern these more complicated and/or larger features, examples of which include various types of logic circuitry. The geometric complexity of the logic circuits located in the peripheral region 104 makes using pitch multiplication difficult in this region of the integrated circuit 100. In contrast, the regular grid typical of array patterns is conducive to pitch multiplication. Additionally, some devices in the peripheral region 104 may require larger geometries due to electrical constraints, thereby making pitch multiplication less advantageous than conventional photolithography for such devices. In addition to possible differences in relative scale, the relative positions, and the number of peripheral regions 104 and array regions 102 in the integrated circuit 100 can vary in other embodiments. In embodiments wherein different processing techniques are separately used to form features in the array region 102 and the peripheral region 104, the peripheral region 104 can be masked during processing of the array region.

[0048] Figure 2A illustrates that the partially formed integrated circuit 100 includes a substrate 106 having a first hard mask layer 108 formed thereover. In an example embodiment, the first hard mask layer 108 comprises a material such as silicon nitride, silicon oxide, or an organic material, such as an amorphous carbon material, a polymer material, or a spin on dielectric material. In a preferred embodiment, the first hard mask layer 108 comprises a form of amorphous carbon that is highly transparent to light and that offers further improvements for photo alignment by being transparent to the wavelengths of light used for such alignment. In other modified embodiments, the first hard mask layer 108 is omitted.

[0049] An optional second hard mask layer 110 is formed over the first hard mask layer 108. The second hard mask layer 110 preferably comprises an inorganic material. Example materials for the second hard mask layer 110 include silicon nitride, polycrystalline silicon, or a dielectric antireflective coating ("DARC"), such as silicon-rich silicon oxynitride. Preferably, the material comprising the second hard mask layer 110 can be selectively etched with respect to subsequently-deposited spacer materials. Use of a DARC for the second hard mask layer 110 can be particularly advantageous for forming patterns having pitches near the resolution limits of a photolithographic technique. In particular, a DARC can enhance resolution by reducing light reflections, thus increasing the precision with which photolithography can define the edges of a pattern. The second hard mask layer 110 is omitted in embodiments wherein the first hard mask layer 108 can be etched selectively with respect to subsequently deposited spacer materials. In still other embodiments, the second hard mask layer 110 is replaced with an organic spin on antireflective coating ("ARC") positioned between the first hard mask layer 108 and the subsequently described overlying array photoresist layer.

[0050] An array photoresist layer 111, also referred to herein as a mandrel layer, is formed over the second hard mask layer 110. The array photoresist layer 111 preferably comprises photosensitive material, such as a photoresist material that is compatible with 157 nm, 193 nm, 248 nm or 365 nm wavelength systems, 193 nm wavelength immersion systems, extreme ultraviolet systems such as 13.7 nm wavelength systems, or electron beam lithographic systems. Examples of

preferred photoresist materials include argon fluoride sensitive photoresist (that is, photoresist suitable for use with an argon fluoride light source) and krypton fluoride sensitive photoresist (that is, photoresist suitable for use with a krypton fluoride light source). Argon fluoride photoresists are preferably used with shorter wavelength photolithography systems, such as 193 nm wavelength systems. Krypton fluoride photoresists are preferably used with longer wavelength photolithography systems, such as 248 nm wavelength systems. In a modified embodiment, the array photoresist layer 111 comprises a photoresist material that can be patterned by nano-imprint lithography, such as by using a mold or a mechanical force to pattern the photoresist material.

[0051] In general, the materials for the first hard mask layer 108, the second hard mask layer 110, and the array photoresist layer 111 are chosen based on the chemistry and the process conditions for the various pattern forming and transfer steps disclosed herein. For instance, in an example embodiment, the first hard mask layer 108, the second hard mask layer 110, and the array photoresist layer 111 can each be selectively etched with respect to each other. As used herein, a material is considered "selectively etched" (or "preferentially etched") when the etch rate for that material is greater than that for a neighboring material. For example, in certain embodiments, a "selectively etchable" material has an etch rate that is at least about 2 times greater, at least about 10 times greater, at least about 20 times greater, or at least about 40 times greater than that for a neighboring material. In modified embodiments other layers are added if suitable other materials, chemistries and/or processes conditions are used.

[0052] The first hard mask layer 108, the second hard mask layer 110, and the array photoresist layer 111 can be formed using deposition processes such as spin-on coating, sputtering, chemical vapor deposition ("CVD"), or atomic layer deposition. For example, a low temperature CVD process (less than about 550°C, less than about 450°C, or even less than about 400°C) advantageously reduces chemical and/or physical disruption of an amorphous carbon layer, and thus is useful for deposition of materials over an existing amorphous carbon layer, such as the first hard mask layer 108. Additional information regarding the formation of

amorphous carbon layers, including doped amorphous carbon layers, is provided in U.S. Patent 6,573,030 (issued 3 June 2003) and U.S. Patent Application Publication 2005/0042879 (published 24 February 2005). The entire disclosure of this patent and patent application publication is hereby incorporated by reference herein.

[0053] The thicknesses of the first hard mask layer 108, the second hard mask layer 110, and the array photoresist layer 111 are also chosen depending upon compatibility with the etch chemistries and process conditions disclosed herein. For example, when etching a material through a mask of another material, such as when transferring a pattern from an overlying layer to an underlying layer by selectively etching the underlying layer, materials from both layers are removed to some degree. Thus, the upper layer is preferably sufficiently thick such that it is not completely worn away over the course of the pattern transfer. In an example embodiment, the second hard mask layer 110 is preferably between about 10 nm and about 40 nm thick, and is more preferably between about 15 nm and about 30 nm thick.

[0054] The thickness of the array photoresist layer 111 depends on the wavelength of light used to pattern the array photoresist layer 111. In an example embodiment wherein 248 nm light is used to perform photolithography, the array photoresist layer 111 is preferably between about 50 nm and about 300 nm thick, and is more preferably between about 200 nm and 250 nm thick. This height can vary depending upon the wavelength of light used to pattern the photoresist layer. Because lines are subsequently formed in the array photoresist layer 111, in certain embodiments the height of the array photoresist layer 111 is limited by the structural integrity and the aspect ratio of the lines to be formed, since tall spacer lines may collapse or otherwise deform.

[0055] As illustrated in Figures 3A and 3B, a pattern is defined in the array photoresist layer 111 that comprises trenches 122 delimited by lines 124. In some embodiments this pattern can be found anywhere on the substrate; defining the pattern in the array region merely represents a particular embodiment with particular advantages. The trenches 122 can be formed by, for example, photolithography with 248 nm or 193 nm light, in which the array photoresist layer 111 is exposed to

radiation through a reticle and then developed. After being developed, the remaining photodefinable material, which is photoresist in the illustrated embodiment, forms mask features such as the illustrated lines 124. In other embodiments, maskless lithography, or maskless photolithography can also be used to define the lines 124.

[0056] The pitch of the resulting lines 124 is equal to the sum of the width of a line 124 and the width of a neighboring trench 122. To reduce the dimensions of features formed using this pattern of lines 124 and trenches 122, the pitch can be at or near the limits of the photolithographic technique used to pattern the array photoresist layer 111. For example, for photolithography using 248 nm light, the pitch of the lines 124 is preferably between about 80 nm and about 150 nm, and is more preferably between about 90 nm and about 120 nm. Thus, in an example embodiment the pitch is the minimum pitch of the photolithographic technique and the subsequently-formed pitch multiplied spacer pattern advantageously has a pitch below the minimum pitch of the photolithographic technique. In alternative embodiments, because the margin of error for position and feature size typically increases as the limits of a photolithographic technique are approached, the lines 124 are formed having larger feature sizes, such as 200 nm, to reduce errors in the positions and sizes of the lines 124.

[0057] As illustrated in Figures 4A and 4B, the trenches 122 are preferably widened by etching the lines 124, to form modified trenches 122' and modified lines 124'. The lines 124 are preferably etched using a isotropic etch to "shrink" these features. Suitable etches include etches using an oxygen-containing plasma, such as a $SO_2/O_2/N_2/Ar$ plasma, a $C\ell_2/O_2/He$ plasma, or a $HBr/O_2/N_2$ plasma. The extent of the etch is preferably selected so that the width of the modified lines 124' is substantially equal to the desired spacing between subsequently-formed pitch doubled features. For example, in an example embodiment the width of the lines 124 is reduced from between about 80 nm and about 120 nm to between about 35 nm and about 70 nm, and in another embodiment the width is reduced to between about 40 nm and about 50 nm. Advantageously, the width-reducing etch allows the modified lines 124' to be narrower than would otherwise be possible using the

photolithographic technique used to form the lines 124. Additionally, the etch can provide the modified lines 124' with smoothed edges, thus improving the uniformity of the modified lines 124'. While the critical dimensions of the modified lines 124' can be etched below the resolution limits of the photolithographic technique, this etch does not alter the pitch of the modified trenches 122' and the modified lines 124', since the distance between identical points in these features remains the same.

[0058] As illustrated in Figures 5A and 5B, a blanket layer of low temperature spacer material 126 is deposited over the modified lines 124'. In an example embodiment, the low temperature spacer material 126 comprises a layer of oxide material deposited using an atomic layer deposition ("ALD") technique. Generally, photoresist materials are not as tolerant of high temperatures as inorganic or carbon materials. Therefore, forming the spacers from a low temperature oxide material advantageously allows a separate mandrel layer deposition, pattern and transfer to be eliminated, with the patterned array photoresist layer 111 serving the same function. The low temperature spacer material is deposited at less than about 200°C in one embodiment, at less than about 100°C in another embodiment, at less than about 80°C in another embodiment, and at less than about 75°C in another embodiment.

[0059] In an example embodiment, the low temperature spacer material 126 is deposited in an ALD process using $Si_2C\ell_6$, H_2O and C_5H_5N precursors. In such embodiments the spacer material 126 is deposited to a thickness that is between about 20 nm and about 65 nm in one embodiment, between about 25 nm and about 60 nm in another embodiment, and between about 30 nm and about 55 nm in another embodiment. In one embodiment, the spacer material thickness is between about 30 nm and about 40 nm, and in another embodiment, the spacer material thickness is between about 43 nm and about 55 nm. The spacer material deposition rate is between about 1 Å per cycle and about 4 Å per cycle in one embodiment, and is about 2 Å per cycle in another embodiment.

[0060] As illustrated in Figures 6A through 6D, a periphery photoresist layer 128 is optionally deposited in the peripheral region 104, while at least a portion

of the array region 102 is left open. In a preferred embodiment, illustrated in Figure 6B, the periphery photoresist layer 128 is blanket deposited over substantially the entire peripheral region 104. In an alternative embodiment, illustrated in Figure 6C, the periphery photoresist layer 128 is patterned to define periphery features. Example periphery features include landing pads, transistors, local interconnects, and the like. In another alternative embodiment, illustrated in Figure 6D, the periphery photoresist layer 128 is deposited over the looped ends of the low temperature spacer material 126 and the tips 124" of the modified lines 124', thereby blocking the tips 124" of the modified lines 124'. The embodiment illustrated in Figure 6D is particularly advantageous for forming damascene structures because this configuration prevents the looped ends over the low temperature spacer material 126 from being operational during subsequent etching processes.

[0061] In yet another modified embodiment, the second masking step of Figures 6A through 6D is omitted, is conducted at an earlier stage, or is conducted at a later stage. This leaves the spacer material 126 exposed in the peripheral region 104. For example, in one arrangement, the periphery photoresist layer 128 is deposited in the same deposition step in which the array photoresist layer 111 is deposited. In such embodiments, the mask used to pattern the array photoresist layer 111 is configured so as to leave a photoresist pattern or blanket layer in the peripheral region 104. This process results in photoresist being deposited directly on the second hard mask layer 110 in the peripheral region 104, without the intervening spacer material 126.

[0062] As illustrated in Figures 7A and 7B, the low temperature spacer material 126 is then subjected to an anisotropic etch to remove spacer material from horizontal surfaces of the partially formed integrated circuit 100. Such an etch, also known as a spacer etch, can be performed using, for example a $HBr/C\ell_2$-containing plasma. Thus, pitch multiplication has been accomplished to form spacers 130. In the illustrated embodiment, the pitch of the spacers 130 is roughly half that of the photoresist lines 124 and trenches 122 (see Figures 3A and 3B) originally formed by photolithography. Where the photoresist lines 124 had a pitch of about 200 nm, spacers 130 having a pitch of about 100 nm or less (for a width of about 50 nm) can

be formed. Because the spacers 130 are formed on the sidewalls of the modified lines 124', the spacers 130 generally follow the outline of the pattern of modified lines 124' in the first or array photoresist layer 111, and thus typically form a closed loop as illustrated in Figure 7B. However, in general, the configuration of the spacers 130 depends on the absence or presence and pattern of the second photoresist layer 128 (see discussion of Figures 6A through 6D and variations, above).

[0063] As illustrated in Figures 8A and 8B, the remaining exposed photoresist material is selectively etched from the partially formed integrated circuit 100. This includes the first or array photoresist layer 111, as well as any second or periphery photoresist material 128. This results in the formation of freestanding spacers 130 separated by modified trenches 122'. The periphery features are now defined by any remaining low temperature spacer material 126 in the peripheral region 104. Thus, the array photoresist layer 111 is used as a mandrel to form the spacers 130. The photoresist material is selectively removed using an organic strip process. Preferred etch chemistries include an oxygen-containing plasma etch, such as an etch using SO_2. In embodiments wherein the peripheral photoresist layer 128 is deposited directly on the second hard mask layer 110, the photoresist material is selectively etched from only the array region 102 of the integrated circuit 100. Alternatively, in such embodiments the photoresist material is etched from both the array region 102 and the peripheral region 104, followed by a subsequent deposition of photoresist material in the peripheral region 104. In embodiments wherein the peripheral photoresist layer is omitted, the hard mask layer 110 is exposed in the peripheral array region 104.

[0064] After the freestanding spacers 130 are formed, subsequent processing steps can be conducted, such as a dry develop step and an *in situ* etch step. The subsequent processing steps can be used to transfer the pattern of spacers 130 and periphery features to the underlying first hard mask layer 108 and/or the second hard mask layer 110, as illustrated in Figures 9A and 9B. Specifically, Figures 9A and 9B illustrate the pattern of spacers 130 defined in the first hard mask layer 108 and the second hard mask layer 110. The second hard

mask layer 110 is optionally etched from the structure illustrated in Figures 9A and 9B. This pattern can then be transferred into the underlying substrate 106 by etching of the underlying substrate 106. The structure can also be otherwise processed (such as by doping, oxidizing, nitridizing, or selectively depositing) through the pattern defined in the first hard mask layer 108 and/or the second hard mask layer 110. As noted herein, the substrate 106 can include previously deposited layers, such as insulating layers for damascene metallization, or metal layers for conventional metallization.

[0065] Certain of the techniques disclosed herein advantageously enable the formation of a pitch doubled pattern of spacers without the use of additional layers to define the array features, such as a top carbon layer and an amorphous silicon layer. Specifically, by forming low temperature oxide spacers directly on the array photoresist layer 111 as disclosed herein, the photosensitive or photoresist material itself can be used to define mandrels which are used in a subsequent pitch multiplication technique. This advantageously eliminates the need to pattern additional masking layers to define mandrels. Such techniques advantageously allow process steps associated with such additional masking layers to be eliminated, such as additional dry develop steps and hard mask etch steps. Furthermore, such techniques also advantageously allow the periphery photoresist layer 128 to be defined using the same low temperature spacer material that is used to form the spacers in the array region. Certain of the embodiments disclosed herein also advantageously allow a hard mask material—as compared to a more vulnerable photoresist material—to be used to block and define features in the peripheral region 104 without requiring the use of a separate hard mask layer.

SCOPE OF THE INVENTION

[0066] While the foregoing detailed description discloses several embodiments of the present invention, it should be understood that this disclosure is illustrative only and is not limiting of the present invention. It should be appreciated that the specific configurations and operations disclosed can differ from those

described above, and that the methods described herein can be used in contexts other than integrated circuit fabrication.

WE CLAIM:

1. A method for fabricating a semiconductor device, the method comprising:

patterning a layer of photoresist material to form a plurality of mandrels;

using an atomic layer deposition technique to deposit an oxide material onto the plurality of mandrels;

anisotropically etching the oxide material from exposed horizontal surfaces; and

etching the photoresist material selectively with respect to the oxide material, thereby forming a plurality of oxide spacers.

2. The method of Claim 1, wherein the oxide material is deposited using a precursor selected from the group consisting of $Si_2C\ell_6$, H_2O and C_5H_5N.

3. The method of Claim 1, wherein:

the plurality of mandrels are formed in a device array region; and

the oxide material is also deposited over a device peripheral region.

4. The method of Claim 3, further comprising forming a pattern of photoresist material over the oxide material in the device peripheral region.

5. The method of Claim 4, wherein etching the photoresist material selectively further comprises etching photoresist material from the device peripheral region selectively.

6. The method of Claim 1, further comprising isotropically etching the plurality of mandrels to form a plurality of modified mandrels before depositing the oxide material.

7. The method of Claim 6, wherein isotropically etching the plurality of mandrels comprises using an oxygen-containing plasma selected from the group consisting of a $SO_2/O_2/N_2/Ar$ plasma, a $C\ell_2/O_2/He$ plasma, and a $HBr/O_2/N_2$ plasma.

8. The method of Claim 6, wherein the modified mandrels have a width between about 35 nm and about 70 nm.

9. The method of Claim 1, wherein patterning the layer of photoresist comprises using nano-imprint lithography.

10. The method of Claim 1, wherein anisotropically etching the oxide material comprises using a $HBr/C\ell_2$-containing plasma.

11. The method of Claim 1, wherein the oxide material is deposited at a temperature less than about 100°C.

12. The method of Claim 1, wherein the oxide material is deposited at a temperature less than about 80°C.

13. The method of Claim 1, wherein the layer of photoresist material is patterned over a hard mask layer.

14. The method of Claim 1, wherein the layer of photoresist material is patterned over a silicon oxynitride layer that is positioned over a carbon layer.

15. The method of Claim 1, wherein the plurality of mandrels have a height between about 50 nm and about 300 nm.

16. The method of Claim 1, wherein the layer of photoresist material comprises a material selected from the group consisting of amorphous carbon, argon fluoride photoresist, and krypton fluoride photoresist.

17. A method of forming a memory device, the method comprising:

forming a plurality of mandrels over a substrate, the mandrels separated by exposed portions of the substrate;

depositing a spacer material over the mandrels and over the exposed portions of the substrate using an atomic layer deposition technique conducted at a temperature less than about 100°C; and

anisotropically etching the spacer material from (a) exposed horizontal surfaces of the plurality of mandrels and (b) the exposed portions of the substrate, thereby leaving spacer material remaining on vertical sidewalls of the plurality of mandrels.

18. The method of Claim 17, wherein the substrate includes a hard mask directly under the spacer material.

19. The method of Claim 17, further comprising removing the plurality of mandrels, thereby leaving a pattern of spacers positioned over the substrate.

20. The method of Claim 19, wherein the spacers comprising the pattern of spacers have a width of about 50 nm or less.

21. The method of Claim 19, wherein the spacer material is deposited to a thickness *x* over the mandrels, and wherein the spacers comprising the pattern of spacers comprising the pattern of spacers have a width *x*.

22. The method of Claim 19, further comprising transferring the pattern of spacers into an amorphous carbon hard mask.

23. A method of forming an integrated circuit, the method comprising:

forming a plurality of mandrels on a hard mask layer, wherein the mandrels comprise a photosensitive material;

depositing a spacer material using an atomic layer deposition technique, wherein the spacer material covers the plurality of mandrels;

anisotropically etching the spacer material from horizontal surfaces, thereby exposing photosensitive material;

removing exposed photosensitive material after anisotropically etching the spacer material, thereby leaving a pattern of spacers on the hard mask layer;

transferring the pattern of spacers to the hard mask layer; and

etching the pattern of spacers from the hard mask layer.

24. The method of Claim 23, wherein the hard mask layer comprises carbon.

25. The method of Claim 23, wherein:

the mandrels are formed in an array region of the integrated circuit; and

the spacer material is deposited over (a) the array region of the integrated circuit and (b) a peripheral region of the integrated circuit, the peripheral region surrounding the array region.

26. The method of Claim 25, further comprising:

forming a pattern of photosensitive material over the spacer material in the peripheral region before anisotropically etching; and

removing exposed photosensitive material from the peripheral region after anisotropically etching the spacer material.

27. The method of Claim 23, wherein the hard mask layer comprises carbon and a material selected from the group consisting of silicon, silicon nitride and silicon oxynitride.

28. The method of Claim 23, wherein the hard mask layer is positioned over a semiconductor substrate.

29. The method of Claim 23, wherein the spacer material is deposited at a temperature less than about 100°C.

30. The method of Claim 23, further comprising isotropically etching the plurality of mandrels before depositing the spacer material.

31. A method of integrated circuit fabrication, the method comprising:

using a lithographic technique to define a plurality of elongate mandrels over a hard mask layer, wherein the mandrels comprise a photoresist material; and

forming a pattern of spacers around the mandrels, wherein:

the pattern of spacers has a pitch that is smaller than a minimum resolvable pitch of the lithographic technique,

the pattern of spacers is formed from an oxide material, and

the pattern of spacers is deposited using an atomic layer deposition technique at a temperature less than about 100°C.

32. The method of Claim 31, wherein the pattern of spacers is deposited at a temperature less than about 80°C.

33. The method of Claim 31, wherein the pattern of spacers is deposited at a temperature less than about 30°C.

34. The method of Claim 31, further comprising transferring the pattern of spacers into the hard mask layer.

35. The method of Claim 34, wherein transferring the pattern of spacers into the hard mask layer further comprises exposing a portion of a substrate that underlies the hard mask layer.

36. The method of Claim 31, wherein the pattern of spacers comprises a pattern of spacer loops formed around the mandrels.

37. The method of Claim 31, wherein the hard mask layer comprises a material selected from the group consisting of silicon, silicon nitride and silicon oxynitride.

38. The method of Claim 31, wherein the hard mask layer comprises a dielectric antireflective coating.

39. The method of Claim 31, wherein the hard mask layer comprises an organic antireflective coating.

40. The method of Claim 31, wherein the hard mask layer is formed over a semiconductor substrate.

41. The method of Claim 31, wherein the hard mask layer is formed over a semiconductor substrate and an amorphous carbon layer.

42. The method of Claim 31, wherein the mandrels have a height between about 50 nm and about 300 nm.

43. The method of Claim 31, wherein the mandrels have a height between about 200 nm and about 250 nm.

44. The method of Claim 31, wherein the mandrels comprise a material selected from the group consisting of amorphous carbon, argon fluoride photoresist, and krypton fluoride photoresist.

45. The method of Claim 31, wherein the pattern of spacers has a pitch between about 70 nm and about 120 nm.

46. The method of Claim 31, wherein the patterns has a pitch between about 80 nm and about 100 nm.