METHOD FOR FORMING A RELEASED MICROSTRUCTURE SUITABLE FOR A MICROELECTROMECHANICAL DEVICE

Technical Field

The present invention relates to microstructures for microelectromechanical (MEMS) devices and, in particular, relates to a method for forming a released microstructure suitable for a MEMS device.

Background Art

MEMS devices are integrated micro devices or systems combining electrical and mechanical components. They are normally made using integrated circuit (IC) batch processing techniques and can range in size from micrometres to millimetres. These devices can sense, control and actuate on the micro scale, and can function individually or in arrays to generate effects on the macro scale. Micromachines consist of sensors and actuators. Sensors provide an electrical output in response to a signal. For example, sensors may be used to measure acceleration, pressure, speed, flow, density, light intensity, temperature or chemical content. Actuators convert an electrical signal into an action. For example, an actuator may take the form of an electrostatic rotary motor, an electrostatic linear motor or a supersonic motor.

Known manufacturing methods for forming microstructures for MEMS devices have a number of known problems. One of these problems is stiction, the permanent sticking of the microstructures to the substrate. As the microstructures are designed to be movable, stiction can induce noise and unwanted non-linear motion when the MEMS device is used.

Stiction may occur during the manufacture of the microstructures, such as in "after-rinse stiction" when sacrificial wet etching is used to release the microstructures. It may also occur when the MEMS device is in use. This "in-use stiction" may be caused by high electrostatic forces or large shocks.

In known microstructure releasing techniques, the released microstructure always remains a short distance from the substrate, so it is very difficult to completely ensure that the microstructure and the substrate never come into contact with one another. Such known microstructure release techniques can never completely overcome the problem of stiction.

Another problem of known microstructure manufacturing methods is the damage caused by probe testing. In such methods, in order to tell if the movable microstructures have been released, the microstructures need to be physically probed to see if they move. Such probing can damage the delicate structures, may create undetectable stiction points and may introduce electrical shorting which affects the performance of the MEMS device.

The present inventors have now devised a new method for forming released microstructures suitable for MEMS devices.

Disclosure of Invention

In a first aspect, the present invention provides a method for forming a released microstructure suitable for a microelectromechanical device, the method comprising the steps of:

(a) providing a multi-layered wafer comprising:

(i) a device layer having an outer surface;

(ii) a substrate layer having an outer surface; and

(iii) an intermediate layer disposed between the device layer and the substrate layer, the intermediate layer being adapted to resist removal by a first removal technique;

(b) forming a microstructure in the device layer by removing portions of the device layer using a first removal technique;

(c) releasing the microstructure by using a second removal technique to selectively remove:

(i) portions of the substrate layer which lie below the microstructure, the removal process beginning at the substrate layer surface and moving towards the intermediate layer; and

(ii) portions of the intermediate layer which lie below the microstructure.

The first removal technique comprises:

(a) forming a first masking layer on the outer surface of the device layer, the first masking layer being patterned to reveal those portions of the outer surface of the device layer immediately surrounding the microstructure to be formed; and

(b) etching away the revealed portions of the device layer, the etching technique beginning at the outer surface of the device layer and moving towards the intermediate layer to form the microstructure.

The device layer comprises at least one silicon wafer and the step of etching away the revealed portions of the device layer comprises etching using deep silicon wafer etching (DRIE).

The step of forming the first masking layer on the outer surface of the device layer comprises:

(a) growing a first layer of oxide on the outer surface of the device layer; and

(b) etching away portions of the first oxide layer to reveal those portions of the outer surface of the device layer that immediately surround the microstructure to be formed.

The step of etching away portions of the first oxide layer comprises dry etching techniques to form substantially straight side walls in the etched-away portions of the first oxide layer.

The first oxide layer comprises a layer of silicon dioxide.

The step of selectively removing portions of the substrate layer which lie below the microstructure comprises:

(a) forming a second masking layer on the outer surface of the substrate layer, the second masking layer being patterned to reveal those portions

of the outer surface of the substrate layer which lie below the microstructure; and

(b) etching away the revealed portions of the substrate layer, beginning at the outer surface of the substrate layer and moving towards the intermediate layer

to provide a partial release hole below the microstructure which reveals those portions of the intermediate layer which lie below the microstructure.

The substrate layer comprises at least one silicon wafer and the step of etching away the revealed portions of the substrate layer comprises etching using deep silicon wafer etching (DRIE).

The step of forming the second masking layer on the outer surface of the substrate layer comprises:

(a) growing a second layer of oxide on the outer surface of the substrate layer; and

(b) etching away portions of the second oxide layer to reveal those portions of the outer surface of the substrate layer which lie below the microstructure.

The step of etching away portions of the second oxide layer comprises dry etching techniques to form substantially straight side walls in the etched-away portions of the second oxide layer.

The second oxide layer comprises silicon dioxide.

The intermediate layer has a first surface touching the substrate layer, and a second surface touching the device layer and wherein the step of selectively removing portions of the intermediate layer which lie below the microstructure comprises etching away the revealed portions of the intermediate layer, beginning at the first surface of the intermediate layer and moving towards the second surface of the intermediate layer to provide a complete release hole below the microstructure, thereby releasing the microstructure.

The step of etching away the revealed portions of the intermediate layer comprises dry etching techniques to form substantially straight side walls in the etched-away portions of the intermediate layer.

The device layer comprises a silicon wafer which is about 20 to 40 μm thick.

The substrate layer comprises a silicon wafer which is about 300 to 400 μm thick.

The intermediate layer comprises a layer of thermal oxide which is about 2 to 3 μm thick.

Preferably, the step of releasing the microstructure is performed before the step of forming the microstructure, i.e. the microstructure is partially released before the step of forming the microstructure.

Alternatively, the step of releasing the microstructure is performed after the step of forming the microstructure.

In a second aspect the present invention provides a released microstructure suitable for a microelectromechanical device when formed according to the first aspect of the present invention.

In a third aspect the present invention provides a multi-layered wafer incorporating a released microstructure suitable for a microelectromechanical device when formed according to the first aspect of the present invention.

Throughout this specification, unless the context requires otherwise, the phrase "portions ... which lie below the microstructure" will be understood to imply those portions which lie below the microstructure when the multi-layered wafer is oriented in a horizontal plane with the device layer positioned above the substrate layer.

Throughout this specification, unless the context requires otherwise, the word "comprise", or variations such as "comprises" or "comprising", will be understood to imply the inclusion of a stated element, integer or step, or group of elements, integers or steps, but not the exclusion of any other element, integer or step, or group of elements, integers or steps.

Any discussion of documents, acts, materials, devices, articles or the like which has been included in the present specification is solely for the purpose of providing a context for the present invention. It is not to be taken as an admission that any or all of these matters form part of the prior art base or were common general knowledge in the field relevant to the present invention as it existed before the priority date of each claim of this application.

In order that the present invention may be more clearly understood, preferred forms will be described with reference to the following drawings and examples.

Brief Description of the Drawings

Figure 1 is a flow chart illustrating the steps involved in the method for forming a released microstructure suitable for a microelectromechanical device according to the present invention;

Figures 2-6 are perspective views of multi-layered wafers used in the preferred method of the present invention;

Figures 7-9 are inverse perspective views of multi-layered wafers used in the method according to the present invention;

Figure 10 is a perspective view of a multi-layered wafer used in the preferred method of the present invention; and

Figures 11-19 are cross-sectional side views of multi-layered wafers used to form a released microstructure according to a second preferred embodiment of the present invention.

Detailed Description

The present invention provides a method for forming a released microstructure suitable for a microelectromechanical device. The first preferred method involves a number of steps. As shown in Figures 1 and 2, the first step involves providing 1 a multi-layered wafer 2. The wafer has a device layer 3 having an outer surface 4, a substrate layer 5 having an outer surface 6, and an intermediate layer 7. The intermediate layer 7 is disposed between the device layer 3 and the substrate layer 5 and is adapted to resist removal by a first removal technique. The device layer 3 and the substrate layer 5 are both silicon wafers, the substrate layer 5 being significantly thicker than the device layer 3.

Turning to Figures 1 and 3, the next step involves forming 8 a microstructure 9 in the device layer 3. The step of forming 8 a microstructure 9 in the device layer 3 involves a number of subsidiary steps. The first of these involves forming a first masking layer 23 on the outer surface 4 of the device layer 3. As shown in Figure 3, this involves growing a first layer of oxide 10 on the outer surface 4 of the device layer 3. The first oxide layer 10 is a layer of silicon dioxide.

The next step in forming the first masking layer 23 is shown in Figure 4 and involves etching away portions of the first oxide layer 10 to reveal those portions 11 of the outer surface 4 of the device layer 3 which immediately surround the microstructure 9 to be formed. This etching step is performed using dry etching to form straight side walls 12 in the etched-away portions of the first oxide layer 10.

Turning to Figure 5, the next step involves etching away the revealed portions 11 of the device layer 3. This etching technique should begin at the outer surface 4 of the device layer 3 and move towards the intermediate layer 7, to form the microstructure 9. This etching step is performed using deep silicon wafer etching (DRIE) all the way through to the intermediate layer 7. Because the intermediate layer 7 is formed of a material, such as silicon dioxide, which is adapted to resist removal by DRIE the intermediate layer 7 remains substantially intact throughout the DRIE process. Due to the DRIE etching process, the microstructure 9 has substantially straight side walls.

As shown in Figure 1, the next step involves releasing 13 the microstructure 9 using a second removal technique.

This second removal technique usually involves a number of steps. Turning to Figure 6, the first step involves forming a second masking layer 24 on the outer surface 6 of the substrate layer 5. This involves growing a second layer of oxide 14 on the outer surface 6 of the substrate layer.

Figure 7 is a perspective view of the multi-layered wafer with the wafer inverted, so that the substrate layer 5 now appears above the device layer 3. As shown in Figure 7, the next step involves etching away portions of the second oxide layer 14 to reveal those portions 15 of the outer surface 6 of the substrate layer 5 which lie below the microstructure 9. The etching away of the portions of the second oxide layer 14 is done using dry etching techniques to form substantially straight walls 16 in the etched-away portions of the second oxide layer 14.

Once the second masking layer 24 has been patterned in this way, the next step involves etching away the revealed portions 15 of the substrate layer 5, beginning at the outer surface 6 of the substrate layer and moving towards the intermediate layer 7. This etching step is done using DRIE etching and serves to form a partial release hole 17 in the substrate layer 5, as shown in Figure 8.

If the multi-layered wafer 2 is oriented in a horizontal plane, such as that shown in Figure 6, with the device layer 3 positioned above the substrate layer 5, the partial release hole 17 is positioned below the microstructure 9.

By forming the partial release hole 17 in the substrate layer 5, this reveals portions of the intermediate layer 7 which also lie below the microstructure 9.

The next step, shown in Figure 9, involves dry etching away the revealed portions of the intermediate layer 7, beginning at the substrate layer 5 side of the intermediate layer and moving towards the device layer 3 side. When the revealed portions 18 of the intermediate layer 7 are dry-etched away, the partial release hole 17 becomes a complete release hole 17 and the microstructure 9 is released.

In this way, the microstructure 9 is formed in the device layer 3 by DRIE etching from one side of the multi-layered wafer 2 and then, from the other side of the wafer 2, forming a release hole 17 below the microstructure 9 by DRIE etching away those portions of the substrate layer 5 which lie below the microstructure 9, and dry etching the corresponding revealed portions 18 of the intermediate layer 7, thereby producing a released microstructure 9, as shown in Figure 10.

Although not shown in Figure 10, once the microstructure 9 has been released, the first 10 and second 14 oxide layers should then be removed using an appropriate oxide removal technique.

As shown in Figure 10, the end product is a multi-layer wafer 2 incorporating a released microstructure 9 suitable for a microelectromechanical device. The multi-layer wafer 2 has a device layer 3 with the microstructure 9 formed therein, a substrate layer 5 having a release hole 17 below the microstructure 9, and an intermediate layer 7 abuttingly disposed between the device layer 3 and the substrate layer 5. The intermediate layer 7 is formed from an oxide material and has a release hole below the microstructure 9.

A second preferred embodiment will now be described with reference to Figures 11 to 19 which are cross-sectional side views of a multi-layered wafer 2 having a microstructure 9 formed therein according to a second preferred embodiment of the present invention. Features identified with numeral references common to those of Figures 1-9 are intended to refer to common features.

Referring to Figure 11, the first step in the second preferred method involves providing a multi-layered wafer 2 made up of a silicon device layer 3 and a silicon substrate layer 5. An embedded intermediate layer 7 made of thermal oxide, isolates the device 3 and substrate 5 layers.

As shown in Figure 11, the first step in the second preferred method involves growing first 10 and second 14 oxide layers on both sides of the wafer 2. These oxide layers serve as masks during deep silicon wafer etching (DRIE). On the device layer 3 side of the wafer 2, DRIE is used to etch

microelectricalmechanical structures 9 (not shown). On the substrate layer 5 side of the wafer 2, DRIE is used to etch release holes 17 (not shown).

The minimum thickness of the first 10 and second 14 oxide layers is determined by the selectivity of silicon and oxide during the deep silicon wafer etching. The thickness of these oxide layers is not critical and they may be thicker than the required minimum thickness. The inventors have found that a 250 nm thick first oxide layer 10 is suitable to allow deep silicon wafer etching through the device layer 3. The device layer is 20-40 μm thick.

The inventors have found that substrate layers 5 of 300-400 μm are suitable. The intermediate thermal oxide layer 7 should be about 2-3 μm thick.

In this example, 0.2-0.3 μm thick thermal oxide is grown on both sides of the wafer to form the first 10 and second 14 oxide layers. The first oxide layer 10 is used as a first masking layer 23 to pattern the device layer 3. This masking layer 23 is preferably relatively thin so that small shapes may be easily formed via lithography. In this way, precise features on the first masking layer 23 can be dry-etched in a short period of time.

As will be shown in subsequent figures, the second oxide layer 14 is combined with a thick resist layer 19 to form a second masking layer 24 to allow deep silicon etching of the substrate layer 5. By adding a resist layer 19 greater than 10 μm thick, the masking layer 14 is durable enough to allow etching through the entire substrate layer 5. The selectivity of resist to silicon is greater than 1:70. In order to increase this selectivity, the resist should be baked for a sufficient period of time before DRIE. If it is not baked, the outer surface 6 of the substrate layer 5 can be exposed to the plasma through cracks in the resist. If cracks or pin holes form in the resist, the surrounding portions of the resist flake away, resulting in rapid removal of the substrate layer 5 beneath. In addition, the flaked portions of the resist layer 19 may get into the etching area and act as micro-masks. If this occurs, the wafer surface could become rough and turn black. The resist should therefore be baked in order to avoid such problems.

Turning to Figure 12, the next step is a metallisation step in which electrodes and alignment marks are created on the device layer side of the wafer 2. Aluminium or gold may be used for the electrodes. Aluminium is commonly used in integrated circuit and MEMS applications. Aluminium is one of the few films which is readily accepted in the silicon deep etcher. Gold may also be chosen due to its low Au/Si contact resistance, its clean surface which resists oxidation, and also its resistance to attack by acid. However, exposed gold in the plasma may cause contamination in a deep silicon etcher. Because of these concerns, gold evaporation may be performed as the last step in the preferred method.

Figure 12 shows the electrodes 20 formed at the outer surface 4 of the device layer, but does not show the alignment marks created in the first oxide layer 10.

The next step involves vapour priming the wafer and spinning and baking a photoresist onto both sides of the wafer. The photoresist is then baked on. The purpose of the photoresist on the second oxide layer 14 side of the wafer 2 is to protect that oxide from etching when wet etching is used to remove the oxide. The thickness and type of photoresist is not particularly critical as the selectivity between resist and oxide in wet etching is high.

The resist on the first oxide layer 10 is exposed, developed and descumed using lithographic processes. This step is relatively simple due to the large bond pad shapes and alignment marks. The next step involves wet etching the exposed portions of the first oxide layer 10 by dipping the entire wafer 2 into buffered hydrofluoric acid (HF). The photoresist coating of the second oxide layer 14 protects that layer and the exposed regions of the first oxide layer 10 are removed by the wet etching process.

After this oxide etching step, a thin layer of aluminium (about 100-200nm) is evaporated onto the entire surface of the wafer 2. The wafer 2 is then immersed in acetone for seven hours or more in order to dissolve the photoresist. In this way, the photoresist, and the layer of aluminium which coats it, is removed, but the layer of aluminium on the exposed regions of the outer surface 4 of the silicon device layer 3 remains.

The next step involves ultrasonically cleaning the wafer in order to remove unwanted residual metal and resist particles.

The next step involves inserting the wafer into an annealing furnace having a hydrogen environment in order to form ohmic contacts between the aluminium and the silicon. This annealing step should only take about ½ an hour.

Turning to Figure 13, the next step involves depositing a third oxide layer 21 on the device layer side of the wafer 2 in order to cover the bonding pads and alignment marks. This deposition step is preferably performed using plasma-enhanced chemical vapour deposition (PECVD). This step is performed in order to cover the metal layer to prevent it from contamination when in the plasma. The thickness to which this third oxide layer 21 should be applied is determined by the selectivity of silicon and silicon oxide during the deep silicon etching to be performed. As an example, in a basic process flow, 150-200 nm thick PECVD oxide is sufficient to protect the metal layer when etching the silicon up to 40 μm thick. The thickness of this third oxide layer 21 should be kept to a minimum since the first 10 and third 21 oxide layers combine for use as a first masking layer 23 in order to form fine features in the device layer 3. If the third oxide layer 21 is both smooth and thin, this can make it easier in the lithography and etching steps.

Turning to Figure 14, the next step involves patterning the first masking layer 10 in the shape of the microstructure to be formed. This patterning step is done using standard lithography and etching processes. If lithography is used, the wafer 2 is aligned to the alignment marks formed from the aluminium. In this step, the metal should be aligned with the trenches that define the bonding pad area. If etching is used, dry etching should be used to create straight side walls 12 in the first oxide layer 10. The resulting patterned first masking layer 23 is used as a mask for DRIE in the next step.

As seen in Figure 14, this patterning step reveals exposed portions 11 of the outer surface 4 of the device layer 3. These exposed portions 11 are those portions immediately surrounding the microstructure 9 to be formed.

Turning to Figure 14, the next step involves patterning the second oxide layer 24 to reveal portions 15 of the outer surface 6 of the substrate layer 5 which lie below the microstructure 9 to be formed. This patterning step is performed using lithography, alignment, pattern transfer and removal of the silicon dioxide in the second oxide layer 14. This process leaves the second oxide layer having substantially straight inner walls 16.

The wafer 2 is then primed and a resist layer 19 is spun and baked onto both sides of the wafer 2. The resist on the device layer 3 side of the wafer is there to protect the outer surface 4 of the device layer 3, helping to keep it free of contamination. It is also used to protect the first masking layer 23 if a wet etching method is applied.

The resist layer 19 on the substrate layer side of the wafer 2 is used for alignment and lithography. The alignment is conducted using a standard alignment tool. Because the alignment marks on the device layer side of the wafer may have large dimensions, either digital alignment or infrared alignment may be used. The alignment errors used in these techniques are negligible when compared with misalignment allowance in the designs. The resist is then baked hard. The exposed portions of the second oxide layer 14 are removed using dry etching. If wet etching is used, without polishing the substrate layer side of the wafer 2, it is difficult to remove the second oxide layer 14.

Turning to Figure 16, the thick resist layer 19 and second oxide layer 14 act as a second masking layer 24. The second masking layer 24 is used to selectively remove those portions of the substrate layer 5 which lie below the microstructure to be formed, thereby creating a release hole 17 in the substrate layer 5. Because the selectivity between resist 19 and silicon is greater than 1:70 and the selectivity between the second oxide layer 14 and silicon is around 1:200, the silicon in the substrate layer 5 can be removed to a depth of several hundred microns using DRIE. The DRIE process begins at the outer surface 6 of the substrate layer 5 and continues until it reaches the intermediate thermal oxide layer 7.

During the DRIE process it is also useful to form scribing lines of dies in order to facilitate chip dicing and to minimise contamination. By adding scribing lines that are hundreds of micrometres in depth, it is easy to achieve die to die separation without damaging the released microstructures 9. In addition, this also minimises the particles generated during the chip separation process. By adding small bridges to separated scribe lines the potential for wafer breakage is greatly minimised. However, these bridges should not be too wide or they may affect wafer cleavage. In the present example, bridges of around 50 μm have been used.

Once the DRIE step has been performed, a partial release hole 17 is formed in the substrate layer 5 which exposes those portions 18 of the intermediate layer 17 which lie below the microstructure 9 to be formed.

Turning to Figure 17, the next step involves removing those exposed portions 18 of the intermediate layer 7 which lie below the microstructure 9 to be formed. This step is performed using dry oxide etching. If wet etching is used, special care is needed when handling and cleaning the wafer during this stage because the whole wafer is very delicate, particularly once the intermediate layer has been removed. Subsequent water cleaning, air blowing or handling may easily produce cracks in the wafer.

As shown in Figure 17, the next step involves reactive ion etching (RIE) the resist layer 19 from both sides of the wafer. RIE oxide etching for twenty seconds should be sufficient. This RIE etching process also serves to remove any native oxide on the exposed portions 11 of the device layer 3 which immediately surround the microstructure 9 to be formed. If native oxide is present, this can cause unwanted masking due to the very high selectivity of the DRIE etching (around 100:1 for silicon/silicon dioxide). In this way, any small pieces of oxide on the exposed portions 11 of the outer surface of the device layer 3 would act as masks.

The next step involves forming the microstructure 9 in the device layer 3 by removing those portions 11 of the device layer 3 immediately surrounding the microstructure to be formed. This step is performed by DRIE using the first

oxide layer 10 as a first masking layer 23. During this deep silicon etch the pattern in the first masking layer 23 is transferred into the silicon of the device layer 3 by a deep, vertical and isotrophic etch. It is recommended that during the DRIE etching process, the vacuum is not broken. If a vacuum is broken, native oxide may quickly form on the portions of the silicon device layer 3 which are exposed to air. If this occurs, it may severely affect the etching quality.

Helium cooling should be used during the DRIE process. One way to tell when the DRIE etch has gone through the device layer 3 is to detect when the helium pressure drops below a certain predetermined value. This will indicate that the microstructure 9 is at least partially released. As shown in Figure 18, thin silicon bridges 25 (about 10 μm thick) may still connect the microstructures 9 which, naturally, are designed to be moving parts. The existence of these bridges 25 is usually due to differences in etch rates and etch uniformity variations called "loading effects".

A number of techniques were tried in order to remove the final silicon bridges 25 between the microstructures 9 being formed. One such method involved continuing the DRIE process with the helium cooling turned off. This method did not produce good results and a lot of springs were broken during the process. This is because without helium cooling, the etch rate increases and the direction of the etching becomes hard to control. In addition, without helium cooling, the temperature in the chamber increases significantly, electrical charge accumulates, and the resulting heat and electrical charge may damage the released microstructures 9.

An alternative method was used which served the purpose of recreating the vacuum seal to allow the DRIE process to be performed with helium cooling. As shown in Figure 18, this is performed by attaching a seal-forming substrate 27 to the substrate layer 5. This is done by spinning an adhesive resist 26 onto the substrate layer 5. Standard exposure and development steps are then performed and a blank mask is used to remove most of the resist on the wafer, just leaving a small portion of adhesive resist 26 on the edge of the substrate layer 3 for bonding purposes. The seal-forming substrate 27 is then pressed against the adhesive resist 26 on the substrate layer 5 and the entire structure is

pressed together. The combined structure is then put on a hot plate for one minute and force is applied. This hot plate treatment sticks the seal-forming substrate 27 to the substrate layer 5. In this way, the seal-forming substrate 27 allows a vacuum to be formed to allow helium cooling to continue and DRIE etching can be used to remove the silicon bridges 25, thereby releasing the microstructures 9.

As shown in Figure 19, once the microstructures 9 are released, the first masking layer 23 of oxide is removed using RIE, thereby exposing the metal bonding pads 20.

The above method therefore produces a multi-layer wafer 2 incorporating a released microstructure 9 suitable for a microelectromechanical device. The wafer 2 formed in this way can then be diced, wire-bonded and tested. The dicing can be performed by gently pressing the scribing lines.

It will be appreciated from the foregoing discussion that the present invention overcomes, or at least ameliorates a number of the problems of the prior art. The problem of stiction is removed, as the release hole extends right through the intermediate and substrate layers and there is no substrate below the microstructure to which it could stick. In addition, physical probing is not needed to tell if the microstructure has been released. In this method, the releasing step may be visually monitored since the portion of the substrate below the microstructure has been removed and is therefore transparent. Another way to test if the microstructure has been released is to check the resistance between the bonding pads between microstructures which are supposed to be isolated. If the resistance is above the mega ohm range, this clearly indicates that the microstructure has been released. The method of the present invention also has the advantage of producing a high yield with minimum complexity. The process allows ready portability to other foundries. All process steps have a high etch selectivity which is no less than 1:70 and it does not require critical alignment and precision in the exposure techniques during lithographic processes.

It will be appreciated by persons skilled in the art that numerous variations and/or modifications may be made to the invention as shown in the specific embodiments without departing from the spirit or scope of the invention as broadly described. The present embodiments are, therefore, to be considered in all respects as illustrative and not restrictive.

Claims:

1. A method for forming a released microstructure suitable for a microelectromechanical device, the method comprising the steps of:

(a) providing a multi-layered wafer comprising:

(i) a device layer which is about 20 to 40 μm thick comprising at least a single crystal silicon wafer having an outer surface;

(ii) a substrate layer comprising a silicon wafer which is about 300 to 400 μm thick having an outer surface; and

(iii) an intermediate layer which is about 2 to 3 μm thick comprising a layer of thermal oxide disposed between the device layer and the substrate layer, the intermediate layer being adapted to resist removal by a first removal technique;

(b) forming a microstructure in the device layer by removing portions of the device layer using a first removal technique consisting of:

(i) forming a first masking layer on the outer surface of the device layer, the first masking layer being patterned to reveal those portions of the outer surface of the device layer immediately surrounding the microstructure to be formed; and

(ii) etching away the revealed portions of the device layer, the etching technique beginning at the outer surface of the device layer and moving towards the intermediate layer to form the microstructure, wherein the etching uses deep silicon wafer etching (DRIE),

wherein the step of forming the first masking layer on the outer surface of the device layer comprises:

(I) growing a first layer of oxide on the outer surface of the device layer, wherein the first oxide layer comprises a layer of silicon dioxide; and

(II) etching away portions of the first oxide layer to reveal those portions of the outer surface of the device layer that immediately surround the microstructure to be formed,

wherein the step of etching away portions of the first oxide layer comprises dry etching techniques to form substantially straight side walls in the etched-away portions of the first oxide layer; and

(c) releasing the microstructure by using a second removal technique:

(i) to selectively remove portions of the substrate layer which lie below the microstructure by:

(I) forming a second masking layer on the outer surface of the substrate layer, the second masking layer being patterned to reveal those portions of the outer surface of the substrate layer which lie below the microstructure; and

(II) etching away the revealed portions of the substrate layer using deep silicon wafer etching (DRIE), beginning at the outer surface of the substrate layer and moving towards the intermediate layer,

to provide a partial release hole below the microstructure which reveals those portions of the intermediate layer which lie below the microstructure,

wherein the step of forming the second masking layer on the outer surface of the substrate layer comprises:

- growing a second layer of oxide comprising silicon dioxide on the outer surface of the substrate layer; and
- etching away portions of the second oxide layer to reveal those portions of the outer surface of the substrate layer which lie below the microstructure,

wherein the step of etching away portions of the second oxide layer comprises dry etching techniques to form substantially straight side walls in the etched-away portions of the second oxide layer; and

(ii) to selectively remove portions of the intermediate layer which lie below the microstructure by etching away the revealed portions of the intermediate layer using dry etching techniques to form substantially straight side walls in the etched-away portions of the intermediate layer, beginning at a first surface of the intermediate layer touching the substrate layer and moving towards a second surface of the intermediate layer touching the device layer to provide a complete release hole below the microstructure, thereby releasing the microstructure.

2. A method according to claim 1, wherein the microstructure is partially released before the step of forming the microstructure.

3. A method according to claim 1, wherein the step of releasing the microstructure is performed after the step of forming the microstructure.

4. A method according to claim 2, wherein a second oxide layer is combined with a resist layer to form the second masking layer to allow deep silicon etching of the substrate layer.

5. A method according to claim 4, wherein the second oxide layer is 0.2 – 0.3 µm thick and the resist layer is greater than 10 µm thick.

6. A method according to any of claims 1 to 5, wherein a further step is a metallization step in which electrodes and alignment marks are created on the device layer of the wafer.

7. A method according to claim 6, wherein aluminium or gold are used for the electrodes.

8. A released microstructure suitable for a microelectromechanical device when formed according to the method defined in any one of claims 1 to 7.

9. A multi-layered wafer incorporating a released microstructure suitable for a microelectromechanical device when formed according to the method defined in any one of claims 1 to 7.