## ABSTRACT OF THE DISCLOSURE

A method and apparatus for updating the architectural state in a system implementing staggered execution with multiple micro-instructions. According to one aspect of the invention, a method is provided in which a macro-instruction is decoded into a first and second micro-instructions. The macro-instruction designates an operation on a pieced of data, and execution of the first and second micro-instructions separately cause the operation to be performed on different parts of the piece of data. The method also requires that the first micro-instruction is executed irrespective of the second micro-instructions (e.g., at a different time), and that it is detected that said second micro-instruction will not cause any non-recoverable exceptions. The results of the first micro-instruction are then used to update the architectural state in an earlier clock cycle than said second micro-instruction.

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