STANDARD CELL TEMPLATE AND SEMICONDUCTOR STRUCTURE

~~Cross-Reference to Related Applications~~

~~The present disclosure claims the priority to Chinese Patent Application No. 202110163720.X, titled "STANDARD CELL TEMPLATE AND SEMICONDUCTOR STRUCTURE", filed on February 5, 2021, which is incorporated herein by reference in its entirety.~~

Technical Field

The present disclosure relates to, but is not limited to, a standard cell template and a semiconductor structure.

Background

A standard cell library is the basis of integrated circuit design. Based on a standard cell library (SCL), integrated circuit (IC) design can carry out logic synthesis and layout route, which improves the efficiency of circuit design.

The SCL includes multiple pre-designed standard cell templates, which are provided for the IC designer or circuit design synthesis tool to complete IC layout design according to design requirements.

Summary

An overview of the subject matter detailed in the present disclosure is provided below, which is not intended to limit the protection scope of the claims.

The present disclosure provides a standard cell template and a semiconductor structure.

A first aspect of the present disclosure provides a standard cell template. The standard cell template includes a first well region and a second well region, arranged along a first direction; a first gate pattern, located in the first well region and extending along the first direction, configured for defining a first gate; a second gate pattern, located in the second well region and extending along the first direction, configured for defining a second gate; and a gate electrical connection pattern, located between the first gate pattern and the second gate pattern, configured for defining a gate electrical connection structure. The gate electrical connection structure is arranged on the same layer as the first gate and the second gate to electrically connect the first gate and/or the

FIG. 11 is a sectional view taken along CC1 direction in FIG. ~~9~~10.

FIG. 12 is another sectional view of the semiconductor structure according to the still another embodiment of the present disclosure.

FIG. 13 is a yet another sectional view of the semiconductor structure according to the still another embodiment of the present disclosure.

Detailed Description

The technical solutions in the embodiments of the present disclosure are described below clearly and completely with reference to the drawings in the embodiments of the present disclosure. Apparently, the described embodiments are merely part rather than all of the embodiments of the present disclosure. All other embodiments obtained by those skilled in the art based on the embodiments of the present disclosure without creative efforts should fall within the protection scope of the present disclosure. It should be noted that the embodiments in the present disclosure and features in the embodiments may be combined with each other in a non-conflicting manner.

The existing semiconductor structure fabricated by using a standard cell template has high power consumption and poor signal quality.

FIG. 1 is a schematic view of a standard cell template; and FIG. 2 is a partial sectional view of a semiconductor structure fabricated by using the standard cell template shown in FIG. 1.

Referring to FIGS. 1 and 2, the standard cell template includes: an N-type well region 11 and a P-type well region 12 arranged adjacently; at least one first gate pattern 13 located in the N-type well region 11, and configured for defining a first gate 23; at least one second gate pattern 14 located in the P-type well region 12, and configured for defining a second gate 24; a first contact hole pattern 15 located on the first gate pattern 13, and configured for defining a first contact hole structure 25 electrically connected to the first gate 23; a second contact hole pattern 16 located on the second gate pattern 14, and configured for defining a second contact hole structure 26 electrically connected to the second gate 24; and an electrical connection pattern 17 spanning the N-type well region 11 and the P-type well region 12, and connecting the first contact hole pattern 15 and the second contact hole pattern 16, and configured for defining an electrical connection layer 27. The electrical connection layer 27 is electrically connected to the first contact hole structure 25 and the second contact hole structure 26; and the electrical connection layer 27 is a