A CMOS APS WITH STACKED AVALANCHE MULTIPLICATION LAYER AND LOW VOLTAGE READOUT ELECTRONICS

FIELD OF THE INVENTION

[0001] The present invention relates to image sensors which use a stacked avalanche multiplication layer to amplify the intensity of light captured by a pixel circuit.

BACKGROUND OF THE INVENTION

[0002] Amid the rising popularity for digital image devices such as digital cameras is a demand for increasingly higher picture resolution and for increasingly compact designs of such devices. Due to the interior space constraints in the housings of the compact designs, it is necessary to reduce the sizes of the electronic circuits in the device, including the image sensor. However, upon shrinking the size of the image sensor, a tradeoff must be made between resolution and the signal levels outputted from the image sensor. If the resolution is kept the same upon reducing the size of the image sensor, the size of each pixel must be proportionately reduced. Smaller pixels reduce the amount of charge that can be collected by each pixel during image exposure, which in turn reduces the sensitivity of the image sensor. Although the reduced sensitivity effect can be offset by increasing the integration (exposure) time, this is an undesirable "solution" because increasing integration time also

increases the potential for obtaining a blurred image if there is any movement by the image subject or the device during exposure. On the other hand, in order to maintain the same sensitivity without having to increase integration time, the pixels must be made larger, which limits the resolution.

[0003] One solution towards achieving both a more compact size and high image quality is disclosed in "CMOS Image Sensor Overlaid with a HARP Photoconversion Layer," by T. Watabe, *et al.*, published in the Program of the 1999 IEEE Workshop on Charge-Coupled Devices and Advanced Image Sensors, pp. 211-214. In this image sensor, which is shown in FIGS. 1A and 1B, the pixel circuit 902 is overlaid with a stacked charge multiplying photoconversion layer, such as a high-gain avalanche rushing amorphous photoconductor ("HARP") photo-conversion layer 904 for amplifying the light signal produced by each pixel.

[0004] When a photon 906 hits the upper surface 908 of the HARP layer 904, a charge 910 in the form of holes is generated and amplified to many times its original level while being propelled through the HARP layer 904 to the bottom side 912. The pixel circuit 902 is electrically connected to the bottom side 912 of the HARP layer 904 such that the amplified light signal 910, upon reaching the bottom side 912 of HARP layer 904, is conducted into the pixel circuit 902 as electrical charge. The charge accumulates at a storage node 914 in the pixel circuit until the pixel data is read out by activating the gate of a row select switch 916. The amount of charge accumulated at the node 914, which is proportional to the intensity of light 906 detected, is read out. In this manner, the image

sensor of FIGS. 1A and 1B allows each pixel to capture image data with an intensity and sensitivity equivalent to that attainable by significantly larger pixels which do not have the avalanche multiplication capability. As a result, use of a HARP layer enables the image quality to be improved without having to increase the size of the image sensor array.

[0005] In order to obtain avalanche multiplication in the HARP layer, an electric field of about 10^6 V/cm is required, which is achieved by applying an operating voltage of between 50 – 100 V to the HARP layer. In a typical HARP image sensor, voltages of less than about 8 V are used in the pixel circuit connected beneath the HARP layer, with the pixel circuit generally having a breakdown voltage of around 20 V. When the intensity of the incident light on the image sensor is at the upper end of the detection range for the charge multiplying photoconversion layer, the voltage level accumulating at the storage diode beneath the HARP layer approaches the level of the operating voltage applied to the HARP layer. Thus, voltages of 50-100 V may be applied to the storage diode when the image sensor is exposed to a strong light, resulting in a breakdown of the readout components of the pixel circuit.

[0006] To address this problem, attempts have been made to build a pixel circuit having a higher breakdown tolerance. An example of such a high tolerance pixel circuit is disclosed in the article by T. Watabe *et al.* mentioned above, in which the pixel circuit is constructed as MOS transistor having a double drain structure. This structure is shown in FIG. 2, in which the n-doped drain formed in the p-doped silicon layer 922 includes a low-dose n- region 924 surrounding a conventional high-dose n+ region 926. The double

drain MOS transistor structure was shown to achieve an endurance voltage up to just under 60 V. However, a special MOS fabrication process is required for forming the double drain MOS transistor, and the size of the MOS transistor makes it difficult to attain small pixel sizes for high resolution image sensors.

[0007] Another problem encountered in typical HARP image sensors when the voltage level at the storage node rises is that the effective voltage applied across the photoconversion layer decreases, which affects the charge amplification function of the photoconversion layer. For example, in the arrangement shown in FIGS. 1A and 1B, as the charge representing a detected light flows from the HARP layer 904 and accumulates on the node 914 of the storage diode, the voltage at the node 914 increases, causing the potential difference between the operating voltage V_{target} applied to the HARP layer 904 and the storage node 914 to decrease. The result is pixel signal saturation and a nonlinear response in which the signal levels recorded by the imaging device are not correctly represented in the pixel output.

[0008] To address this problem, it is necessary to find a way to amplify the intensity of light signals by the same amount under bright light conditions as for lower light conditions, by either accounting for the loss of effective operating voltage across the charge multiplying photoconversion layer or otherwise addressing the decreasing amplification in bright light conditions.

BRIEF SUMMARY OF THE INVENTION

[0009] A first aspect of the present invention serves to mitigate problems associated with the high voltages which may be generated by a HARP layer under bright light conditions by incorporating a protection circuit into the pixel circuit connected to the HARP layer. The protection circuit prevents the pixel circuit from breaking down when the voltage in the pixel circuit reaches the operating voltage applied to the charge multiplying photoconversion layer in response to the image sensor being exposed to a strong light. In particular, the protection circuit of the present invention may be designed in any of several configurations in which additional voltage entering the pixel circuit from the charge multiplying photoconversion layer over a predetermined threshold voltage level is dissipated before reaching the storage node and other lower voltage components downstream therefrom.

[0010] A second aspect of the present invention addresses the problem of pixel saturation and nonlinear amplification of the image signal output from a charge multiplying photoconversion layer by incorporating an output control circuit into the pixel circuit connected to the charge multiplying photoconversion layer. Preferably, the output control circuit is constructed as a charge trans-impedance amplifier (CTIA) circuit including at least an operational amplifier, wherein the CTIA serves to fix the voltage level at the storage node to thereby maintain a constant effective operating potential across the charge multiplying photoconversion layer.

[0011] In one exemplary embodiment of the output control circuit in accordance with the invention, the effective voltage is maintained across a photoconversion element at a constant level to provide a linear output throughout the entire operating range of the photoconversion element. Another exemplary embodiment of an output control circuit in accordance with the invention also fixes the voltage across the photoconversion element, and further logarithmically compresses the image signal obtained from the photoconversion element. A third exemplary embodiment of the output control circuit provides a linear output signal in low light conditions until the current from the photoconversion element reaches a predetermined threshold value, whereupon the output control circuit then switches the output to a logarithmic signal in brighter light conditions. Optionally, the output control circuit of this last embodiment may be constructed so that the threshold value between the linear and logarithmic output characteristics is adjustable.

[0012] These and other features and advantages of the present invention will become more apparent from the following detailed description of the invention which is provided with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] FIG. 1A is a cross-sectional view of a pixel in an image sensor having a charge multiplying photoconversion layer as known in the art;

[0014] FIG. 1B is a circuit diagram of the pixel arrangement shown in FIG. 1A;

[0015] FIG. 2 is a cross-sectional view of a double-drain MOS transistor as known in the art;

[0016] FIG. 3 is an illustration of an alternative photoconversion element usable with the present invention;

[0017] FIG. 4 is a circuit diagram of a first preferred embodiment in accordance with the present invention;

[0018] FIG. 5 is a circuit diagram of a second preferred embodiment in accordance with the present invention;

[0019] FIG. 6 is a circuit diagram of a third preferred embodiment in accordance with the present invention;

[0020] FIG. 7 is a circuit diagram of a fourth preferred embodiment in accordance with the present invention;

[0021] FIG. 8 is a circuit diagram of a fifth embodiment in accordance with the present invention;

[0022] FIG. 9 is a circuit diagram of a sixth embodiment in accordance with the present invention;

[0023] FIG. 10 is a circuit diagram of a seventh embodiment in accordance with the present invention;

[0024] FIG. 11 is a graph for illustrating the conversion characteristics obtained by the embodiment shown in FIG. 10;

[0025] FIG. 12 is a circuit diagram of a eighth embodiment in accordance with the present invention;

[0026] FIG. 13 is a circuit diagram in accordance with a ninth embodiment of the present invention;

[0027] FIG. 14 is an example of an imaging apparatus incorporating the present invention; and

[0028] FIG. 15 is an illustration of a processing system communicating with the imaging apparatus of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0029] A first aspect of the present invention protects a pixel circuit connected to the HARP layer from breakdown caused by a high voltage transferred to the pixel circuit from the HARP layer under bright light conditions. The pixel circuit is protected from breakdown by incorporating therein a protection circuit which prevents excess voltage above a predetermined threshold level from reaching the components of the pixel circuit downstream from the protection circuit. A pixel structure in accordance with this aspect of the invention is described below with reference to FIGS. 4-7 showing four exemplary embodiments of a protection circuit providing the capability described above.

[0030] A first exemplary embodiment of the invention is shown in FIG. 4, and is similar to the pixel arrangement shown in FIG. 1B in that it includes a charge (hole) multiplying photoconversion layer 102 connected to a voltage V_{target} at its upper plate and connected to storage node 104 of a storage element 510 at its bottom plate. In this embodiment, storage element 510 is provided as a storage diode 106. Although the charge multiplying photoconversion layer is preferably a high-gain avalanche rushing amorphous photoconductor (HARP) photoconversion layer, other structures for detecting and performing photoconversion of a light signal and subsequently or simultaneously amplifying the resulting electrical charge may be used. Storage node 104 is the cathode of storage diode 106 for accumulating charge corresponding to image data being collected during the image sensor integration time. An output circuit 500 is connected to and positioned downstream from node 104, for reading out the charge accumulated at storage

diode 106. As shown in FIG. 4, output circuit 500 may be simply constructed as a row select transistor 108.

[0031] The anode of storage diode 106 is connected to ground so as to block current flow through diode 106 when the voltage at node 104 is a higher level than the ground connection, which will always be the case when an image signal is received from the charge multiplying photoconversion layer 102, since the signal charges are holes. Thus, with respect to storage diode 106, therefore, as long as the row select transistor 108 is open, charge flowing from charge multiplying photoconversion layer 102 as a result of the detection of light will accumulate at node 104.

[0032] Row select transistor 108 of output circuit 500 is connected to a column readout line 110 so that when the gate for the row select transistor 108 is closed, the charge at storage node 104 is transferred to the column readout line 110. When the column line containing the relevant pixel is activated, the image data from the pixel is transferred out of the pixel circuit 100 into an image processor where that charge is translated into image data along with the data read out from the other pixels in the image sensor array, to thereby construct the output image.

[0033] In order to prevent the charge accumulating at node 104 from reaching the breakdown point of storage diode 106 or row select transistor 108, a protection circuit 520 comprising a protection diode 112, the anode of which is connected to node 104 of storage diode 106. The cathode of protection diode 112 is connected to a voltage V_{dd}, so

that when the voltage level at storage node 104 reaches the level of V_{dd}, any additional voltage arriving from the charge multiplying photoconversion layer 102 is bled off away from node 104 toward the voltage source V_{dd}. In this manner, protection diode 112 serves to limit the voltage at node 104 to V_{dd}.

[0034] Once voltage is bled off from node 104 through protection diode 112, image data representing light intensities detected at the upper end of the capability range of charge multiplying photoconversion layer 102 will be lost. Thus, the voltage level at source V_{dd} should be set to strike a balance between minimizing the potential to lose image data acquired in the upper end of the detection range of layer 102, and limiting the voltage at node 104 to a comfortable level to avoid the risk of breakdown of the storage diode 106 and the row select transistor 108.

[0035] A second exemplary embodiment of the invention is shown in FIG. 5, and is identical to the pixel circuit of the first embodiment except that the storage element 510 is embodied as a storage capacitor 202 instead of a storage diode. Preferably, storage capacitor 202 has a large capacitance value per unit area, even more preferably in the rage of 2-5 fF/μ^2c. Such a capacitor provides a higher capacitance value while reducing the space required for the charge storage region, relative to the use of a storage diode.

[0036] In this embodiment, charge from the charge multiplying photoconversion layer 204 is stored in the capacitor 202, until the voltage at the capacitor 206 reaches V_{dd}. Additional voltage flowing to node 206 from the charge multiplying photoconversion layer

204 is then directed through the protection diode 208 of protection circuit 520 so that the charge stored in the capacitor 202 maintains a voltage of around V_{dd}.

[0037] A third exemplary embodiment of the invention, as shown in FIG. 6, is identical to the pixel circuit of the first embodiment, except that the protection diode of the protection circuit 520 is replaced with an n-MOS transistor 302. Both the drain and the gate of the transistor 302 are connected to the storage diode 308 of storage element 510, and the source of the transistor 302 is connected to a voltage potential of V_{dd}.

[0038] As in the embodiments described previously, charge from the image signal accumulates at the storage node 304 until the voltage at node 304 reaches and surpasses V_{dd}. Once this occurs, the higher voltage at the transistor drain causes the excess voltage to flow through the transistor, so that the voltage at the storage node 304 remains around V_{dd}.

[0039] In a variant of this embodiment, the storage diode 308 of storage element 510 may be replaced with the high capacity capacitor as described above with reference to the embodiment of FIG. 5.

[0040] FIG. 7 shows a fourth exemplary embodiment of the invention, which is identical to the embodiment of FIG. 4 except that the protection circuit 520 further includes a resistor 402 positioned between the bottom plate 406 of the charge multiplying photoconversion layer 404 and the storage diode 408 of storage element 510. The resistor preferably has a high resistance value which reduces the voltage passing through the

pixel circuit 400 from the charge multiplying photoconversion layer 404 and the storage diode 408 at node 410.

[0041] The presence of protection circuit 510, embodied here as protection diode 412, provides additional protection for the pixel circuit 400, so that in the event the signal voltage flowing from the charge multiplying photoconversion layer 404 is significantly larger than V_{dd} that the voltage at node 410 upon passing through resistor 402 is still too high, the excess voltage will be directed away from the storage diode 408 and the row select transistor 414 through the protection diode 412.

[0042] A first variation of the FIG. 7 embodiment may be provided by replacing the storage diode 408 of storage element 510 with the capacitor discussed above in the embodiment of FIG 4. Similarly, the present invention also encompasses a second variation of this embodiment in which the protection diode 412 is replaced with an n-MOS transistor as described above in the embodiment of FIG 5. In a third variation of the FIG. 7 embodiment, both the storage diode 408 of storage element 510 and the protection diode 412 are replaced with the capacitor of FIG. 5 and the n-MOS transistor of FIG. 6, respectively.

[0043] In an image sensor using a charge multiplying photoconversion layer, as the voltage level at the storage node rises, the effective voltage applied to the photoconversion layer decreases, which affects the charge amplification function of the photoconversion layer. For example, if the voltage V_{target} applied to the charge multiplying photoconversion

layer is reduced, the amplification achieved by the photoconversion layer is also reduced. Thus, when the signal level is read out upon activating the row select switch, the signal level recorded by the imaging device will be less than the signal level actually detected.

[0044] A second aspect of the present invention addresses this concern by incorporating into each pixel circuit an output control circuit which prevents the effective voltage across the photoconversion layer from decreasing during integration of light in the pixel. More specifically, the output control circuits according to this aspect of the invention serve to fix the voltage level at the storage node to maintain a constant effective operating potential across the charge multiplying photoconversion layer. The pixel structure disclosed herein will be further described below with reference to FIGS. 8-13 showing five exemplary embodiments of the output circuit in accordance with this aspect of the invention.

[0045] According to a fifth embodiment of the invention, shown in FIG. 8, the pixel structure includes a charge multiplying photoconversion layer 502 connected to a voltage V_{target} at its upper plate. The bottom plate of the charge multiplying photoconversion layer 502 is connected to output circuit 500 which includes a signal generation circuit 600 and a row select switch 130. Signal generation circuit 600 controls the characteristics of the charge received from the charge multiplying photoconversion layer 502. Row select switch 130 is connected to the output side of the signal generation circuit 600 for reading out the accumulated charge representing the image signal acquired from the charge multiplying photoconversion layer 502. Preferably, row select switch 130 is formed as a MOS

transistor and operated by a gate signal transmitted by a controller, such as the controller 824 shown in FIG. 14.

[0046] Row select switch 130 is connected to column readout line 110 so that when the switch 130 is closed (for example, upon receiving a gate signal from a controller when the row select switch is a transistor), the output voltage of the signal generation circuit 600 is transferred to a column readout line 110 and from there to a sample and hold circuit (*see, e.g.*, element 814 in FIG. 14). The image data from the pixel is transferred from the sample and hold circuit to a digitizer and then to an image processor where that charge is translated into image data along with the data read out from the other pixels in the image sensor array, to thereby construct the output image.

[0047] As seen in FIG. 8, the signal generation circuit 600 according to this embodiment is a charge trans-impedance amplifier (CTIA) circuit which includes a differential amplifier 128 connected to a constant voltage supply V_{REF} at a positive input 114 thereof. V_{REF} is set to a value slightly below the operating voltage of the differential amplifier to obtain sufficient output voltage swing. A feedback loop 120 is formed between an output node 116 of the differential amplifier 128 and a negative input node 122 thereof, and a capacitor 118 is connected in the feedback loop 120. A reset switch 126 is connected in a second loop 124 formed between the negative input node 122 and the output node 116 of the differential amplifier 128 and parallel to the feedback loop 120, for shorting out the capacitor 118 at the initialization period preceding each integration

time. Row select switch 130 is also connected to the output node 116 of the differential amplifier 128 downstream of the feedback loop 120 and second loop 124.

[0048] The differential amplifier 128 forces the voltage at the negative input node 122 to become fixed at V_{REF}, which in turn maintains the effective operating potential V_{target} across the charge multiplying photoconversion layer 502 at a constant level, i.e., $V_{target} - V_{REF}$. Since the multiplication factor to which an image signal is amplified in the photoconversion layer 502 is a function of the applied bias to the photoconversion layer, fixing the potential at the at the output side of the photoconversion layer 502, which is at the same potential as the negative input node 122 to the differential amplifier 128, yields a constant multiplication factor of the image signals detected by the charge multiplying photoconversion layer 502.

[0049] During integration time in this pixel circuit, current from the photoconversion layer 502 is integrated on the capacitor 118. When the row select switch 130 is closed, the output voltage of the differential amplifier 128 is transferred to the column readout line 110. Configured in this manner, the output voltage from the differential amplifier 128 represents the intensity of the detected incident light on the photoconversion layer 502, and is given by Eq. 1 below:

[0050] $$V_{out} = V_{REF} - \frac{I_{HARP} \bullet t_{INT}}{C_{fb}} \quad \ldots\ldots\ldots\ldots \quad (1)$$

[0051] wherein I_{HARP} and t_{INT} represent the current from the charge multiplying photoconversion layer 502 and the integration time, respectively, and C_{fb} represents the capacitance of the capacitor 118.

[0052] With the CTIA as shown in FIG. 8, the signal generation circuit 600 provides a linear output along the entire operating range of charge multiplying photoconversion layer 502.

[0053] FIG. 9 shows a pixel circuit in accordance with a second embodiment of the present invention. The pixel circuit of the sixth embodiment is generally the same as the pixel circuit discussed above with reference to FIG. 8, except that the signal generation circuit 600 in FIG. 8 is replaced by signal generation circuit 610 in the embodiment shown in FIG. 9. Components of this embodiment which are equivalent to those shown in FIG. 8 are identified in FIG. 9 with the same reference numerals, and description of those elements will be omitted in the description below.

[0054] Like signal generation circuit 600, signal generation circuit 610 also fixes the potential at the output side of a charge multiplying photoconversion layer 502 and the negative input node 122 to a differential amplifier 128, so as to maintain a constant effective input node voltage across the charge multiplying photoconversion layer 502 to be $V_{target} - V_{REF}$. Instead of a capacitor connected in the feedback loop, the CTIA circuit of signal generation circuit 610 includes a feedback diode 218 connected in a feedback loop 220 between the output node 116 and the negative input node 122 of the differential

amplifier 128. The anode of the feedback diode 218 is connected to the negative input node 122 of the differential amplifier 128 while the cathode of the feedback diode 218 is connected to the output node 116 of the differential amplifier. The current flowing across the feedback diode 218 is determined according to Eq. 2 below:

[0055] $$I_{Dfb} = I_o \cdot \left\{\exp\frac{q}{kT}(V_{REF} - V_{out}) - 1\right\} = I_{HARP} \quad \ldots\ldots\ldots\ldots\ldots\ldots (2)$$

[0056] wherein I_0 is the saturation current of the feedback diode 218, q represents the charge of an electron (= $1.6 \cdot 10^{-19}$ coulombs (C)), k is Boltzmann's constant (= $1.38 \cdot 10^{-23}$ J/°K), T represents the temperature of the diode measured in degrees Kelvin, V_{out} is the output voltage from the differential amplifier 128, and I_{HARP} represents the current from the charge multiplying photoconversion layer 502.

[0057] Using Eq. 2, the output voltage from the differential amplifier 128 can be determined as set forth in Eq. 3:

[0058] $$V_{out} = V_{REF} - \frac{kT}{q}\ln\frac{I_{HARP}}{I_0} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (3)$$

[0059] As can be seen from Eq. 3, the presence of feedback diode 218 in the feedback loop of the signal generation circuit 610 operates to logarithmically compress the current I_{HARP} flowing from the charge multiplying photoconversion layer 502 through the differential amplifier 128. Although the image signal obtained from the pixel circuit shown in FIGS. 1A and 1B becomes compressed due to the decreasing effective voltage across the photoconversion layer as the detected light level increases, logarithmically compressing the

image signal with the CTIA of the signal generation circuit 610 enables the pixel readout signal to be correlated much more predictably with the intensity of light actually detected at the photoconversion layer.

[0060] A seventh embodiment of the present invention is shown in FIG. 10 and includes an signal generation circuit 620 in place of the output control circuits 10 and 20 in the fifth and sixth embodiments described above. Components shown in FIG. 10 that are equivalent to the components shown in FIGS. 8 and 9 are identified with the same reference numerals, and discussion of those components will be omitted in the description of this embodiment below. Signal generation circuit 620 is constructed as a CTIA which includes a first feedback loop 120 and a second feedback loop 320 both connected between the output node 116 and the negative input node 122 of a differential amplifier 128.

[0061] Feedback loop 120 includes a capacitor 118 for providing a linear output from the differential amplifier 128, similarly to the embodiment of FIG. 8. Feedback loop 320 is arranged in parallel to feedback loop 120 and includes a feedback diode 218 and an offset voltage source 328 that applies a voltage V_{off} to the cathode of feedback diode 218. Offset voltage source 328 is connected to the output node 116 of a differential amplifier 128 and to the cathode of feedback diode 218, while the anode of feedback diode is connected to the negative input node 122 of the differential amplifier 128. A third loop 124 contains a reset switch 126 and is also connected between the output node 116 and the negative input node 122 of differential amplifier 128, in parallel to feedback loops 120 and 320.

[0062] The current I_{HARP} from the photoconversion layer 502 flows through the CTIA of signal generation circuit 620 according to Eq. 4 as follows:

[0063] $$I_o \cdot \exp\left\{\frac{q}{kT}(V_{REF} - V_{out} - V_{off})\right\} + \frac{d}{dt} C_{fb} (V_{REF} - V_{out}) = I_{HARP} \quad \ldots\ldots\ldots (4)$$

[0064] The first term represents the current flowing across the feedback diode 218 and the second term represents the current flowing to the feedback capacitor 118. When $V_{REF} - V_{out} - V_{off} < 0$, that is, when $V_{REF} - V_{off} < V_{out} < V_{REF}$, the second term of Eq. 4 is dominant. In this situation, no current flows through the feedback diode 218, and the output voltage V_{out} from the signal generation circuit 620 is determined according to Eq. 1 set forth above.

[0065] On the other hand, when $V_{REF} - V_{out} - V_{off} > 0$, that is, when $V_{out} < V_{REF} - V_{off}$, current flows through the feedback diode 218 and becomes logarithmically compressed, as indicated by the first term in Eq. 4. When I_{HARP} is sufficiently large, the second term becomes negligible, which yields an output voltage of the differential amplifier 128 according to Eq. 5 below:

[0066] $$V_{out} = V_{REF} - V_{off} - \frac{kT}{q} \ln \frac{I_{HARP}}{I_0} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (5)$$

[0067] The resulting conversion characteristics represented by V_{out} over time is shown in FIG. 11, where it can be clearly seen that linear conversion characteristics are obtained when $V_{out} > V_{REF} - V_{off}$, and logarithmic conversion characteristics are obtained when $V_{out} < V_{REF} - V_{off}$. Thus, the readout signal obtained from the pixel circuit shown in FIG.

10 varies linearly with the signal outputted from the charge multiplying photoconversion layer 502 in low light conditions, and varies logarithmically with the signal outputted from the charge multiplying photoconversion layer 502 in bright light conditions.

[0068] Optionally, the transition point at which the signal generation circuit 620 switches from the linear conversion mode to the logarithmic conversion mode can be made to be adjustable by enabling a user to apply a variable reverse bias potential to the feedback diode 218. This variation of the pixel circuit of FIG. 10 is illustrated in FIG. 12 and discussed below as the eighth embodiment of the present invention.

[0069] The pixel circuit shown in FIG. 12 is nearly identical to that shown in FIG. 10, except that the offset voltage source 328 in FIG. 10 is replaced with an offset capacitor 430. Again, components in FIG. 12 that are equivalent to those shown in the previous drawings are identified with the same reference numerals, and descriptions of those elements will be omitted in the explanation of this embodiment provided below.

[0070] One terminal of a switch 432 is connected to the offset capacitor 430 at a node 434 located along a feedback loop 320 between the capacitor 430 and a feedback diode 218. The other terminal of the switch 432 is connected to a voltage source 436 having a voltage $V_{REF} + V_{off}$. The voltage level of V_{off} may be adjustable by a user to thereby adjust the transition point between the linear and logarithmic operation modes of the pixel circuit. The adjustable voltage V_{off} is applied to the feedback diode 218 by closing the switch 432 which enables current from the voltage source 436 at the selected voltage level to flow to

the capacitor 430. Even if the level of V_{off} is not adjusted, the voltage level applied to the cathode of feedback diode 218 can be adjusted by controlling the length of time that the switch 432 is closed, which controls the amount of charge in, and hence the voltage across the feedback capacitor 430.

[0071] During the initialization period before the start of each integration time and before charging the offset capacitor 430, the switch 432 is closed along with reset switch 126 by a reset signal ΦRS. When the switches 126 and 432 are closed by the reset signal ΦRS, the capacitor 118 is shorted out to clear out any residual charge on the capacitors associated with the image signal most recently read out from the pixel circuit and the capacitor 430 is charged to V_{off}.

[0072] A ninth embodiment of the present invention is shown in FIG. 13, and is identical to the embodiment shown in FIG. 12, except that the embodiment shown in FIG. 13 further includes a circuit for performing a freeze frame shutter operation. Specifically, a freeze frame switch 542 and a hold capacitor 540 are connected in the pixel circuit between the output node 116 from the differential amplifier 128 and the row select switch 130. Freeze frame switch 542 is controlled by a transfer signal ΦT that closes the freeze frame switch 542 to enable the image signal to flow to and be stored in the hold capacitor 540. When the freeze frame switch is opened, no further charge can accumulate in the hold capacitor 540.

[0073] After charging the hold capacitor 540 with the image signal, the charge is held in the hold capacitor to enable the image signal for that pixel to be read out by closing the row select switch 130 for each readout operation. For example, when an image is captured by an entire image sensor pixel array, the image sensor can be operated in freeze frame mode in which the image signal for each pixel is frozen so that the image data from all the pixels in the array can be read out row by row. Thus, the freeze frame switch 542 is closed and then opened by operation of the transfer signal ΦT to all of the pixels in the image sensor array at the same time, whereupon the row select signal is applied to the image sensor array row by row to read out the pixel image signals.

[0074] In the embodiments shown in FIGS. 9, 10, 12 and 13 described above, feedback diode 218 may be implemented by use of the sub-threshold characteristics of a MOS transistor. It is readily understood by one of ordinary skill in the art that a MOS transistor has four operational modes depending on bias conditions: 1) when no bias is applied to the gate, the transistor is off and no current flows from the drain; 2) the transistor is in a subthreshold region when the gate voltage V_G is less than a predetermined threshold voltage V_T, wherein the current flowing from the drain is $I_D = I_0 \cdot \exp\{q(V_G - V_T)/kT\}$; 3) the transistor is in a saturation region when $V_G - V_T < V_D$ (drain voltage), wherein the current flowing from the drain is $I_D = (\beta/2) \cdot (V_G - V_T)^2$; and 4) the transistor is in a linear region when $V_G - V_T > V_D$, wherein the current flowing from the drain is $I_D = \beta \cdot (V_G - V_T - V_D/2) \cdot V_D$.

[0075] In each of the fifth through ninth embodiments of the invention as shown in FIGS. 8-13, there is no storage element connected between the bottom plate of the charge multiplying photoconversion layer and the output control circuit as is the case in the first through fourth embodiments of the invention as shown in FIGS. 4-7. Thus, in the embodiments of FIGS. 8-13, the bottom plate of the charge multiplying photoconversion layer is connected directly to the input node 122 of the respective output control circuit 500.

[0076] An additional aspect of the invention provides a pixel structure having both an output circuit 500 for maintaining a constant voltage across the charge multiplying photoconversion layer and a protection circuit 520 for dissipating excess voltage over a predetermined threshold being outputted from the charge multiplying photoconversion layer into the output control circuit 500. Here, the bottom plate of the charge multiplying photoconversion layer is connected to both the negative input of the differential amplifier 128 in the output circuit 500 and the input to the protection circuit 520.

[0077] A tenth embodiment of a pixel structure in accordance with this aspect of the invention is nearly identical to the fifth embodiment pixel structure shown in FIG. 8, but further includes a protection circuit connected to the node 122 in the output control circuit 500. As with the protection circuits described above, the protection circuit in the tenth embodiment may be constructed as a diode such as the protection diode 112 shown and described above with reference to FIG. 4, an n-MOS transistor such as the n-MOS

transistor 302 shown and described above with reference to FIG. 6, a resistor and a diode such as the resistor 402 and protection diode 412 shown and described above with reference to FIG. 7, or a resistor and an n-MOS transistor as disclosed above.

[0078] An eleventh embodiment of a pixel structure in accordance with this aspect of the invention is nearly identical to the sixth embodiment pixel structure shown in FIG. 9, and further includes a protection circuit connected to the node 122 in the output control circuit 500. As with the protection circuits described above, the protection circuit in the eleventh embodiment may be constructed as a diode such as the protection diode 112 shown and described above with reference to FIG. 4, an n-MOS transistor such as the n-MOS transistor 302 shown and described above with reference to FIG. 6, a resistor and a diode such as the resistor 402 and protection diode 412 shown and described above with reference to FIG. 7, or a resistor and an n-MOS transistor as disclosed above.

[0079] A twelfth embodiment of a pixel structure in accordance with this aspect of the invention is nearly identical to the seventh embodiment pixel structure shown in FIG. 10, and further includes a protection circuit connected to the node 122 in the output control circuit 500. As with the protection circuits described above, the protection circuit in the twelfth embodiment may be constructed as a diode such as the protection diode 112 shown and described above with reference to FIG. 4, an n-MOS transistor such as the n-MOS transistor 302 shown and described above with reference to FIG. 6, a resistor and a diode such as the resistor 402 and protection diode 412 shown and described above with reference to FIG. 7, or a resistor and an n-MOS transistor as disclosed above.

[0080] A thirteenth embodiment of a pixel structure in accordance with this aspect of the invention is nearly identical to the eighth embodiment pixel structure shown in FIG. 12, and further includes a protection circuit connected to the negative input to the differential amplifier in the output control circuit 500. As with the protection circuits described above, the protection circuit in the thirteenth embodiment may be constructed as a diode such as the protection diode 112 shown and described above with reference to FIG. 4, an n-MOS transistor such as the n-MOS transistor 302 shown and described above with reference to FIG. 6, a resistor and a diode such as the resistor 402 and protection diode 412 shown and described above with reference to FIG. 7, or a resistor and an n-MOS transistor as disclosed above.

[0081] A fourteenth embodiment of a pixel structure in accordance with this aspect of the invention is nearly identical to the ninth embodiment pixel structure shown in FIG. 13, and further includes a protection circuit connected to the negative input to the differential amplifier 128 in the output control circuit 500. As with the protection circuits described above, the protection circuit in the fourteenth embodiment may be constructed as a diode such as the protection diode 112 shown and described above with reference to FIG. 4, an n-MOS transistor such as the n-MOS transistor 302 shown and described above with reference to FIG. 6, a resistor and a diode such as the resistor 402 and protection diode 412 shown and described above with reference to FIG. 7, or a resistor and an n-MOS transistor as disclosed above.

circuit does not affect the operation of the pixel since the input to the differential amplifier is fixed at V_{REF}. However, if a storage element is present and if the differential amplifier and the feedback loop(s) are malfunctioning, the current may then accumulate at the storage element.

[0083] In each of the embodiments described above, the charge multiplying photoconversion layer is preferably a high-gain avalanche rushing amorphous photo conductor (HARP) photoconversion layer. Alternatively, however, other photosensitive elements for detecting and performing photoconversion of a light signal and subsequently or simultaneously amplifying the resulting electrical charge may be used instead, such as a photodiode or a stacked pixel sensor structure, wherein the effective light sensitive area may be significantly increased by the stacked structure. An example of a stacked pixel sensor structure is illustrated in FIG. 3 and described in fuller detail in "A Stacked CMOS APS For Charge Particle Detection And Its Noise Performance," by I. Takayanagi *et al.*, IEEE Workshop on Charge-Coupled Devices and Advanced Image Sensors, pp. 159-162, June 1999, the contents of which are hereby incorporated by reference.

[0084] An example of an imaging device incorporating the present invention is shown in FIG. 14. Specifically, an imaging apparatus 800 includes an image sensor 802 having a pixel array arranged according to a Bayer color filter pattern. A charge multiplying photoconversion layer such as a HARP layer is provided over each of the pixels in the array under the filter pattern. Each pixel 804 contains the protection and readout circuits in accordance with any one of the various embodiments discussed herein above.

[0085] The imaging apparatus 800 further includes a row decoder 806 includes a plurality of row select activation lines 808 corresponding in number to the number of rows in the pixel array of the image sensor 802, wherein each line is connected to each row select switch in all the pixels in a respective row of the array. Similarly, column decoder 812 includes a plurality of column lines 812, the number of which corresponds to the number of columns in the pixel array of the image sensor 802. Each column line 812 is connected to the output sides of the row select switches in all the pixels in a respective column.

[0086] To read the image data obtained by the image sensor 802, controller 824 controls the row decoder 806 to sequentially activate the row select lines, whereby the row select switches for each pixel in a selected row is activated to thereby dump the image data from each respective pixel to the respective column line. Since each pixel in a row is connected to a different column line, the image data for each pixel is then read out to the image processor by sequentially activating all the column lines through column decoder 810. Thus, after activation of each row select line, the column lines are sequentially activated to collect the image data in an orderly manner across the array.

[0087] Upon reading the image data out of the pixel array, the data is passed through a number of processing circuits which, in linear order, generally include a sample and hold circuit 814, an amplifier 816, an analog to digital converter 818, an image processor 820, and an output device 822.

[0088] Without being limiting, such the imaging apparatus 800 could be part of a computer system, camera system, scanner, machine vision system, vehicle navigation system, video telephone, surveillance system, auto focus system, star tracker system, motion detection system, image stabilization system and other systems requiring an imager.

[0089] The imaging apparatus 800 may also be connected to a processor system 850, as shown in FIG. 15, such as a computer system. A processor system 850 generally comprises a central processing unit (CPU) 852 that communicates with an input/output (I/O) device 854 over a bus 856. The imaging apparatus 800 communicates with the system over bus 856 or a ported connection. The processor system 800 also includes random access memory (RAM) 858, and, in the case of a computer system, may include peripheral devices such as a floppy disk drive 860 and a compact disc (CD) ROM drive 862 which also communicate with CPU 852 over the bus 856.

[0090] Although the present invention has been described in relation to particular embodiments thereof, many other variations and modifications and other uses will become apparent to those skilled in the art. Therefore, the present invention is to be limited not by the specific disclosure herein, but only by the appended claims.

CLAIMS

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. An image sensor pixel among an array of pixels in an image sensor, comprising:

a charge multiplying photoconversion element; and

a charge storage element electrically connected to the charge multiplying photoconversion element, and

a protection circuit electrically connected to the charge storage element for limiting a voltage which accumulates at the charge storage element.

2. The image sensor pixel according to claim 1, wherein the charge multiplying photoconversion element is a high gain avalanche rushing amorphous photoconductor photoconversion layer.

3. The image sensor pixel according to claim 1, wherein the charge multiplying photoconversion element is a stacked pixel structure.

4. The image sensor pixel according to claim 1, wherein the storage element is a junction photodiode, the cathode of which is connected to the charge multiplying photoconversion element.

5. The image sensor pixel according to claim 1, wherein the storage element is a capacitor.

6. The image sensor pixel according to claim 1, wherein the protection circuit includes a protection diode electrically connected to the storage element at the anode thereof and connected to a voltage source which sets a limit voltage level at the cathode thereof, whereby voltage accumulating at the storage element in excess of the limit voltage level is transferred away from the storage element through the protection diode.

7. The image sensor pixel according to claim 6, wherein the protection circuit further comprises a resistor electrically connected between the charge multiplying photoconversion element and the storage element.

8. The image sensor pixel according to claim 1, wherein the protection circuit includes an n-MOS transistor having a drain and a gate both electrically connected to the storage element, and a source electrically connected to a voltage source which sets a limit voltage level, whereby voltage accumulating at the storage element in excess of the limit voltage level is transferred away from the storage element through the n-MOS transistor.

9. The image sensor pixel according to claim 8, wherein the protection circuit further comprises a resistor electrically connected between the charge multiplying photoconversion element and the storage element.

10. The image sensor pixel according to claim 1, further comprising an output circuit connected to the charge storage element and to the protection circuit.

11. The image sensor pixel according to claim 10, wherein the output circuit includes a row select transistor which reads out the charge stored at the charge storage element.

12. An image sensor pixel among an array of pixels in an image sensor, comprising:

a photosensitive element having an input side for detecting a light signal and an output side for outputting the detected light signal as an electrical image signal; and

an output control circuit connected to the output side of the photosensitive element, wherein the output control circuit fixes the potential of the output side of the photosensitive element at a predetermined voltage level.

13. The image sensor pixel according to claim 12, wherein the photosensitive element is a photodiode.

14. The image sensor pixel according to claim 12, wherein the photosensitive element is a stacked pixel structure.

15. The image sensor pixel according to claim 12, wherein the photosensitive element is a charge multiplying photoconversion layer.

16. The image sensor pixel according to claim 12, wherein the photosensitive element is a high gain avalanche rushing amorphous photoconductor photoconversion layer.

17. The image sensor pixel according to claim 12, wherein the output control circuit comprises an operational amplifier and a feedback loop.

18. The images sensor pixel according to claim 17, wherein the operational amplifier is a differential amplifier having a first input, a second input and an output, wherein the first input is connected to a fixed voltage V_{REF}, and the second input is connected to the output of the differential amplifier via the feedback loop.

19. The image sensor pixel according to claim 18, wherein the first input is a positive input to the differential amplifier and the second input is a negative input to the differential amplifier.

20. The image sensor pixel according to claim 12, wherein the output control circuit provides a linear amplification of the image signal outputted from the photosensitive element.

21. The image sensor pixel according to claim 20, wherein the output control circuit comprises:

a differential amplifier having a fixed voltage V_{REF} connected to a positive input to the differential amplifier,

a feedback loop connecting a negative input of the differential amplifier to the output thereof, and

a capacitor connected in the feedback loop.

22. The image sensor pixel according to claim 21, wherein the output control circuit further comprises a second loop connected between the output of the differential amplifier and the negative input thereto, in parallel with the feedback loop, wherein the second loop includes a reset switch connected therein.

23. The image sensor pixel according to claim 12, wherein the output control circuit provides a logarithmically compressed conversion of the image signal outputted from the photosensitive element.

24. The image sensor pixel according to claim 23, wherein the output control circuit comprises:

a differential amplifier having a fixed voltage V_{REF} connected to a postive input to the differential amplifier,

a feedback loop connecting a negative input of the differential amplifier to the output thereof, and

a diode connected in the feedback loop with the anode of the diode connected to the negative input to the differential amplifier and the cathode of the diode connected to the output of the differential amplifier.

25. The image sensor pixel according to claim 24, wherein the diode is formed as a MOS transistor.

26. The image sensor pixel according to claim 24, wherein the output control circuit further comprises a second loop connected between the output of the differential amplifier and the negative input thereto, in parallel with the feedback loop, wherein the second loop includes a reset switch connected therein.

27. The image sensor pixel according to claim 12, wherein the output control circuit provides a linear conversion when the image signal outputted from the photosensitive element is within a first signal range and a logarithmically compressed conversion when the image signal is within a second signal range.

28. The image sensor pixel according to claim 27, wherein the output control circuit comprises:

a differential amplifier having a fixed voltage V_{REF} connected to a positive input to the differential amplifier,

a first feedback loop connecting a negative input of the differential amplifier to the output thereof,

a feedback capacitor connected in the first feedback loop,

a second feedback loop connecting the negative input of the differential amplifier to the output thereof, in parallel with the first feedback loop,

a diode connected in the second feedback loop with the anode of the diode connected to the negative input to the differential amplifier, and

a reverse bias voltage connected to the cathode of the diode in the second feedback loop.

29. The image sensor pixel according to claim 28, further comprising an offset voltage source connected in the second feedback loop and to the cathode of the diode for supplying the reverse bias voltage to the diode.

30. The image sensor pixel according to claim 28, further comprising

an offset capacitor connected in the second feedback loop and to the cathode of the diode, and

an offset switch having a first terminal connected to the second feedback loop between the cathode of the diode and the offset capacitor, and having a second terminal connected to an offset voltage source, whereby the offset capacitor becomes charged upon closing the offset switch to thereby apply the reverse bias voltage to the diode.

31. The image sensor pixel according to claim 28, wherein the diode is formed as a MOS transistor.

32. The image sensor pixel according to claim 28, wherein the output control circuit further comprises a third loop connected between the output of the differential amplifier and the negative input thereto, in parallel with the first and second feedback loops, wherein the third loop includes a reset switch connected therein.

33. The image sensor pixel according to claim 12, wherein the output control circuit includes a freeze frame circuit for performing a freeze frame shutter function.

34. The image sensor pixel according to claim 33, wherein the freeze frame circuit comprises:

a freeze frame switch, and

a capacitor connected to one terminal of the freeze frame switch, for capturing the charge of an image signal when the freeze frame switch is closed.

35. The image sensor pixel according to claim 12, further comprising a protection circuit connected to the output side of the photosensitive element and an input to the output control circuit.

36. The image sensor pixel according to claim 35, wherein the protection circuit includes a protection diode.

37. The image sensor pixel according to claim 36, wherein the protection circuit further comprises a resistor.

38. The image sensor pixel according to claim 35, wherein the protection circuit includes an n-MOS transistor having a drain and a gate both electrically connected to the output of the photosensitive element, and a source electrically connected to a voltage source which sets a limit voltage level, whereby current flowing from the photosensitive element having a voltage in excess of the limit voltage level is transferred away from the output circuit through the n-MOS transistor.

39. The image sensor pixel according to claim 38, wherein the protection circuit further comprises a resistor.

40. The image sensor pixel according to claim 35, wherein the output control circuit includes

a differential amplifier having a positive input fixed at V_{REF}, a negative input connected to the output of the photosensitive element, and an output,

a feedback loop connecting the output and the negative input of the differential amplifier, and

a capacitor in the feedback loop and connected to the output and the negative input of the differential amplifier.

41. The image sensor pixel according to claim 35, wherein the output circuit includes

a differential amplifier having a positive input fixed at V_{REF}, a negative input connected to the output of the photosensitive elmeent, and an output,

a feedback loop connecting the output and the negative input of the differential amplifier, and

a diode in the feedback loop having its cathode connected to the output of the differential amplifier and its anode connected to the negative input of the differential amplifier.

42. The image sensor pixel according to claim 35, wherein the output circuit includes

a differential amplifier having a positive input fixed at V_{REF}, a negative input connected to the output of the photosensitive element, and an output,

a feedback circuit connecting the output and the negative input of the differential amplifier,

a capacitor in the feedback circuit and connected to the output and the negative input of the differential amplifier,

a diode in the feedback circuit in parallel with the capacitor and having its anode connected to the negative input of the differential amplifier, and

an offset voltage source in the feedback circuit in parallel with the capacitor and connected to the cathode of the diode and to the output of the differential amplifier.

43. An image sensor comprising:

a charge multiplying photoconversion element; and

an image sensor pixel array having a plurality of pixels, wherein each pixel comprises:

an output circuit connected to the charge multiplying photoconversion element, wherein the output control circuit maintains the potential across the charge multiplying photoconversion element to be at a predetermined voltage level.

44. An image sensor comprising:

a charge multiplying photoconversion element; and

an image sensor pixel array having a plurality of pixels, wherein each pixel comprises:

an output control circuit connected to the charge multiplying photoconversion element, wherein the output control circuit provides a linear conversion of an image signal outputted from the charge multiplying photoconversion element for the entire operational range of the charge multiplying photoconversion element.

45. An image sensor comprising:

a charge multiplying photoconversion element; and

an image sensor pixel array having a plurality of pixels, wherein each pixel comprises:

an output control circuit connected to the charge multiplying photoconversion element, wherein the output control circuit provides a logarithmically compressed conversion of an image signal outputted from the charge multiplying photoconversion element for the entire operational range of the charge multiplying photoconversion element.

46. An image sensor comprising:

a charge multiplying photoconversion element; and

an image sensor pixel array having a plurality of pixels, wherein each pixel comprises:

an output control circuit connected to the charge multiplying photoconversion element, wherein the output control circuit provides a linear conversion of image signal outputted from the charge multiplying photoconversion element when the output of the charge multiplying photoconversion element is within a first range and a logarithmically compressed conversion of the image signal when the output of the charge multiplying photoconversion element is within a second range.

47. A method for obtaining an image signal, comprising:

detecting a light signal in an image sensor;

photoconverting the light signal into an electrical signal in a photosensitive element in the image sensor;

amplifying the electrical signal in the photosensitive element;

transferring the electrical signal to a storage element;

accumulating charge from the electrical signal at the storage element; and

limiting the voltage at the storage element to a predetermined limit voltage level.

48. The method according to claim 47, wherein limiting the voltage includes transferring charge away from the storage element when the voltage resulting from the accumulated charge exceeds the predetermined limit level.

49. The method according to claim 48, wherein limiting the voltage further includes lowering the voltage of the electrical signal prior to the charge accumulating at the storage element.

50. The method according to claim 47, further comprising reading out the charge accumulated at the storage element.

51. A method for obtaining an image signal, comprising:

detecting a light signal in an image sensor;

photoconverting the light signal into an electrical signal with a charge multiplying photosensitive element of the image sensor;

amplifying the electrical signal in the charge multiplying photosensitive element; and

maintaining the potential across the photosensitive element to be constant at a predetermined voltage level.

52. The method according to claim 51, further comprising performing a linear conversion of the electrical signal outputted from the photosensitive element over the entire operating range of the photosensitive element.

53. The method according to claim 51, further comprising logarithmically compressing the electrical signal outputted from the photosensitive element over the entire operating range of the photosensitive element.

54. The method according to claim 51, further comprising performing a linear conversion of the electrical signal outputted from the photosensitive element when the outputted electrical signal is within a first range up to a predetermined threshold level, and

logarithmically compressing the electrical signal when the outputted electrical signal is within a second range above the threshold level.

55. The method according to claim 54, further comprising adjusting the threshold level at which the output control circuit switches from performing linear conversion of the electrical signal to logarithmic compression of the electrical signal.

56. The method according to claim 51, further comprising performing a freeze frame operation on the electrical signal obtained by the charge multiplying photosensitive element.

57. The method according to claim 51, wherein maintaining a constant potential across the photosensitive element comprises limiting the voltage of the electrical signal outputted from the charge multiplying photosensitive element to the predetermined voltage level.

58. The method according to claim 57, wherein limiting the voltage includes transferring away a portion of the electrical signal which exceeds the predetermined voltage level.

59. The method according to claim 58, wherein limiting the voltage further includes lowering the voltage of the electrical signal prior to transferring away the portion of the signal which exceeds the predetermined voltage level.

60. An image processing apparatus comprising:

an image sensor for detecting an image and outputting image signals corresponding to the detected image; and

an image processor for processing the image signals outputted from the image sensor,

wherein the image sensor comprises:

a charge multiplying photoconversion element; and

a pixel array having a plurality of pixels, wherein each pixel includes

a charge storage element electrically connected to the charge multiplying photoconversion layer, and

a protection circuit electrically connected to the charge storage element for limiting a voltage which accumulates at the charge storage element.

61. A processing system, comprising:

a processor for receiving and processing image data; and

an image data generator for supplying image data to the processor, the image data generator comprising

an image sensor for detecting light and outputting an image signal,

an image processor for processing the image signal, and

a controller for controlling the image sensor and the image processor,

wherein the image sensor comprises

a charge multiplying photoconversion element; and

a pixel array having a plurality of pixels, wherein each pixel includes

a charge storage element electrically connected to the charge multiplying photoconversion layer, and

a protection circuit electrically connected to the charge storage element for limiting a voltage which accumulates at the charge storage element.

62. An image processing apparatus comprising:

an image sensor for detecting an image and outputting image signals corresponding to the detected image; and

an image processor for processing the image signals outputted from the image sensor,

wherein the image sensor comprises a pixel array having a plurality of pixels, wherein each pixel comprises:

a photosensitive element having an input side for detecting a light signal and an output side for outputting the detected light signal as an electrical signal; and

an output control circuit connected to the output side of the photosensitive element, wherein the output control circuit maintains the potential across the photosensitive element to be constant.

63. The image processing apparatus of claim 62, wherein each pixel further comprises a protection circuit for limiting the voltage level at the output side of the photosensitive element at a predetermined voltage level.

64. A processing system, comprising:

a processor for receiving and processing image data; and

an image data generator for supplying image data to the processor, the image data generator comprising:

an image sensor for obtaining an image and outputting an image signal,

an image processor for processing the image signal, and

a controller for controlling the image sensor and the image processor,

wherein the image sensor comprises

a charge multiplying photoconversion element; and

a pixel array having a plurality of pixels, wherein each pixel includes

a photosensitive element having an input side for detecting a light signal and an output side for outputting the detected light signal as an electrical signal; and

an output control circuit connected to the output side of the photosensitive element, wherein the output control circuit maintains the potential across the photosensitive element to be constant.

65. The processing system of claim 64, wherein each pixel further comprises a protection circuit for limiting the voltage level at the output side of the photosensitive element at a predetermined voltage level.