MEMORY

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is based on and claims priority of the Chinese Patent Application No. 202411689849.4, filed with the China National Intellectual Property Administration on November 22, 2024 and entitled "MEMORY". The above-referenced disclosure is incorporated herein by reference in its entirety.

TECHNICAL FIELD

[0002] Embodiments of this application relate to the semiconductor field, and in particular to a memory.

BACKGROUND

[0003] In a design of a memory, especially in a design of a dynamic random access memory (DRAM), the gate of an access transistor in a memory cell is connected to a word line, the drain thereof is connected to a bit line, the word line is driven by a word line driver, and the voltage of the bit line is amplified by a sense amplifier. In different memory products, memory cells may be arranged in a plane or may be stacked in multiple layers. In different scenarios, the layouts of the word line driver and the sense amplifier need to be changed adaptively.

SUMMARY

[0004] Embodiments of this application provide a memory, which facilitates at least increasing the density of memory cells in the memory in an extension direction of a word line.

[0005] According to some embodiments of this application, the embodiments of this application provide a memory, which may include at least: memory arrays and word line

drivers, where the word line drivers are configured to drive word lines in the memory arrays, the word lines include first-type word lines and second-type word lines, the word line drivers include first drivers and second drivers, the first drivers are configured to drive the first-type word lines, and the second drivers are configured to drive the second-type word lines; and connection bridges, including first connection bridges and second connection bridges, where the first-type word lines are connected to the first drivers via the first connection bridges, and the second-type word lines are connected to the second drivers via the second connection bridges; and an extension direction of each of the connection bridges is the same as a first direction, a direction of each of the first connection bridges toward the second connection bridges is perpendicular to the first direction, and the first direction is an extension direction of each of the word lines.

[0006] In some embodiments, the first-type word lines are odd-numbered word lines, the second-type word lines are even-numbered word lines, the first connection bridges and the second connection bridges are located on two opposite sides of the memory arrays in a second direction, the second direction is perpendicular to the first direction, and the second direction is an extension direction of a common bit line.

[0007] In some embodiments, at least three memory arrays sequentially arranged in the extension direction of each of the word lines share one of the first connection bridges and one of the second connection bridges, and share one of the first drivers and one of the second drivers.

[0008] In some embodiments, multiple ones of the memory arrays sharing the same one of the first connection bridges and the same one of the second connection bridges form an array group, the first connection bridges are connected to the first drivers via first word line contact pads, the second connection bridges are connected to the second drivers via second word line contact pads, and the first word line contact pads and the second word line contact pads are located on two opposite sides of only a part of the memory arrays in the array group in the second direction.

[0009] In some embodiments, each of the first connection bridges is in contact connection with only one of the first word line contact pads, and each of the first word line contact pads is connected to one of the first drivers; or each one of the first connection bridges is in contact

connection with multiple ones of the first word line contact pads, and each first word line is in bonding connection with different ones of the first drivers; or each of the first connection bridges is in contact connection with multiple ones of the first word line contact pads, and the multiple ones of the first word line contact pads are connected to the same one of the first drivers.

[0010] In some embodiments, each of the first connection bridges is in contact connection with the multiple ones of the first word line contact pads, and the multiple ones of the first word line contact pads are disposed on each of the first connection bridges at equal intervals.

[0011] In some embodiments, the memory includes multiple layers of the array groups stacked in a vertical direction, each of the first connection bridges is connected to only one of the first word line contact pads, and the projections of the first word line contact pads in the vertical direction corresponding to the array groups at different layers are arranged in the first direction.

[0012] In some embodiments, the memory includes multiple layers of the array groups stacked in a vertical direction, each of the first connection bridges is connected to multiple ones of the first word line contact pads, and the projections of the first word line contact pads in the vertical direction that correspond to the array groups at different layers and that are in the same order are arranged in the first direction.

[0013] In some embodiments, the first connection bridges are located between corresponding ones of the first word line contact pads and the array groups, and the second connection bridges are located between corresponding ones of the second word line contact pads and the array groups.

[0014] In some embodiments, the first word line contact pads and the second word line contact pads corresponding to the same one of the array groups have staggered orthographic projections in the second direction, the first word line contact pads corresponding to different ones of the array groups have overlapping orthographic projections in the second direction, and the second word line contact pads corresponding to different ones of the array groups have overlapping orthographic projections in the second direction.

BRIEF DESCRIPTION OF DRAWINGS

[0015] One or more embodiments are exemplified with the figures in the accompanying drawings corresponding to the one or more embodiments. These example descriptions are not intended to limit the embodiments, and unless specifically stated, no scale limitations are constituted by the figures in the accompanying drawings.

[0016] FIG. 1 is a schematic diagram of a connection relationship between a word line contact structure and a memory array in a memory;

[0017] FIG. 2 is a schematic diagram of a connection relationship between a word line driver and a word line in a memory;

[0018] FIG. 3 is a schematic structural diagram of a word line contact structure in a memory;

[0019] FIG. 4 is a schematic layout diagram of multiple memory array tile in a memory; and

[0020] FIG. 5 to FIG. 12 are schematic structural diagrams of a memory according to embodiments of this application.

DESCRIPTION OF EMBODIMENTS

[0021] Embodiments of this application are described in detail below with reference to the accompanying drawings. However, it may be understood by a person of ordinary skill in the art that in the embodiments of this application, many technical details are provided to enable readers to better understand this application. However, the technical solutions claimed in this application may be implemented even without these technical details and various changes and modifications made based on the following embodiments.

[0022] FIG. 1 is a schematic diagram of a connection relationship between a word line contact structure and a memory array in a memory. FIG. 2 is a schematic diagram of a connection relationship between a word line driver and a word line in a memory. FIG. 3 is a schematic structural diagram of a word line contact structure in a memory. FIG. 4 is a schematic layout diagram of multiple memory array tiles in a memory.

[0023] Referring to FIG. 1, in the memory, a word line driver SWD drives word lines WL

(or referred to as local word lines) via word line contact structures CT. An extension direction of the word line WL is a first direction X, and an extension direction of a common bit line CBL is a second direction Y. The memory includes multiple memory array tiles Mat arranged in the first direction X, and each memory array tile Mat may include multiple memory arrays subMat arranged in the second direction Y. The common bit line CBL is employed at least for local bit lines LBL at the same location in different memory arrays subMat. The word line contact structure CT is disposed between adjacent memory arrays subMat arranged in the first direction X, each word line contact structure CT is connected to the word line WL and the word line driver SWD, and the word line driver SWD drives, via the word line contact structure CT, a corresponding connected word line WL.

[0024] As shown in FIG. 1, for two word line contact structures CT adjacent in the first direction X, one is connected to an odd-numbered word line OWL in adjacent memory arrays subMat, and the other is connected to an even-numbered word line EWL in the adjacent memory arrays subMat. In other words, the word lines WL in each memory array subMat are driven by the word line contact structures CT in the first direction X located on two adjacent sides of each memory array subMat. The word line contact structure CT serves to connect the word line driver SWD, and further serves to separate different memory arrays subMat.

[0025] In FIG. 1, that each memory array subMat includes two odd-numbered word lines OWL and two even-numbered word lines EWL is taken as an example. Each word line contact structure CT is connected to all odd-numbered word lines OWL or even-numbered word lines EWL in adjacent memory arrays subMat. For a non-edge word line contact structure CT, each word line contact structure CT is connected to four word lines WL. Further, as shown in FIG. 2, when the word line driver SWD drives the word lines WL via a non-edge word line contact structure CT, four word lines WL are driven simultaneously (where bold lines are employed to represent that the word lines WL are driven).

[0026] In FIG. 2, a dashed line extending in the first direction X is employed to represent the odd-numbered word line OWL, and a solid line extending in the first direction X is employed to represent the even-numbered word line EWL. The word line driver SWD drives word lines in adjacent memory arrays subMat via a corresponding word line contact structure SC, and different word line contact structures SC correspond to different word line drivers

SWD.

[0027] Referring to FIG. 3, the word line contact structure CT includes a contact pad CTP, a horizontal connection bridge CTH, and a vertical connection bridge CTV. The contact pad CTP extends in the second direction Y and is in contact connection with the horizontal connection bridge CTH (namely, a physical connection). The horizontal connection bridge CTH is connected to the vertical connection bridge CTV. The vertical connection bridge CTV has a relatively large width in the second direction Y, which facilitates connections to word lines WL at different locations, and can maintain that the word line WL extends in the first direction X without requiring the word line to bend or wind.

[0028] In some memories, the memory includes multiple layers of stacked memory structure, and each layer of the memory structure includes multiple memory array tiles Mat arranged in an array. Each memory array tile Mat includes multiple memory arrays subMat arranged in the second direction Y. Word line contact structures CT corresponding to different memory arrays subMat stacked in a third direction Z are also stacked in the third direction Z. The third direction Z is perpendicular to the first direction X and the second direction Y, and the third direction Z may be a vertical direction.

[0029] Ideally, the horizontal connection bridges CTH and the vertical connection bridges CTV in different word line contact structures CT stacked in the third direction Z have completely overlapping orthographic projections in the third direction Z, but the contact pads CTP do not overlap at least partially. In this way, different contact pads CTP can be separately connected to different word line drivers via conductive plugs extending in the third direction Z. In FIG. 3, a digit marked for the contact pad CTP represents which layer at which the contact pad CTP is located. It may be learned that contact pads at different layers are staggered. For example, an extension length of the contact pad CTP at a first layer is longer than an extension length of the contact pad CTP at a third layer, the projection of the contact pad CTP at the third layer is located in the projection of the contact pad CTP at the first layer, and the contact pad CTP at the third layer and the contact pad CTP at a fourth layer are arranged in the first direction X.

[0030] Referring to FIG. 4, the memory includes multiple memory array tiles Mat arranged in the first direction X. Word line contact structures CT are disposed on two opposite

sides of each memory array tile Mat in the first direction X. Bit line contact structures SAP are disposed on two opposite sides in the second direction Y, the bit line contact structure SAP is configured to connect to a sense amplifier, and the sense amplifier is configured to amplify the voltage of a common bit line in the memory array tile Mat.

[0031] It may be learned from the foregoing description that the memory shown in FIG. 1 to FIG. 4 has the following features: ① In the first direction X, the word line contact structure CT is disposed between adjacent memory arrays subMat, or different memory arrays subMat are divided via the word line contact structure CT. ② Each word line contact structure CT is connected to only word lines WL in memory arrays subMat on two adjacent sides, and a case that three or more memory arrays subMat arranged consecutively share one word line contact structure CT does not exist. ③ The structure of the word line contact structure CT is relatively complex, and a parasitic capacitance is easily generated between the contact pad CTP of the same word line contact structure CT and the vertical connection bridge CTV. Two contact pads CTP of different word line contact structures CT possibly have overlapping orthographic projections, and a parasitic capacitance is also easily generated. ④ Memory cells between adjacent memory array tiles Mat are blocked by the word line contact structure CT, a spacing between adjacent memory array tiles Mat is large, and the density of the memory cells is relatively low.

[0032] FIG. 5 to FIG. 12 are schematic structural diagrams of a memory according to embodiments of this application.

[0033] Referring to FIG. 5, the memory includes memory arrays subMat and word line drivers SWD, where the word line drivers SWD are configured to drive word lines WL in the memory arrays subMat, the word lines WL include first-type word lines and second-type word lines, the word line drivers SWD include first drivers SWD1 and second drivers SWD2, the first drivers SWD1 are configured to drive the first-type word lines, and the second drivers SWD2 are configured to drive the second-type word lines; and connection bridges Br, including first connection bridges Br1 and second connection bridges Br2, where the first-type word lines are connected to the first drivers SWD1 via the first connection bridges Br1, and the second-type word lines are connected to the second drivers SWD2 via the second connection bridges Br2; an extension direction of each of the connection bridges Br1 is the

same as a first direction, a direction of each of the first connection bridges Br1 toward the second connection bridges Br2 is perpendicular to the first direction X, and the first direction X is an extension direction of each of the word lines WL.

[0034] In this embodiment of this application, by controlling the direction of the first connection bridge Br1 toward the second connection bridge Br2 perpendicular to an extension direction of the connection bridge Br, it is helpful to avoid that one of the first connection bridge Br1 and the second connection bridge Br2 affects an extension of the other, so that the first connection bridge Br1 and the second connection bridge Br2 can extend in the first direction. Therefore, the first connection bridge Br1 can be connected to first-type word lines in more than two memory arrays subMat, and the second connection bridge Br2 can be connected to second-type word lines in more than two memory arrays subMat. In this way, it is helpful to reduce a quantity of word line contact structures, reduce the size of the memory in the extension direction of the word line, reduce a memory area, and increase the density of memory cells in the first direction.

[0035] The embodiments of this application are described in more detail below with reference to the accompanying drawings.

[0036] In some embodiments, for example, in FIG. 5, in a second direction Y, a word line WL connected to an odd-numbered memory cell is an odd-numbered word line OWL, and a word line WL connected to an even-numbered memory cell is an even-numbered word line EWL. The first-type word line is an odd-numbered word line OWL, the second-type word line is an even-numbered word line EWL, and memory cells corresponding to a pair of the odd-numbered word line OWL and the even-numbered word line WL share a local bit line LBL. Every two non-repeated memory cells share a local bit line LBL, and the odd-numbered word line OWL and the even-numbered word line EWL cannot be activated simultaneously. Otherwise, data in the two memory cells is output simultaneously. Therefore, the odd-numbered word line OWL and the even-numbered word line EWL are driven via different word line drivers SWD.

[0037] The memory array subMat is a planar structure, and an extension direction of the local bit line LBL is perpendicular to a plane in which the memory array subMat is located. An extension direction of the common bit line CBL is the second direction Y, the common bit

line CBL is configured to connect to local bit lines LBL at the same location in different memory arrays subMat arranged in the second direction Y, and a plane formed by the common bit line CBL and the word line WL is parallel to a plane in which the memory array subMat is located.

[0038] Further, in the embodiment shown in FIG. 5, because the extension direction of the word line WL is the same as an extension direction of the connection bridge Br, an intermediate bridge structure needs to be disposed to connect the word line WL and the connection bridge Br parallel disposed. The intermediate bridge structure includes a first intermediate bridge MB1 and a second intermediate bridge MB2. The first intermediate bridge MB1 is configured to connect the odd-numbered word line OWL and the first connection bridge Br1, and the second intermediate bridge MB2 is configured to connect the even-numbered word line EWL and the second connection bridge Br2. Both the first intermediate bridge MB1 and the second intermediate bridge MB2 need to cross the intermediate region of the memory array subMat. In other words, the locations of the first intermediate bridge MB1 and the second intermediate bridge MB2 in the second direction Y overlap at least partially. In this case, the first connection bridge Br1 and the second connection bridge Br2 cannot be disposed in the intermediate region of the memory array subMat without employing a jumper.

[0039] It is assumed that the memory array subMat includes a first memory sub-array Gr1 and a second memory sub-array Gr2 arranged in the second direction Y. The size of the first memory sub-array Gr1 is the same as the size of the second memory sub-array Gr2, and the intermediate region of the memory array subMat is a region between the first memory sub-array Gr1 and the second memory sub-array Gr2.

[0040] In some embodiments, a jumper may be employed to avoid a conflict between the first connection bridge Br1 and the second intermediate bridge MB2, and avoid a conflict between the second connection bridge Br2 and the first intermediate bridge MB1, so that the first connection bridge Br1 and the second connection bridge Br2 are parallel disposed in the intermediate region of the memory array subMat. "Jumper" means a measure of temporarily connecting a conductive wire of a conductive layer to another conductive layer to bypass a conflicting region.

[0041] In some embodiments, for example, in FIG. 5, the first connection bridge Br1 and the second connection bridge Br2 are located on two opposite sides of the memory array subMat in the second direction Y, the second direction Y is perpendicular to the first direction X, and the second direction is an extension direction of the common bit line CBL. In this way, memory cells of the same memory array subMat can be disposed together, which facilitates simplifying a process manufacture procedure, and avoids introducing another factor affecting performance of the memory cell.

[0042] In some embodiments, every two non-repeated memory cells in the second direction Y do not share a local bit line LBL, and local bit lines corresponding to different memory cells are different. In this case, it is not necessary to set the odd-numbered word line and the even-numbered word line to be driven by different word line drivers. In this scenario, the first-type word line may be a word line in the first memory sub-array Gr1, and the second-type word line may be a word line in the second memory sub-array Gr2. In this case, if the first connection bridge and the second connection bridge are parallel disposed in the intermediate region of the memory array, the first connection bridge is close to the first memory sub-array, and the second connection bridge is close to the second memory sub-array, the first intermediate bridge and the second intermediate bridge do not overlap with each other in the second direction Y. Therefore, there is no wiring conflict problem. Alternatively, the first connection bridge is disposed in the intermediate region of the first memory sub-array, and the second connection bridge is disposed in the intermediate region of the second memory sub-array. In this case, the first intermediate bridge and the second intermediate bridge do not overlap with each other in the second direction Y.

[0043] In still some other embodiments, adjacent memory cells do not share a local bit line. Each memory array includes at least three memory sub-arrays sequentially arranged in the second direction Y. Each memory sub-array has a corresponding intermediate bridge and a connection bridge. The connection bridge may be disposed in the intermediate region of a corresponding memory sub-array or disposed on a side of the memory sub-array in the second direction. Connection bridges corresponding to different memory sub-arrays may be disposed adjacent to each other, and the locations of intermediate bridges corresponding to different memory sub-arrays do not overlap with each other in the second direction.

[0044] The intermediate bridge extends in the second direction, and the intermediate bridge is configured to connect a corresponding word line in a memory sub-array and a corresponding connection bridge. The capacity of different memory sub-arrays (the quantity of memory cells included) may be different. Locations of intermediate bridges corresponding to different memory sub-arrays in the first direction X may be the same or different. It may be understood that discussing whether the different intermediate bridges are completely staggered, at least partially overlap with each other, or are aligned in the second direction is independent of the locations of the different intermediate bridges in the first direction X.

[0045] The memory cell includes a data storage element and a storage transistor. The data storage element represents different data via different statuses or parameters of the data storage element, to store data. The data storage element may be a capacitor element, a resistor element, a magnetic element, or the like. The gate of the storage transistor is connected to a word line, the source thereof is connected to a local bit line, and the drain thereof is connected to the data storage element. When the word line is activated, the storage transistor is turned on to read and write data.

[0046] In some embodiments, referring to FIG. 5, at least three memory arrays subMat sequentially arranged in the extension direction of the word line WL (that is, in the first direction X) share the first connection bridge Br1 and the second connection bridge Br2. In the first direction X, different memory arrays subMat belong to different memory array tiles Mat. Each memory array tile Mat has a corresponding bit line contact structure, multiple bit line contact structures corresponding to the same memory array tile Mat are concentrated in the same connection region and evenly distributed, and bit line contact structures corresponding to different memory array tiles Mat are concentrated in different connection regions and different connection regions are spaced apart. Therefore, a specific location of the memory array tile can be determined via a region in which the bit line contact structure is located, thereby determining a quantity of memory arrays subMat sharing the first connection bridge Br1 and the second connection bridge Br2 in the first direction X.

[0047] In some embodiments, referring to FIG. 6, multiple memory arrays subMat sharing the same first connection bridge Br1 and the same second connection bridge Br2 form an array group. The first connection bridge Br1 is connected to the first driver (not shown in the

figure) via a first word line contact pad WLP1, and the second connection bridge Br2 is connected to the second driver (not shown in the figure) via a second word line contact pad WLP2. The first word line contact pad WLP1 and the second word line contact pad WLP2 are located only on two opposite sides of some memory arrays subMat in the array group in the second direction, or in other words, located in a part of regions on two opposite sides of the array group in the second direction. In other embodiments, the second direction intersects the first direction but is not perpendicular to the first direction.

[0048] In the embodiment shown in FIG. 6, eight memory arrays subMat form one array group AG. Each array group AG shares the same first connection bridge Br1, each first connection bridge Br1 corresponds to one first word line contact pad WLP1, and one first word line contact pad WLP1 corresponding to each array group AG is located on one side of one memory array subMat in the array group AG. Correspondingly, each array group shares the same second connection bridge Br2, each second connection bridge Br2 corresponds to one second word line contact pad WLP2, and one second word line contact pad WLP2 corresponding to each array group AG is located on one side of one memory array subMat in the array group AG.

[0049] In addition, in the embodiment shown in FIG. 6, multiple array groups AG are stacked in the third direction Z. The orthographic projections of first word line contact pads WLP1 corresponding to array groups AG at different layers in the third direction X are arranged in the first direction X. In other words, the orthographic projections of the first word line contact pads WLP1 corresponding to the array groups AG at the different layers in the third direction Z are in the same row. However, in FIG. 3, the orthographic projections of contact pads CTP corresponding to memory arrays at different layers in the third direction Z are in at least four rows. In the third direction Z, the orthographic projections of the array groups at the different layers may be considered as completely overlapping, the orthographic projections of connection bridges and intermediate bridges corresponding to the array groups at the different layers may be considered as completely overlapping, and a set of the orthographic projections of the first word line contact pads WLP1 corresponding to the array groups at the different layers is located on one side of the orthographic projections of some memory arrays subMat in the array group. The third direction is perpendicular to the first

direction and the second direction, and the third direction may be a vertical direction.

[0050] Specifically, the memory includes multiple layers of memory structures stacked in the vertical direction, each layer of memory structure has multiple memory arrays arranged in an array, and an array group is formed by multiple memory arrays that are arranged in the first direction and that share the same first connection bridge. In other words, the memory includes multiple layers of array groups stacked in the vertical direction, each array group AG has a corresponding first connection bridge Br1, each first connection bridge Br1 is connected to only one first word line contact pad WLP1, and the projections of the first word line contact pads WLP1 corresponding to the array groups AG at the different layers in the vertical direction are arranged in the first direction. The vertical direction is perpendicular to a plane on which the memory array subMat is located. In other words, the vertical direction is perpendicular to the first direction and the second direction.

[0051] In this way, because different first word line contact pads WLP1 have non-overlapping projections in the vertical direction, which facilitates reducing a parasitic capacitance between the different first word line contact pads WLP1, and facilitates reducing a quantity of first word line contact pads WLP1 adjacent to the first intermediate bridge MB1, and increasing the distance between the first intermediate bridge MB1 and the first word line contact pad WLP1, thereby reducing a parasitic capacitance between the first intermediate bridge MB1 and the first word line contact pad WLP1. In addition, the first word line contact pad WLP1 no longer blocks adjacent memory arrays subMat, which facilitates increasing the density of memory cells of the memory.

[0052] In addition, in the embodiment shown in FIG. 6, the first word line contact pad WLP1 is located between a corresponding first connection bridge Br1 and the memory array subMat, and the second word line contact pad WLP2 is located between a corresponding second connection bridge Br2 and the memory array. A first word line contact pad WLP1 and a second word line contact pad WLP2 corresponding to the same array group have overlapping orthographic projections in the second direction Y. First word line contact pads WLP1 corresponding to different array groups have overlapping orthographic projections in the second direction Y, and second word line contact pads WLP2 corresponding to the different array groups have overlapping orthographic projections in the second direction Y. In

this way, the first connection bridge Br1 is relatively away from the memory array subMat, which facilitates avoiding an increase in the leakage rate of an adjacent memory cell due to a potential change of the connection bridge Br.

[0053] In another embodiment, each first connection bridge Br1 is in contact connection with two or more first word line contacts WLP1, and multiple first word line contact pads WLP1 are disposed on the first connection bridge Br1 at equal intervals. Referring to FIG. 7, each first connection bridge Br1 is connected to three first word line contact pads WLP1. The three first word line contact pads WLP1 are evenly disposed at different locations of the first connection bridge Br1. In addition, the first word line contact pads WLP1 are not disposed at two ends of the first connection bridge Br1, and the three first word line contact pads WLP1 evenly separate the first connection bridge Br1 into four segments. In an embodiment shown in FIG. 8, the first word line contact pads WLP1 are disposed at the two ends of the first connection bridge Br1, and the three first word line contact pads WLP1 evenly separate the first connection bridge Br1 into two segments.

[0054] To be specific, a difference between FIG. 7 and FIG. 8 lies in that N first word line contact pads WLP1 evenly separate the first connection bridge Br1 into (N+1) segments in FIG. 7, and the N first word line contact pads WLP1 evenly separate the first connection bridge Br1 into (N–1) segments in FIG. 8, where N is a natural number greater than 2. A connection manner of the second connection bridge Br2 and the second word line contact pad WLP2 may be similar to that of the first connection bridge Br1 and the first word line contact pad WLP1. Details are not described again. However, it should be noted that the first word line contact pads WLP1 are disposed on the first connection bridge Br1 at equal intervals, and only the distance between adjacent first word line contact pads WLP1 is required to be equal, and the distance between an end point of the first connection bridge Br1 and an adjacent first word line contact pad WLP1 is not required to be equal to the distance between the adjacent first word line contact pads WLP1.

[0055] In the embodiment shown in FIG. 8, the drive capabilities of word line drivers connected to the first word line contact pads WLP1 at the two ends of the first connection bridge Br1 may be weaker than the drive capability of a word line driver connected to a first word line contact pad WLP1 at another location. In this way, when the drive capabilities at

different locations on the first connection bridge Br1 can be kept balanced, the size of a part of the word line drivers is reduced, and the size of the memory is reduced.

[0056] In an embodiment shown in FIG. 7, the memory includes multiple layers of array groups stacked in the vertical direction. Each array group has a corresponding first connection bridge Br1, and each first connection bridge Br1 is connected to multiple first word line contact pads WLP1. The projections of first word line contact pads WLP1 that correspond to array groups at different layers and that are in the same order are arranged in the first direction. In FIG. 7, the "same order" refers to orders of the first word line contact pads WLP1 on the first connection bridge Br1 in the first direction. For example, the leftmost first word line contact pad WLP1 is numbered 1, the middle first word line contact pad WLP1 is numbered 2, and the rightmost first word line contact pad WLP1 is numbered 3.

[0057] In another embodiment, refer to FIG. 9. FIG. 9 has at least two differences from FIG. 7. ① The first connection bridge Br1 is located between a corresponding first word line contact pad WLP1 and the array group AG, and the second connection bridge Br2 is located between a second word line contact pad WLP2 and the array group AG. ② The first word line contact pad WLP1 and the second word line contact pad WLP2 corresponding to the same array group AG have staggered orthographic projections in the second direction Y (a "stagger" refers to having a different location in the first direction X). First word line contact pads WLP1 corresponding to different array groups have overlapping orthographic projections in the second direction Y, and second word line contact pads WLP2 corresponding to the different array groups have overlapping orthographic projections in the second direction Y. In this way, corresponding first word line contact pads WLP1 and second word line contact pads WLP2 that are located between adjacent array groups AG are arranged alternately in the first direction X. This facilitates increasing space utilization of the memory, and avoids the waste of space between adjacent first word line contact pads WLP1 and space between adjacent second word line contact pads WLP2 in the first direction X.

[0058] It should be noted that, in comparison with FIG. 7, the foregoing two distinguishing points in FIG. 9 may be separately implemented in different embodiments, and are not limited to being implemented together.

[0059] In different embodiments, the word line driver SWD and the memory array subMat

may be in the same wafer or different wafers. If the word line driver SWD is located in a first wafer with a first bonding pad, and the memory array subMat is located in a second wafer with a second bonding pad, the second bonding pad of the second wafer is electrically connected to the first bonding pad of the first wafer via a bonding process such as hybrid bonding. An output end of the word line driver SWD is electrically connected to the first bonding pad, and the first word line contact pad WLP1 and the second word line contact pad WLP2 may be electrically connected to different second bonding pads via a vertical conductive plug.

[0060] In different embodiments, the ratio of the quantities of first connection bridges, first word line contact pads, and first drivers may be set based on a requirement, and the ratio of the quantities of second connection bridges, second word line contact pads, and second drivers may also be set based on a requirement. The first connection bridges, the first word line contact pads, and the first drivers are taken as an example, and there are at least the following several possibilities: Referring to FIG. 10, each first connection bridge Br1 is in contact connection with only one first word line contact pad WLP1, and each first word line contact pad WLP1 is connected to one first driver SWD1. Alternatively, referring to FIG. 11, each first connection bridge Br1 is in contact connection with multiple first word line contact pads WLP1, and each first word line contact pad WLP1 is connected to a different first driver SWD1. Alternatively, each first connection bridge Br1 is in contact connection with multiple first word line contact pads WLP1, and each first word line contact pad WLP1 is connected to the same first driver SWD1. In both FIG. 10 and FIG. 11, that three memory arrays subMat form one array group is taken as an example. In FIG. 11, that each first connection bridge Br1 is in contact connection with three first word line contact pads WLP1, and each first word line contact pad WLP1 is connected to a different first driver SWD1 is taken as an example.

[0061] In some embodiments, referring to FIG. 12, first intermediate bridges MB1 of every two adjacent memory arrays subMat are combined together, and second intermediate bridges MB2 of every two memory arrays subMat are combined together. To be specific, odd-numbered word lines in the two memory arrays subMat are connected to the first connection bridge Br1 via the same first intermediate bridge MB1 after combination, and even-numbered word lines in the two memory arrays subMat are connected to the second connection bridge

Br2 via the same second intermediate bridge MB2 after combination.

[0062] Specifically, in the extension direction of the word line WL, an even-numbered word line EWL in an Nth memory array subMat shares the second intermediate bridge MB2 with an even-numbered word line EWL in an (N+1)th memory array to connect to the second connection bridge Br2. An odd-numbered word line OWL in the (N+1)th memory array subMat shares the first intermediate bridge MB1 with an odd-numbered word line OWL in an (N+2)th memory array to connect to the first connection bridge Br1, where N is a positive integer.

[0063] In another embodiment, in the extension direction of the word line WL, an odd-numbered word line OWL in an Nth memory array subMat shares the first intermediate bridge MB1 with an odd-numbered word line OWL in an (N+1)th memory array subMat to connect to the first connection bridge Br1. An even-numbered word line EWL in the (N+1)th memory array subMat shares the second intermediate bridge MB2 with an even-numbered word line EWL in an (N+2)th memory array to connect to the second connection bridge Br2, where N is a positive integer.

[0064] When the distance between a word line contact pad and a part of a corresponding word line is possibly relatively far, to enhance a driven capability of the word line, the length of the word line may be shortened, to ensure that a far end of each word line can also be effectively driven. In some embodiments, at least one memory array has a word line whose length is shorter than the length of a word line in another memory array. When the length of the word line is shortened, the quantity of memory cells connected to the word line also decreases. In this case, when the total quantity of memory cells remains unchanged, the memory cells may be divided into more memory arrays with a smaller capacity, and each first connection bridge is connected to more first intermediate bridges, to shorten the length of a conductive path between the far end of the word line (one end thereof not connected to the intermediate bridge) and the word line contact pad, thereby improving drive efficiency of the word line driver.

[0065] A person of ordinary skill in the art may understand that the foregoing implementations are specific embodiments for implementing this application. In actual application, various modifications may be made to the forms and details of the

implementations without departing from the spirit and scope of this application. Any person skilled in the art may make changes and modifications without departing from the spirit and scope of this application. Therefore, the protection scope of this application shall be subject to the scope defined by the claims.

CLAIMS

What is claimed is:

1. A memory, comprising:

memory arrays and word line drivers, the word line drivers being configured to drive word lines in the memory arrays, the word lines comprising first-type word lines and second-type word lines, the word line drivers comprising first drivers and second drivers, the first drivers being configured to drive the first-type word lines, and the second drivers being configured to drive the second-type word lines; and

connection bridges, comprising first connection bridges and second connection bridges, the first-type word lines being connected to the first drivers via the first connection bridges, and the second-type word lines being connected to the second drivers via the second connection bridges; and an extension direction of each of the connection bridges being the same as a first direction, a direction of each of the first connection bridges toward the second connection bridges being perpendicular to the first direction, and the first direction being an extension direction of each of the word lines.

2. The memory according to claim 1, wherein the first-type word lines are odd-numbered word lines, the second-type word lines are even-numbered word lines, the first connection bridges and the second connection bridges are located on two opposite sides of the memory arrays in a second direction, the second direction is perpendicular to the first direction, and the second direction is an extension direction of a common bit line.

3. The memory according to claim 2, wherein at least three memory arrays sequentially arranged in the extension direction of each of the word lines share one of the first connection bridges and one of the second connection bridges, and share one of the first drivers and one of the second drivers.

4. The memory according to claim 3, wherein a plurality of ones of the memory arrays sharing a same one of the first connection bridges and a same one of the second connection bridges form an array group, the first connection bridges are connected to the first drivers via first word line contact pads, the second connection bridges are connected to the second drivers via second word line contact pads, and the first word line contact pads and the second word line contact pads are located on two opposite sides of only a part of the memory arrays in the

array group in the second direction.

5. The memory according to claim 4, wherein each of the first connection bridges is in contact connection with only one of the first word line contact pads, and each of the first word line contact pads is connected to one of the first drivers; or each one of the first connection bridges is in contact connection with a plurality of ones of the first word line contact pads, and each first word line is in bonding connection with different ones of the first drivers; or each of the first connection bridges is in contact connection with a plurality of ones of the first word line contact pads, and the plurality of ones of the first word line contact pads are connected to a same one of the first drivers.

6. The memory according to claim 5, wherein each of the first connection bridges is in contact connection with the plurality of ones of the first word line contact pads, and the plurality of ones of the first word line contact pads are disposed on each of the first connection bridges at equal intervals.

7. The memory according to claim 4, wherein the memory comprises a plurality of layers of the array groups stacked in a vertical direction, each of the first connection bridges is connected to only one of the first word line contact pads, and projections of the first word line contact pads in the vertical direction corresponding to the array groups at different layers are arranged in the first direction.

8. The memory according to claim 4, wherein the memory comprises a plurality of layers of the array groups stacked in a vertical direction, each of the first connection bridges is connected to a plurality of ones of the first word line contact pads, and projections of the first word line contact pads in the vertical direction that correspond to the array groups at different layers and that are in a same order are arranged in the first direction.

9. The memory according to claim 4, wherein the first connection bridges are located between corresponding ones of the first word line contact pads and the array groups, and the second connection bridges are located between corresponding ones of the second word line contact pads and the array groups.

10. The memory according to claim 9, wherein the first word line contact pads and the second word line contact pads corresponding to a same one of the array groups have staggered orthographic projections in the second direction, the first word line contact pads

corresponding to different ones of the array groups have overlapping orthographic projections in the second direction, and the second word line contact pads corresponding to different ones of the array groups have overlapping orthographic projections in the second direction.