DUAL ACTIVE LAYERS FOR SEMICONDUCTOR DEVICES AND METHODS OF MANUFACTURING THE SAME

STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT

[0001] The U.S. Government has a paid-up license in this invention and the right in limited circumstances to require the patent owner to license to others on reasonable terms as provided by the terms of Grant/Contract No. W911NF-04-2-0005 by the Army Research Lab (ARL).

CROSS-REFERENCE TO RELATED APPLICATIONS

[0002] This application claims the benefit of U.S. Provisional Application No. 61/472,992, filed April 7, 2011. U.S. Provisional Application No. 61/472,992 is incorporated herein by reference in its entirety.

[0003] This application is a continuation-in-part application of PCT Application No. PCT/US10/36569, filed May 28, 2010. PCT Application No. PCT/US10/36569 claims the benefit of U.S. Provisional Application No. 61/182,464, filed May 29, 2009, and U.S. Provisional Application No. 61/230,051, filed July 30, 2009. Meanwhile, PCT Application No. PCT/US10/36569 is a continuation-in-part application of (a) PCT Application No. PCT/US09/66114, filed November 30, 2009, which claims priority to U.S. Provisional Application No. 61/119,303, filed December 2, 2008; (b) PCT Application No. PCT/US09/66111, filed November 30, 2009, which claims priority to U.S. Provisional Application No. 61/119,248, filed December 2, 2008; and (c) PCT Application No. PCT/US09/66259, filed December 1, 2009. PCT Application No. PCT/US09/66259 claims the benefit of: (i) U.S. Provisional Application No. 61/119,217, filed December 2, 2008; (ii) U.S. Provisional Application No. 61/182,464; and (iii) U.S. Provisional Application No. 61/230,051.

[0004] PCT Application No. PCT/US10/36569, U.S. Provisional Application No. 61/182,464, U.S. Provisional Application No. 61/230,051, PCT Application No PCT/US09/66114, U.S. Provisional Application No. 61/119,303, PCT Application No PCT/US09/66111, U.S. Provisional Application No. 61/119,248, PCT Application No PCT/US09/66259, and U.S. Provisional Application No. 61/119,217 are incorporated herein by reference in their entirety.

FIELD OF THE INVENTION

[0005] This invention relates generally to semiconductor devices, and relates more particularly to semiconductor devices having dual active layers and methods of manufacturing the same.

DESCRIPTION OF THE BACKGROUND

[0006] Thin film transistors are commonly used to power a wide variety of display technologies including liquid crystal displays, electrophoretic displays, organic light emitting diode displays, etc. Many thin film transistors use amorphous silicon as an active layer, but using amorphous silicon can be disadvantageous as a result of the low mobility and low on/off ratio of amorphous silicon. Likewise, the high temperature processing temperatures of amorphous silicon can also be disadvantageous when fabricating flexible displays.

[0007] Accordingly, a need or potential for benefit exists for systems and methods for manufacturing the same that allow improved active layer mobility and on/off ratios while permitting reduced temperature processing.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] To facilitate further description of the embodiments, the following drawings are provided in which:

[0009] FIG. 1 illustrates an example of a method of providing a semiconductor device, according to a first embodiment;

[0010] FIG. 2 illustrates an example of a procedure of providing a flexible substrate, according to the first embodiment;

[0011] FIG. 3 illustrates an example of a process of preparing the flexible substrate, according to the first embodiment;

[0012] FIG. 4 illustrates a top view of an example of the flexible substrate according to the first embodiment;

[0013] FIG. 5 illustrates a partial cross-sectional view of an example of a flexible substrate assembly after attaching the flexible substrate of FIG. 4 to a protective template, according to the first embodiment;

[0014] FIG. 6 illustrates a partial cross-sectional view of an example of the flexible substrate assembly of FIG. 5 after coupling a carrier substrate to the flexible substrate assembly, according to the first embodiment;

[0015] FIG. 7 illustrates an example of a process of processing the flexible substrate assembly of FIG. 5, according to the first embodiment;

[0016] FIG. 8 illustrates a cross-sectional view of an example of the flexible substrate assembly of FIG. 5 after cutting the flexible substrate assembly, according to the first embodiment;

[0017] FIG. 9 illustrates a cross-sectional view of an example of the flexible substrate assembly of FIG. 5 after removing an alignment tab, according to the first embodiment;

[0018] FIG. 10 illustrates a cross-sectional view of an example of the flexible substrate assembly of FIG. 5 after removing a protective material from the flexible substrate assembly, according to the first embodiment;

[0019] FIG. 11 illustrates an example of a procedure of providing semiconductor elements, according to the first embodiment;

[0020] FIG. 12 illustrates an example of a process of providing one or more first semiconductor elements, according to the first embodiment;

[0021] FIG. 13 illustrates a cross-sectional view of an example of a device build area of a semiconductor device after providing a gate metal layer, according to the first embodiment;

[0022] FIG. 14 illustrates a cross-sectional view of an example of a gate contact build area of a semiconductor device after providing the gate metal layer, according to the first embodiment;

[0023] FIG. 15 illustrates a cross-sectional view of an example of the device build area of the semiconductor device of FIG. 13 after providing an active stack layer, according to the first embodiment;

[0024] FIG. 16 illustrates a cross-sectional view of an example of the gate contact build area of the semiconductor device of FIG. 14 after providing the active stack layer, according to the first embodiment;

[0025] FIG. 17 illustrates a cross-sectional view of an example of the device build area of the semiconductor device of FIG. 13 after providing a mesa passivation layer, according to the first embodiment;

[0026] FIG. 18 illustrates a cross-sectional view of an example of the gate contact build area of the semiconductor device of FIG. 14 after providing the mesa passivation layer, according to the first embodiment;

[0027] FIG. 19 illustrates a cross-sectional view of an example of the device build area of the semiconductor device of FIG. 13 after conducting one or more post-mesa passivation layer etches, according to the first embodiment;

[0028] FIG. 20 illustrates a cross-sectional view of an example of the gate contact build area of the semiconductor device of FIG. 14 after conducting one or more post-mesa passivation layer etches, according to the first embodiment;

[0029] FIG. 21 illustrates a cross-sectional view of an example of the device build area of the semiconductor device of FIG. 13 after providing one or more contact elements, according to the first embodiment;

[0030] FIG. 22 illustrates a cross-sectional view of an example of the gate contact build area of the semiconductor device of FIG. 14 after providing one or more contact elements, according to the first embodiment;

[0031] FIG. 23 illustrates an example of a process of providing a first dielectric material, according to the first embodiment;

[0032] FIG. 24 illustrates a cross-sectional view of an example of the device build area of the semiconductor device of FIG. 13 after etching a base dielectric material, a first dielectric material, and a second dielectric material, according to the fist embodiment;

[0033] FIG. 25 illustrates a cross-sectional view of an example of the device build area of the semiconductor device of FIG. 13 after providing a second metal layer and an ITO layer, according to the first embodiment;

[0034] FIG. 26 illustrates a cross-sectional view of an example of the device build area of the semiconductor device of FIG. 13 after providing a silicon nitride layer, according to the first embodiment;

[0035] FIG. 27 illustrates an example of a method of planarizing a flexible substrate, according to a second embodiment;

[0036] FIG. 28 illustrates a cross-sectional view of an example of a semiconductor device according to the method of FIG. 27, according to the second embodiment;

[0037] FIG. 29 illustrates a top view of a portion of a semiconductor device, according to the first embodiment;

[0038] FIG. 30 illustrates a graph of thickness of a dielectric material versus spin rate of a substrate;

[0039] FIG. 31 illustrates an exemplary method of manufacturing a semiconductor device, according to an embodiment;

[0040] FIG. 32 illustrates a cross-sectional view of a device build area of an exemplary semiconductor device after providing a gate metal layer over the substrate;

[0041] FIG. 33 illustrates a cross-sectional view of a gate contact building area of an exemplary semiconductor device after providing a gate metal layer over the substrate;

[0042] FIG. 34 is a flow chart illustrating a procedure of providing the transistor active layer over the gate metal layer, according to the embodiment of FIG. 31;

[0043] FIG. 35 illustrates a cross-sectional view of an example of the device build area of the semiconductor device of FIG. 32 after providing an etch stop layer over the transistor active layer;

[0044] FIG. 36 illustrates a cross-sectional view of an example of the gate contact build area of the semiconductor device of FIG. 33 after providing an etch stop layer over the transistor active layer;

[0045] FIG. 37 illustrates a cross-sectional view of an example of the device build area of the semiconductor device of FIG. 32 after providing a mesa passivation layer over and/or on the etch stop layer;

[0046] FIG. 38 illustrates a cross-sectional view of an example of the gate contact build area of the semiconductor device of FIG. 33 after providing a mesa passivation layer over and/or on the etch stop layer;

[0047] FIG. 39 illustrates a cross-sectional view of an example of the device build area of the semiconductor device of FIG. 32 after the one or more port-mesa passivation layer etches have been conducted;

[0048] FIG. 40 illustrates a cross-sectional view of an example of the gate contact build area of the semiconductor device of FIG. 33 after the one or more port-mesa passivation layer etches have been conducted;

[0049] FIG. 41 illustrates a cross-sectional view of an example of the device build area of the semiconductor device of FIG. 32 after providing a source/drain contact layer over the transistor active layer, the first active layer, and/or the second active layer;

[0050] FIG. 42 illustrates a cross-sectional view of an example of the gate contact build area of the semiconductor device of FIG. 33 after providing a source/drain contact layer over the transistor active layer, the first active layer, and/or the second active layer;

[0051] FIG. 43 illustrates a cross-sectional view of an example of the device build area of the semiconductor device of FIG. 32 after performing one or more additional procedures;

[0052] FIG. 44 illustrates a cross-sectional view of an example of the device build area of the semiconductor device of FIG. 32 after providing one or more semiconductor elements, according to an embodiment;

[0053] FIG. 45 illustrates a cross-sectional view of an example of the device build area of the semiconductor device of FIG. 32 after providing one or more semiconductor elements, according to a different embodiment than the embodiment of FIG. 44;

[0054] FIG. 46 illustrates a top view of a portion of an exemplary semiconductor device;

[0055] FIG. 47 illustrates a cross-sectional view of an example of the device build area of the semiconductor device of FIG. 32 after providing a first active layer over and/or on the gate metal layer and providing a second active layer over and/or on the first active layer, according to an embodiment;

[0056] FIG. 48 is a flow chart illustrating a procedure of providing a source/drain contact layer over the transistor active layer, the first active layer, and/or the second active layer, according to the embodiment of FIG. 1; and

[0057] FIG. 49 is a flowchart illustrating a procedure of providing a gate metal layer over the substrate, according to the embodiment of FIG. 1.

[0058] For simplicity and clarity of illustration, the drawing figures illustrate the general manner of construction, and descriptions and details of well-known features and techniques may be omitted to avoid unnecessarily obscuring the invention. Additionally, elements in the drawing figures are not necessarily drawn to scale. For example, the dimensions of some of the elements in the figures may be exaggerated relative to other elements to help improve understanding of embodiments of the present invention. The same reference numerals in different figures denote the same elements.

[0059] The terms "first," "second," "third," "fourth," and the like in the description and in the claims, if any, are used for distinguishing between similar elements and not necessarily for describing a particular sequential or chronological order. It is to be understood that the terms so used are interchangeable under appropriate circumstances such that the embodiments described herein are, for example, capable of operation in sequences other than those illustrated or otherwise described herein. Furthermore, the terms "include," and "have," and any variations thereof, are intended to cover a non-exclusive inclusion, such that a process, method, system, article, device, or apparatus that comprises a list of elements is not necessarily limited to those elements, but may include other elements not expressly listed or inherent to such process, method, system, article, device, or apparatus.

[0060] The terms "left," "right," "front," "back," "top," "bottom," "over," "under," and the like in the description and in the claims, if any, are used for descriptive purposes and not necessarily for describing permanent relative positions. It is to be understood that the terms so used are interchangeable under appropriate circumstances such that the embodiments of the invention described herein are, for example, capable of operation in other orientations than those illustrated or otherwise described herein.

[0061] The terms "couple," "coupled," "couples," "coupling," and the like should be broadly understood and refer to connecting two or more elements or signals, electrically, mechanically and/or otherwise. Two or more electrical elements may be electrically coupled but not be mechanically or otherwise coupled; two or more mechanical elements may be mechanically coupled, but not be electrically or otherwise coupled; two or more electrical elements may be

mechanically coupled, but not be electrically or otherwise coupled. Coupling may be for any length of time, e.g., permanent or semi-permanent or only for an instant.

[0062] "Electrical coupling" and the like should be broadly understood and include coupling involving any electrical signal, whether a power signal, a data signal, and/or other types or combinations of electrical signals. "Mechanical coupling" and the like should be broadly understood and include mechanical coupling of all types.

[0063] The absence of the word "removably," "removable," and the like near the word "coupled," and the like does not mean that the coupling, etc. in question is or is not removable.

DETAILED DESCRIPTION OF EXAMPLES OF EMBODIMENTS

[0064] Some embodiments include an electronic device. In many embodiments, the electronic device can comprise a transistor. The transistor can comprise a gate metal layer, a transistor active layer over the gate metal layer, and a source/drain contact layer over the transistor active layer. The source/drain contact layer can comprise a first source/drain contact and a second source/drain contact. In the same or different embodiments, the transistor active layer can comprise a first active layer over the gate metal layer, where the first active layer comprises at least one first metal oxide. In the same or different embodiments, the transistor active layer can comprise a second active layer over the first active layer, where the second active layer comprises at least one second metal oxide. In some embodiments, the first active layer comprises a first conductivity, the second active layer comprises a second conductivity, and the first conductivity is greater than the second conductivity.

[0065] Various embodiments include a semiconductor device. In many embodiments, the semiconductor device comprises a substrate, a barrier layer on the substrate, a gate metal layer on the barrier layer, a gate barrier layer on the gate metal layer, a transistor active layer on the gate barrier layer, an etch stop layer on the transistor active layer, a mesa passivation layer on the etch stop layer, and a source/drain contact layer on the mesa passivation layer and the transistor active layer. In the same or different embodiments, the transistor active layer comprises a first active layer on the gate metal layer, where the first active layer comprising at least one first metal oxide. In the same or different embodiments, the transistor active layer comprises a second active layer on the first active layer and between the first active layer and the etch stop layer, where the second active layer comprises at least one second metal oxide. In some embodiments, the first active layer comprises a first conductivity, the second active layer comprises a second conductivity, and the first conductivity is greater than the second conductivity.

[0066] Further embodiments include a method of manufacturing a semiconductor device. The method comprises: providing a substrate; providing a gate metal layer over the substrate; providing a first active layer over the gate metal layer, where the first active layer comprises at least one first metal oxide and a first conductivity; providing a second active layer over the first active layer, where the second active layer comprises at least one second metal oxide and a second conductivity less than the first conductivity; and providing a source/drain contact layer over the second active layer.

[0067] The term "bowing" as used herein means the curvature of a substrate about a median plane, which is parallel to the top and bottom sides, or major surfaces of the substrate. The term "warping" as used herein means the linear displacement of the surface of a substrate with respect to a z-axis, which is perpendicular to the top and bottom sides, or major surfaces of the substrate. The term "distortion" as used herein means the displacement of a substrate in-plane (i.e., the x-y plane, which is parallel to the top and bottom sides, or major surfaces of the substrate). For example, distortion could include shrinkage in the x-y plane of a substrate and/or expansion in the x-y plane of the substrate.

[0068] The term "CTE matched material" as used herein means a material that has a coefficient of thermal expansion (CTE) which differs from the CTE of a reference material by less than about 20 percent (%). Preferably, the CTEs differ by less than about 10%, 5%, 3%, or 1%. As used herein, “polish” can mean to lap and polish a surface or to only lap the surface.

[0069] Turning to the drawings, FIG. 1 illustrates an example of a method 100 of providing a semiconductor device, according to a first embodiment. In the same or different embodiments, method 100 can be considered a method of providing a thin film transistor on a flexible substrate. Method 100 is merely exemplary and is not limited to the embodiments presented herein. Method 100 can be employed in many different embodiments or examples not specifically depicted or described herein.

[0070] Method 100 includes a procedure 110 of providing a flexible substrate. FIG. 2 is a flow chart illustrating procedure 110 of providing a flexible substrate, according to the first embodiment.

[0071] Procedure 110 includes a process 211 of furnishing a flexible substrate. The term "flexible substrate" as used herein means a free-standing substrate comprising a flexible material which readily adapts its shape. In some embodiments, process 211 can include furnishing a flexible substrate with a low elastic modulus. For example, a low elastic modulus can be considered an elastic modulus of less than approximately five GigaPascals (GPa).

[0072] In many examples, the flexible substrate is a plastic substrate. For example, flexible substrates can include polyethylene naphthalate (PEN), polyethylene terephthalate (PET), polyethersulfone (PES), polyimide, polycarbonate, cyclic olefin copolymer, or liquid crystal polymer.

[0073] In many examples, the flexible substrate can include a coating at one or more sides of the flexible substrate. The coating can improve the scratch resistance of the flexible substrate and/or help prevent outgassing or oligomer crystallization on the surface of the substrate. Moreover, the coating can planarize the side of the flexible substrate over which it is located. The coating also can help decrease distortion. In some examples, the coating is located only at the side of the flexible substrate where the electrical device will be fabricated. In other examples, the coating is at both sides of the flexible substrate. In various embodiments the flexible substrate can be provided pre-planarized. For example, the flexible substrate can be a PEN substrate from DuPont Teijin Films of Tokyo, Japan, sold under the tradename "planarized Teonex® Q65." In other embodiments, a flexible substrate can be planarized after being provided. For example, method 2700 (FIG. 27) provides a method of planarizing a substrate.

[0074] The thickness of the flexible or plastic substrate can be in the range of approximately 25 micrometers (μm) to approximately 300 μm. In the same or different embodiments, the thickness of the flexible or plastic substrate can be in the range of approximately 100 μm to approximately 200 μm.

[0075] In some examples, the flexible substrate can be provided by cutting a sheet of a plastic substrate from a roll of the plastic material using a paper cutter or a pair of ceramic scissors. In various examples, after cutting the plastic substrate, the cut sheet is blown clean with a nitrogen gun. In some embodiments of procedure 110, either or both of the cutting and blowing processes can be part of a process 212, described below, instead of being part of process 211.

[0076] Procedure 110 of FIG. 2 continues with process 212 of preparing the flexible substrate. FIG. 3 is a flow chart illustrating process 212 of preparing the flexible substrate, according to the first embodiment.

[0077] Process 212 of FIG. 2 can include an activity 330 of baking the flexible substrate. Baking the flexible substrate can help release oligomers and other chemicals in the flexible substrate that could potentially leach out later during method 100 (FIG. 1).

[0078] In some examples, the flexible substrate can be baked using a vacuum bake process. For example, the temperature in an oven containing the flexible substrate can be ramped up over approximately two to three hours to approximately 160 degrees Celsius (°C) to approximately

200°C. The flexible substrate can be baked for one hour at approximately 160°C to approximately 200°C and at a pressure of approximately one milliTorr (mTorr) to approximately ten mTorr. Then, the temperature in the oven can be lowered to between approximately 90°C to approximately 115°C, and the flexible substrate can be baked for approximately eight more hours. Other baking processes can be also be used. After the baking process is complete, the flexible substrate can be wiped clean of any residues or chemicals that were baked off.

[0079] Subsequently, process 212 of FIG. 3 includes an activity 331 of providing a protective template. The protective template can act as both a guide for the placement of the flexible substrate as well as a protective layer between the flexible substrate and the rollers and/or handling mechanisms of various processing equipment. In some examples, the protective template is a sheet of mylar or any inexpensive plastic.

[0080] The protective template can be 50 μm to 15 mm thick and cut to a length of approximately 0.5 m (meters) to approximately 1.5 m. In various embodiments, as part of activity 331, the protective template is folded in half and run through rollers (e.g., a hot roll laminator) to help lock in the fold. A line trace of a carrier substrate can also be made on the back side of the protective sheet as part of activity 331. Additionally, the protective template can be baked at approximately 90°C to approximately 110°C for approximately five minutes to approximately ten minutes to help flatten the protective template.

[0081] Process 212 of FIG. 3 continues with an activity 332 of applying a protective material to at least a portion of a first surface of the flexible substrate. In some embodiments, a protective material can be applied over at least a portion of a planarized surface of the flexible substrate. In some examples, the protective material is not applied to a portion of the flexible substrate.

[0082] The protective material prevents scratches and adhesive from covering the planarized surface of the flexible substrate and, thus, reduces defects. In some examples, blue low tack tape (e.g., from Semiconductor Equipment Corporation, part number 18133-7.50) or mylar could be used as the protective material. The protective material can be approximately 25 μm to approximately 100 μm thick. For example, the protective material can be approximately 70 μm thick. In some examples, the protective material is applied by rolling the protective material onto the planarized surface of the flexible substrate using a roller to remove air bubbles between the protective material and the flexible substrate.

[0083] Subsequently, process 212 of FIG. 3 includes an activity 333 of cutting the flexible substrate and protective material into the shape of a wafer. A punch cut template can be used to press the wafer shape into the flexible substrate (with the planarized side, if any, up) and/or the

protective material. In one embodiment, the punch cut template is used to create a temporary or permanent impression in the protective material and the flexible substrate at the same time.

[0084] If the pressing of the punch cut template cuts completely through the flexible substrate, the flexible substrate is scrapped because the press cut can create cracks in a coating on the flexible substrate that propagate throughout the flexible substrate. After the wafer shape is outlined into the flexible substrate and/or the protective material using the press, the flexible substrate and the protective material are cut simultaneously with each other. In some examples, the flexible substrate and protective material are cut using ceramic scissors approximately one millimeter outside the impression made by the punch cut template.

[0085] In some examples, the flexible substrate includes a tab extending from the wafer shape in the flexible substrate and the protective material. The tab can be used to help align the flexible substrate to a carrier substrate when traveling through a laminator in process 217 of FIG. 2. FIG. 4 illustrates a top view of a flexible substrate 450, according to a first embodiment. Flexible substrate 450 can include a body 452 and tab 451. In many examples, body 452 can have a circular shape. Although not illustrated in FIG. 4, the protective material is located over flexible substrate 450 also includes a similarly shaped tab. In one embodiment, the tab is not part of the punch cut template and is cut freehand or freestyle into the flexible substrate and the protective material.

[0086] Referring back to FIG. 3, process 212 of FIG. 3 continues with an activity 334 of cleaning the flexible substrate. In some examples, the second or non-planarized side of the flexible substrate (i.e., the side without the protective material) is dry wiped to remove any oligomers, other chemicals, or particles. Afterwards, the planarized side of the flexible substrate having the protective material is blown clean with a nitrogen gun. In other examples, both sides of are dry wiped and/or blown clean.

[0087] Next, process 212 of FIG. 3 includes an activity 335 of aligning the flexible substrate with a protective template. In some examples, the flexible substrate having the wafer shape with the tab is aligned with the line trace of a carrier substrate drawn or made on the protective template in activity 331. The line trace of the carrier substrate is typically slightly larger than the wafer shape of the flexible substrate.

[0088] Subsequently, process 212 of FIG. 3 includes an activity 336 of coupling the flexible substrate to the protective template. In some embodiments, the flexible substrate is attached to the protective template by attaching a portion of the tab of the flexible substrate to the protective template. For example, a piece of double-sided tape can couple the tab of the flexible substrate to the protective template. In some examples, a portion of the protective material is peeled off

of and removed from the tab, and the double-sided tape is coupled to the exposed portion of the tab of the flexible substrate. In some examples, the portion of the protective material can be peeled using tweezers and can be cut from the protective template using a pair of ceramic scissors. In other examples, in activity 332 of FIG. 3, the protective material is not applied to the portion the tab to which the double-sided tape will be attached so peeling and removal of a portion of the protective material is not necessary.

[0089] After coupling the flexible substrate to the protective coating, the protective template is then folded over the flexible substrate. FIG. 5 illustrates a partial cross-sectional view of a flexible substrate assembly 540 after attaching flexible substrate 450 to a protective template 555, according to the first embodiment. In this example, a tape 556 is coupled to flexible substrate 450 and protective template 555. A protective material 553 is coupled to flexible substrate 450, as described previously.

[0090] In some examples, only one side of the flexible substrate is attached to the protective template. In other examples, both sides of the flexible substrate are attached to the protective template.

[0091] Next, process 212 of FIG. 3 includes an activity 337 of laminating the flexible substrate, the protective material, and the protective template. The flexible substrate and the protective material are located between the two folded halves of the protective template. The flexible substrate, the protective material, and the protective template can be laminated using a hot roll laminator to remove air bubbles between the protective material and the protective template and also between the protective material and the flexible substrate. In some examples, the flexible substrate and the protective template are placed over a guide sheet (e.g., a Lexan® guide sheet) and fed into the hot roll laminator. As an example, the tab of the flexible substrate and the protective material can be fed first into the laminator. The flexible substrate and the protective template are laminated at a pressure of approximately 120 kPa (kilopascals) to approximately 160 kPa and at a temperature of approximately 90°C to approximately 110°C. The lamination speed can be approximately one meter per minute to approximately two meters per minute.

[0092] After laminating the flexible substrate and protective template, process 212 is complete. Referring back to FIG. 2, procedure 110 of FIG. 2 includes a process 213 of providing a carrier substrate. In many embodiments, the carrier substrate can be a 6, 8, 12, or 18 inch wafer or panel. In some embodiments the carrier substrate can be a panel of approximately 370 mm by 470 mm.

[0093] The carrier substrate can include a first surface and a second surface opposite the first surface. In some examples, at least one of the first surface and the second surface has been polished. Polishing the surface that is not subsequently coupled to the flexible substrate improves the ability of a vacuum or air chuck to handle the carrier substrate. Also, polishing the surface that is subsequently coupled to the flexible substrate removes topological features of the surface of the carrier substrate that could cause roughness of the flexible substrate assembly in the z-axis after the coupling with the flexible substrate.

[0094] In various embodiments, the carrier substrate comprises at least one of the following: alumina (Al_2O_3), silicon, low CTE glass, steel, sapphire, barium borosilicate, soda lime silicate, an alkali silicate, or another material that is CTE matched to the flexible substrate. The CTE of the carrier substrate should be matched to the CTE of the flexible substrate. Non-matched CTEs can create stress between the carrier substrate and the flexible substrate.

[0095] For example, the carrier substrate could comprise sapphire with a thickness between approximately 0.7 mm and approximately 1.1 mm. The carrier substrate could also comprise 96% alumina with a thickness between approximately 0.7 mm and approximately 1.1 mm. In a different embodiment, the thickness of the 96% alumina is approximately 2.0 mm. In another example, the carrier substrate could be a single crystal silicon wafer with a thickness of at least approximately 0.65 mm. In still a further embodiment, the carrier substrate could comprise stainless steel with a thickness of at least approximately 0.5 mm. In some examples, the carrier substrate is slightly larger than the flexible substrate.

[0096] Next, procedure 110 of FIG. 2 includes a process 214 of providing a cross-linking adhesive. In some examples, the cross-linking adhesive outgases at a rate of less than approximately 2 x 10-4 Torr-liters per second. In some examples, the cross-linking adhesive is thermally and/or UV (ultraviolet) light curable.

[0097] In various embodiments, the cross-linking adhesive is a cross-linking acrylic adhesive. In the same or different embodiment, the cross-linking adhesive is a cross-linking pressure sensitive acrylic adhesive or a cross-linking viscoelastic polymer. In some examples, the CTE of the adhesive is very large compared to the CTE of the flexible substrate and the carrier substrate. However, the CTE of the adhesive is not important because the adhesive does not create any stress (i.e., viscoelasticity) between the flexible substrate and carrier substrate because the layer of adhesive is so thin compared to the thickness of the flexible substrate and carrier substrate.

[0098] Subsequently, procedure 110 of FIG. 2 includes a process 215 of depositing the cross-linking adhesive over a first surface of the carrier substrate. In many embodiments,

depositing the cross-linking adhesive over a first surface of the carrier substrate can be performed using at least one of the following methods: spin-coating, spray-coating, extrusion coating, preform lamination, slot die coating, screen lamination, and screen printing.

[0099] For example, the carrier substrate can be coated with the cross-linking adhesive. The carrier substrate and the cross-linking adhesive can be spun to distribute the cross-linking adhesive over a first surface of the carrier substrate. In some embodiments, the cross-linking adhesive is spin coated on the carrier substrate by spinning the carrier substrate with the cross-linking adhesive at approximately 900 rpm (revolutions per minute) to 1100 rpm for approximately 20 seconds to approximately 30 seconds and then spinning the carrier substrate with the cross-linking adhesive at approximately 3400 rpm to approximately 3600 rpm for approximately 10 seconds to 30 seconds. In a different embodiment, the carrier substrate with the cross-linking adhesive is spun at approximately 600 rpm to approximately 700 rpm to coat the surface of the carrier substrate and then spun at approximately 3400 rpm to approximately 3600 rpm to control the thickness of the cross-linking adhesive.

[00100] Prior to spin coating, the cross-linking adhesive can be dispensed onto or over a geometric center of the carrier substrate. In a different embodiment, the cross-linking adhesive can be dispensed onto or over the carrier substrate while the carrier substrate is spinning.

[00101] The thickness of the cross-linking adhesive over the carrier substrate after the depositing procedure can be between approximately three μm and approximately fifteen μm. In the same or different embodiment, the thickness of the cross-linking adhesive over the carrier substrate after the depositing procedure can be between approximately ten μm and approximately twelve μm.

[00102] Procedure 110 of FIG. 2 continues with a process 216 of baking the cross-linking adhesive. In some embodiments, the cross-linking adhesive can be baked to remove solvents. For example, the cross-linking adhesive can be baked at 80°C for thirty minutes and then baked for fifteen minutes at 130°C.

[00103] In other examples, the cross-linking adhesive is not baked. For example, if the cross-linking adhesive does not include any solvents, a bake is not necessary. Moreover, if the cross-linking adhesive is very viscous, solvents may even be added to the cross-linking adhesive to decrease the viscosity before the adhesive is deposited in process 215.

[00104] Afterwards, the carrier substrate can be placed on the protective template. The flexible substrate is already coupled to one portion (or half) of the protective template as shown in FIG. 6, and the carrier substrate with cross-linking adhesive can be placed on another portion (or half) of the protective template. In some examples, the cross-linking adhesive is still in

liquid form at this point. Thus, the carrier substrate coated with the cross-linking adhesive can be stored horizontally for approximately eight to approximately twelve hours before being coupled with the flexible substrate.

[00105] Next, procedure 110 of FIG. 2 includes a process 217 of coupling the carrier substrate to the flexible substrate using the cross-linking adhesive while both substrates are located between the protective template halves. The second surface of the flexible substrate can be placed over the first surface of the carrier substrate with the adhesive located between the second surface of the flexible substrate and the first surface of the carrier substrate.

[00106] In some examples, the carrier substrate is coupled to the flexible substrate using the cross-linking adhesive by laminating the flexible substrate assembly between the protective template halves to remove air bubbles between the carrier substrate and the flexible substrate. Laminating the flexible substrate involves first aligning the carrier substrate with the flexible substrate so that, when laminated, the carrier substrate and the flexible substrate are aligned. Then, the aligned structure can be fed through a hot roll laminator, which can be the same laminator of activity 337 of FIG. 3. The flexible substrate assembly can be laminated at an approximate speed of 0.4 to 0.6 meters per minute.

[00107] Also, in various embodiments, the protective material may stick to the protective template when laminated. To avoid this problem, a shield material can be located between the protective template and the protective material before the lamination of activity 337 and/or activity 332. The shield material can be, for example, wax paper. In one embodiment, the shield material is originally coupled to the protective material when acquired from the manufacturer.

[00108] In the same or different embodiments, some of the cross-linking adhesive can be squeezed out from between the carrier and flexible substrates during lamination and adhere to the first side or the top of the flexible substrate, particularly because the carrier substrate and the overlying cross-linking adhesive layer is slightly larger than the flexible substrate. The presence of the protective material, however, prevents this problem from occurring. The cross-linking adhesive that squeezes out and adheres to the top of the protective material (instead of the flexible substrate) is inconsequential because the protective material is eventually removed and discarded.

[00109] FIG. 6 illustrates a partial cross-sectional view of flexible substrate assembly 540 after coupling a carrier substrate 651 to flexible substrate assembly 540, according to the first embodiment. In this embodiment, a cross-linking adhesive 652 couples a surface 661 of carrier substrate 651 to a surface 662 of flexible substrate 450. Protective material 553 is located over a

surface 656 of flexible substrate 450. A shield material 654 is located between protective material 553 and protective template 555. Protective template 555 is folded such that protective template 555 is also located under a surface 663 of carrier substrate 651. Tape 556 couples protective template 555 to tab 451 of flexible substrate 450.

[00110] Referring again back to FIG. 2, procedure 110 continues with a process 218 of processing the flexible substrate assembly. FIG. 7 is a flow chart illustrating process 218 of processing the flexible substrate assembly, according to the first embodiment.

[00111] Process 218 of FIG. 7 includes an activity 730 of cutting the flexible substrate assembly. In some examples, a pair of ceramic scissors is used to cut the protective template and across the alignment tab of the flexible substrate located between the protective template, but the alignment tab is not removed entirely. After cutting the flexible substrate assembly, the protective template can be peeled away from or otherwise removed from the shield material and the carrier substrate by hand. FIG. 8 illustrates a cross-sectional view of flexible substrate assembly 540 after cutting the flexible substrate assembly and removing the protective template, according to the first embodiment. More specifically, in FIG. 8, protective template 555 (FIGs. 5 & 6), and tape 556 (FIGs. 5 & 6) of flexible substrate 450 have been removed.

[00112] Referring again to FIG. 7, the next activity in process 218 is an activity 731 of removing the shield material by hand. In some examples, the flexible substrate assembly is placed at an edge of a table with the shield material facing the table. The flexible substrate assembly is slowly moved off the table while the shield layer is removed (e.g., peeled) from the flexible substrate assembly. That is, the shield layer can be removed by pulling the shield material downward away from the edge of the table while the flexible substrate assembly is moved horizontally off the table. In some examples, if the flexible substrate is not properly centered on or otherwise aligned with the carrier substrate after removing the shield layer, the plastic substrate can be slid into alignment with the carrier substrate.

[00113] Subsequently, process 218 of FIG. 7 includes an activity 732 of removing the alignment tab from the flexible assembly. In some examples, the alignment tab can be cut from the flexible substrate using ceramic scissors. The cut should be made slowly as any movement of the flexible substrate in the z-direction (relative to the carrier substrate) might cause de-lamination of the flexible substrate from the carrier substrate. If de-lamination occurs, the flexible substrate assembly can be re-laminated. FIG. 9 illustrates a cross-sectional view of flexible substrate assembly 540 after removing the alignment tab, according to the first embodiment.

[00114] Next, process 218 of FIG. 7 includes an activity 733 of cleaning the flexible substrate assembly. In some examples, the flexible substrate assembly is cleaned with hexanes. The hexanes can be applied by spinning the flexible substrate assembly and spraying the hexanes on the protective material. After the protective material is cleaned, the exposed surface and edge of the carrier substrate is wiped clean with hexanes.

[00115] Procedure 218 of FIG. 7 continues with an activity 734 of curing the cross-linking adhesive. In the same or different embodiment, the cross-linking adhesive is UV cured. For example, the flexible substrate assembly can be exposed to UV light for approximately 15 to 25 seconds and room temperature to cure the cross-linking adhesive. In some embodiments, the cross-linking adhesive can be cured with UV light in the UV light range of approximately 320 nm (nanometers) to approximately 390 nm and with an intensity of approximately 75 mW/cm2 (milliWatts per square centimeter). A Dymax 2000-EC UV Curing Flood Lamp, manufactured by Dymax Corporation of Torrington, Connecticut, can be used to cure the cross-linking adhesive.

[00116] In various examples, the cross-linking adhesive is thermally cured during the baking in activity 736. In some examples, the edges of the cross-linking adhesive are UV cured, and the rest of the cross-linking adhesive is thermally cured during the baking of activity 736.

[00117] Subsequently, process 218 of FIG. 7 includes an activity 735 of removing the protective material from the flexible substrate assembly. In some examples, the protective material can be slowly removed using tweezers. During the removal process, the protective material is kept as flat as possible to avoid de-laminating the flexible substrate from the carrier substrate. In other examples, the protective material can be releasable by UV light. In these examples, the protective material would lose its tack during a UV light exposure. FIG. 10 illustrates a cross-sectional view of flexible substrate assembly 540 after removing the protective material from the flexible substrate assembly, according to the first embodiment.

[00118] Next, process 218 of FIG. 7 includes an activity 736 of baking the flexible substrate assembly. Baking the flexible substrate assembly can help decrease the distortion, bow, and warp in the flexible substrate. In some embodiments, baking can also cure the adhesive.

[00119] In some examples, the flexible substrate assembly can be baked using a vacuum bake process. For example, the temperature in an oven containing the flexible substrate assembly can be ramped up over two to three hours to approximately 160°C to approximately 190°C. The flexible substrate assembly can be baked for approximately 50 minutes to 70 minutes at 180°C and with a pressure of approximately 1 mTorr to approximately 10 mTorr. The temperature in the oven can then be lowered to between approximately 90°C to 115°C, and the flexible

substrate assembly can be baked for approximately seven more hours to approximately nine more hours. Other baking processes can be also be used. After the baking process is complete, the flexible substrate assemblies are cleaned and placed in an oven at approximately 90°C to 110°C for a minimum of approximately two hours.

[00120] After baking the flexible substrate assembly, process 218 is complete, and therefore, procedure 110 is also complete. Procedure 110, as described herein, and similar procedures can allow fabrication of one or more electrical components on a flexible substrate with zero or at least minimal distortion (e.g. approximately the limits of the sensitivity of an Azores 5200, manufactured by Azores Corporation of Wilmington, Massachusetts). Prior art methods of fabricating electrical components on the flexible substrate suffer from significant distortion problems that can lead to handling errors, photolithographic alignment errors, and line/layer defects.

[00121] Referring back to FIG. 1, method 100 includes a procedure 120 of providing semiconductor elements. FIG. 11 is a flow chart illustrating procedure 120 of providing semiconductor elements, according to the first embodiment.

[00122] Procedure 120 of FIG. 11 includes a process 1112 of providing one or more first semiconductor elements. FIG. 12 is a flow chart illustrating process 1112 of providing one or more first semiconductor elements, according to the first embodiment.

[00123] Process 1112 in FIG. 12 includes an activity 1211 of providing a gate metal layer. FIG. 13 illustrates a cross-sectional view of a device build area of an example of a semiconductor device 1350 after providing a gate metal layer, according to the first embodiment. As can be seen in FIG. 29, the cross-sectional view of the device build area is the cross-sectional view of a portion of semiconductor device 1350 taken at the "a" lines. The device build cross sectional view comprises a cross-sectional view of a-Si contact areas 2980 and via area 2982. In addition, FIG. 14 illustrates a cross-sectional view of a gate contact build area of an example of semiconductor device 1350 after providing a gate metal layer, according to the first embodiment. As can be seen in FIG. 29, the cross-sectional view of the gate contact build area is the cross-sectional view of a portion of semiconductor device 1350 taken at the "b" lines. The gate contact build cross sectional view comprises a cross-sectional view of gate contact area 2981. FIG. 29 is merely exemplary and is not limited to the embodiments presented herein.

[00124] Referring to FIGs. 13 and 14, for example, an approximately 0.30 μm thick silicon nitride passivation layer 1352 is provided over flexible substrate assembly 540. Silicon nitride passivation layer 1352 can be provided over flexible substrate 450 (FIG. 10) of flexible substrate

assembly 540. In some embodiments, flexible substrate 450 may baked prior to the deposition of silicon nitride passivation layer 1352.

[00125] In addition, a patterned metal gate 1353 can be provided over silicon nitride passivation layer 1352. Patterned metal gate 1353 can comprise molybdenum. In some examples, an approximately 0.15 μm layer of molybdenum can be deposited over silicon nitride passivation layer 1352 and then pattern etched to form patterned metal gate 1353. For example, molybdenum can be deposited over silicon nitride passivation layer 1352 by sputtering. In some examples, molybdenum can be deposited using a KDF 744, manufactured by KDF Electronic, Inc., of Rockleigh, New Jersey. In the same or different examples, patterned metal gate 1353 can be etched using an AMAT 8330, manufactured by Applied Material, Inc. of Santa Clara, California.

[00126] Subsequently, process 1112 of FIG. 12 includes an activity 1212 of providing an active stack. FIGs. 15 and 16 illustrate an example of semiconductor device 1350 after providing an active stack, according to the first embodiment.

[00127] Referring to FIGs. 15 and 16, for example a silicon nitride gate dielectric 1554 can be formed over patterned metal gate layer 1353 and silicon nitride passivation layer 1352. Referring to FIG. 15, for example, in the device build area of semiconductor device 1350, a patterned amorphous silicon (a-Si) layer 1555 can be provided over silicon nitride gate dielectric 1554, and a patterned silicon nitride intermetal dielectric (IMD) layer 1556 can be provided over a-Si layer 1555.

[00128] In some examples, as shown in FIGs. 15 and 16, silicon nitride gate dielectric 1554 can be deposited onto semiconductor device 1350 over metal gate layer 1353 and silicon nitride passivation layer 1352 by way of plasma-enhanced chemical vapor deposition (PECVD). In the same or different examples, silicon nitride gate dielectric 1554 can be approximately 0.30 μm thick.

[00129] With reference to FIG. 15, as an example, a-Si layer 1555 can be deposited over silicon nitride gate dielectric 1554 by way of PECVD. In the same or different examples, a-Si layer 1555 can be approximately 0.08 μm thick.

[00130] Also, as an example, silicon nitride IMD layer 1556 can be deposited over a-Si layer 1555 by way of PECVD. In the same or different examples, silicon nitride IMD layer 1556 can be approximately 0.10 μm thick.

[00131] In some examples, silicon nitride gate dielectric 1554, a-Si layer 1555, and silicon nitride IMD layer 1556 can all be deposited via PECVD using an AMAT P5000, manufactured by Applied Materials, Inc. of Santa Clara, California. In the same or different examples, the

temperature at which silicon nitride gate dielectric 1554, a-Si layer 1555, and silicon nitride IMD layer 1556 are deposited onto semiconductor device 1350 is greater than approximately 180°C. For example, the temperature at which silicon nitride gate dielectric 1554, a-Si layer 1555, and silicon nitride IMD layer 1556 are deposited onto semiconductor device 1350 is from approximately 180°C to approximately 250°C. As an example, the temperature at which silicon nitride gate dielectric 1554, a-Si layer 1555, and silicon nitride IMD layer 1556 are deposited onto semiconductor device 1350 is from approximately 188°C to approximately 193°C. Furthermore, the deposition of silicon nitride gate dielectric 1554, a-Si layer 1555, and silicon nitride IMD layer 1556 onto semiconductor device 1350 can be done at approximately vacuum.

[00132] After silicon nitride gate dielectric 1554, a-Si layer 1555, and silicon nitride IMD layer 1556 are deposited onto semiconductor device 1350, the resulting layers can be etched. For example, silicon nitride can be etched using a 10:1 buffered oxide etch (BOE). In addition, a-Si layer 1555 can be etched using an AMAT 8330. In some examples, silicon nitride IMD layer 1556 and a-Si layer 1555 are etched so that a-Si layer 1555 is exposed, i.e., a-Si layer 1555 is not completely covered by silicon nitride IMD layer 1556.

[00133] Next, process 1112 of FIG. 12 includes an activity 1213 of providing a mesa passivation layer. FIGs. 17 and 18 illustrate an example of semiconductor device 1350 after providing a mesa passivation layer, according to the first embodiment.

[00134] With reference to FIG. 17, as an example, in the device build area of semiconductor device 1350, mesa passivation layer 1757 is deposited onto semiconductor device 1350 over silicon nitride gate dielectric 1554, a-Si layer 1555, and silicon nitride IMD layer 1556. Mesa passivation layer 1757 can comprise silicon nitride. Mesa passivation layer 1757 can be deposited over a-Si layer 1555 to passivate and/or encapsulate the surface of a-Si layer 1555, thereby preventing contamination of the surface of a-Si layer 1555 and lowering leakage currents along the surface of a-Si layer 1555. With reference to FIG. 18, as an example, in the gate contact build area of semiconductor device 1350, mesa passivation layer 1757 can be deposited over silicon nitride gate dielectric 1554.

[00135] Mesa passivation layer 1757 can be deposited onto semiconductor device 1350 by way of PECVD. As an example, mesa passivation layer 1757 can be approximately 0.10 μm thick. In the same or different examples, mesa passivation layer 1757 can be deposited via PECVD using an AMAT P5000.

[00136] Subsequently, process 1112 of FIG. 12 includes an activity 1214 of conducting one or more post-mesa passivation layer etches. FIGs. 19 and 20 illustrate cross-sectional views of semiconductor device 1350 after one or more post-mesa passivation layer etches have been

conducted. For example, FIG. 20 illustrates semiconductor device 1350 after a contact gate etch has taken place in the gate contact build region of semiconductor device 1350. In the same or different examples, FIG. 19 illustrates semiconductor device 1350 after a contact a-Si etch has taken place in the device build region of semiconductor device 1350.

[00137] The contact gate etch of the gate contact build region of semiconductor device 1350 can etch away silicon nitride. For example, the contact gate etch can etch away mesa passivation layer 1757 and silicon nitride gate dielectric 1554. In many examples, the metal gate layer 1353 underneath silicon nitride gate dielectric 1554 functions as an etch stop for the etching process. The contact gate etch of the contact gate build region can be performed in a Tegal 903, manufactured by Tegal Corporation of Petaluma, California. After the contact gate etch, gate contact 2091 is formed on semiconductor device 1350. Gate contact 2091 is associated with gate contact area 2981 of FIG. 29.

[00138] The contact a-Si etch of the device build region of semiconductor device 1350 can etch away silicon nitride. For example, the contact a-Si etch can etch away mesa passivation layer 1757 and silicon nitride IMD layer 1556. The silicon nitride layers can be etched using a 10:1 BOE. a-Si layer 1555 under silicon nitride layer 1556 can act as an etch stop for the etching process. After the contact a-Si etch, a-Si contacts 1990 are formed on semiconductor device 1350. a-Si contacts 1990 are associated with a-Si contact areas 2980 of FIG. 29. In this embodiment, the contact a-Si etch and the contact gate etch can be separate etches using separate etch masks.

[00139] After activity 1214, process 1112 of FIG. 12 is completed. With reference to FIG. 11, procedure 120 continues with a process 1113 of providing one or more contact elements. FIG. 21 illustrates a cross-sectional view of a device build region of an example of semiconductor device 1350 after process 1113 has been completed. In addition, FIG. 22 illustrates a cross-sectional view of a gate contact build region of an example of semiconductor device 1350 after process 1113 has been completed.

[00140] In the example illustrated in FIG. 21, N+ a-Si layer 2159 is provided over portions of mesa passivation layer 1757, a-Si layer 1555, and silicon nitride IMD layer 1556. As illustrated in FIG. 21, diffusion barrier 2158 is provided over N+ a-Si layer 2159, and metal layer 2160 is provided over diffusion barrier 2158. Similarly, in the example of FIG. 22, N+ a-Si layer 2159 is provided over portions of mesa passivation layer 1757, silicon nitride gate dielectric 1554, and gate metal layer 1353. Also shown in FIG. 22, diffusion barrier 2158 is provided over N+ a-Si layer 2159, and metal layer 2160 is provided over diffusion barrier 2158.

[00141] N+ a-Si layer 2159 may be provided by way of PECVD. As an example, N+ a-Si layer 2159 can be approximately 0.05 μm thick. In the same or different examples, N+ a-Si layer 2159 can be deposited via PECVD using an AMAT P5000.

[00142] As an example, diffusion barrier 2158 can include tantalum (Ta). In the same or different examples, metal layer 2160 can include aluminum (Al). Diffusion barrier 2158 can help prevent movement of atoms from metal layer 2160, such as, for example, Al atoms, from diffusing into N+ a-Si layer 2159, and subsequently a-Si layer 1555. Diffusion barrier 2158 and metal layer 2160 can be deposited over N+ a-Si layer 2159 by way of sputtering. In some examples, diffusion barrier 2158 and metal layer 2160 can be deposited using a KDF 744.

[00143] After, N+ a-Si layer 2159, diffusion barrier 2158, and metal layer 2160 have been deposited onto semiconductor device 1350, the three layers are etched. As an example, the three layers can be etched using an AMAT 8330. In some examples, N+ a-Si layer 2159, diffusion barrier 2158, and metal layer 2160 are etched using a single recipe for all three of the layers. As an example, the N+ a-Si layer 2159, diffusion barrier 2158, and metal layer 2160 are etched using boron trichloride (BCl_3) with a flow rate of approximately 140 sccm (standard cubic centimeters per minute) and chlorine gas (Cl_2) with a flow rate of approximately 10 sccm at a pressure of approximately 20 mTorr for 1 minute and 45 seconds. Next, the Cl_2 is increased to 30 sccm, while the pressure is dropped to 10 mTorr for 15 minutes. Next, the BCl_3 rate is decreased to 30 sccm, and the pressure is increased to 15 mTorr. Finally, the BCl_3 and the Cl_2 flow rates are brought to zero, and oxygen (O_2) is brought in at 50 sccm with a pressure of 50 mTorr for 60 minutes.

[00144] In various embodiments, procedure 120 can include a process 1198 of providing a base dielectrically material. The base dielectric material can provide a uniform surface (e.g., a wetting layer) for the spin-on dielectric material (e.g., dielectric layers 2461 (FIG. 24)). In some examples, base dielectric material can include silicon oxide or silicon nitride. In many examples, the base dielectric material can be provided using a process similar or identical to the process used to provide the second dielectric material (i.e., process 1117), as described below. In other embodiments, procedure 120 does not include providing a base dielectric material.

[00145] Subsequently, procedure 120 includes a process 1114 of providing a first dielectric material. The first dielectric material can be provided over the one or more contact elements of process 1113. In some examples, the first dielectric material can be an organic siloxane-based dielectric material, organosiloxane dielectric material, and/or siloxane-based dielectric material. In various embodiments, the first dielectric material can be organic. Using an organic siloxane-based dielectric material can allow for thicker films and more flexible films than with a non-

organic siloxane-based dielectric material. In some examples, the first dielectric material can be used as an interlayer dielectric. In the other examples, the first dielectric material can be used as an intralayer dielectric.

[00146] Table 1 illustrates properties of an example of a dielectric material that can be used as the first dielectric material in process 1114, according to an embodiment.

Properties	**Dielectric Material**
Cure temperature	~400°C (when deposited over low temperature polysilicon) ~ 350°C (when deposited over amorphous silicon (a-Si)) < 200°C (when deposited over a flexible substrate)
Film Thickness	1.5 μm to 3.5 μm
Transmittance	> 95%
Planarization	> 95%
Resistance to plasma induced damage	Fluorine-based plasma (e.g., Sulfur hexafluorine (SF_6), carbon tetra fluorine (CF_4), trifluoromethane (CHF_3), O_2 plasma used for removing photoresist, and ashing
Adhesion	Aluminum (Al), chromium (Cr), indium tin oxide (ITO), silicon nitride (SiN), organic layers
Outgassing	Low (less than typical CVD chamber pressures)
Moisture uptake	Low moisture uptake
Dispense tool	Spin or slot die coaters, screen printers, spray coating

TABLE 1

[00147] As used in Table 1, film thickness refers to the desired thickness of the dielectric material that displays the other properties in the table. Transmittance refers to the percentage of light that is transmitted through the dielectric material. Planarization refers to the degree of planarization (DOP) of the dielectric material. Resistance to plasma induced damage indicates the plasmas that will not damage this film. Adhesion means the dielectric material can be coupled to at least these other materials. Outgassing can refer to outgassing pressure of the dielectric material or the rate at which the dielectric material outgases. Moisture uptake can refer to the rate at which moisture is absorbed by the dielectric material. Dispense tools refers to equipment that can be used to apply the dielectric material.

[00148] Table 2 illustrates properties of a second example of a dielectric material that can be used as the first dielectric material in process 1114, according to an embodiment.

Properties	Dielectric Material
Film Thickness	1 μm to 4 μm
Cure temperature	~180°C
Etch Chemistry	Standard plasma etch chemistries
Etch Rate	>0.25 μm per minute
Feature Size	< 5 μm
Dielectric Constant (k)	< 4.0
Breakdown Voltage	> 5 megavolts per centimeter (MV/cm)
Heat Resistance	≥ 250°C
Adhesion	Al, ITO, molybdenum (Mo), photoresist
Moisture Uptake	<0.2 wt % over 2 hours
Planarization	> 95%
Outgassing	No
Transparency	>95%

TABLE 2

[00149] As used in Table 2, etch chemistries refers to etch chemistries that can be used to etch the dielectric material. Etch rate is the minimum etch rate of the dielectric material when using the etch chemistries. Feature size refers to the smallest size of an element or feature formed with the dielectric material. Breakdown voltage is the voltage per length at which the dielectric material begins acting as a conductor. Heat resistance is the lowest temperature that the material can withstand before becoming unstable.

[00150] FIG. 23 illustrates an example of process 1114 of providing a first dielectric material. In various embodiments, the first dielectric material can be a spin-on-dielectric. Accordingly, in these examples, the dielectric can be applied to the semiconductor device by spin-coating the first dielectric material over the first metal layer and various silicon nitride layers. In various embodiments, the application of the first dielectric material can be performed in a Rite Track 8600 available from Rite Track, Inc., of West Chester, Ohio.

[00151] Referring to FIG. 23, process 1114 can include an activity 2330 of spinning the semiconductor device at a first predetermined rate. In some examples, the first predetermined spin rate is between approximately 500 rpm and approximately 2000 rpm. In same or different embodiment, the first predetermined rate is approximately 1000 rpm.

[00152] Subsequently, process 1114 can include an activity 2331 of dispensing the first dielectric material. In some examples, the first dielectric material is dispensed over the substrate while the substrate is spinning at the first predetermined rate. In some examples, the first

dielectric material can be dispensed using a syringe. If the substrate is a six inch diameter wafer, approximately 4 mL (milliliters) can be dispensed over the semiconductor device. In some examples, the pressure in the tip of the syringe during dispensing can be approximately 15 kPa. In the same or different embodiment, after the syringe dispenses the first dielectric material, the syringe has suck back pressure of approximately 1 kPa. The suck back pressure of the syringe prevents dripping additional amounts of the first dielectric material from the syringe after the dispensing process is complete. For a 6-in wafer, the dispensing process takes approximately 3 seconds. The semiconductor device is spun at the first predetermined rate until activity 2331 is complete.

[00153] In various embodiments, a dynamic dispensing process is used. That is, the substrate is spinning while the first dielectric material is dispensed. In some examples, the first dielectric material is dispensed at the center of the substrate. In other examples, at the beginning of the dispensing process, the syringe is located over the center of the substrate and moves from the center of the substrate to the edge of the substrate at a constant rate of approximately thirty to approximately sixty millimeters per second while the substrate is spinning. In other embodiments, a static dispensing process is used. That is, the substrate is not spun during the dispensing process.

[00154] Next, process 1114 includes an activity 2332 of ramping-up the speed of the semiconductor device from the first predetermined rate to a second predetermined rate. In some examples, the second predetermined spin rate is between approximately 2000 rpm and approximately 4000 rpm. In the same or different embodiment, the second predetermined rate is approximately 2600 rpm. Spinning the semiconductor device at the second predetermined rate of approximately 2600 rpm for approximately thirty seconds can distribute the first dielectric material with a thickness of approximately two μm over the surface of the semiconductor device. Different thicknesses of the first dielectric material can be achieved by using different second predetermined rates.

[00155] FIG. 30 is an illustration of thickness of the first dielectric material versus the spin rate (i.e., speed) of the semiconductor material.

[00156] Process 1114 can further include an activity 2333 of performing edge bead removal. In some examples, during activities 2331 and 2332, the first dielectric material flows outward due to the centrifugal force toward the edge of the substrate and creates a ridge (i.e., the edge bead) on the top side edge of the semiconductor device. The edge bead, when dried, could flake off and increase defects of the semiconductor device and/or damage the manufacturing equipment. Accordingly, the edge bead is removed in activity 2333. In some examples, the

equipment used in activities 2331 and 2332 can include an edge bead removal device. In some examples, a solvent is sprayed on the edge bead to remove the first dielectric material around the edge of the substrate. In some examples, while the semiconductor device is spun at a third predetermined rate, a solvent is sprayed over, for example, approximately five to approximately six millimeters inside the edge of the substrate. In some examples, removing the first dielectric material from the edges of the substrate also helps to ensure that when a second dielectric material is provided over the first dielectric material (process 1117 of FIG. 11), the edges of the first dielectric material are capped by a second dielectric material.

[00157] In some examples, cyclohexanone, propylene glycol monomethyl ether acetate (PGMEA), or other edge bead removing solvents can be used. In some examples, the semiconductor device is rotated at a third predetermined rate of approximately 1000 rpm during the edge bead removal process. In some examples, the semiconductor device is spun at the third predetermined rate for approximately thirty seconds, and solvent is sprayed on the bead edge during this time.

[00158] Subsequently, process 1114 continues with an activity 2334 of stopping the spinning of the semiconductor device. After the spinning of the semiconductor device is stopped, process 1114 is complete.

[00159] Referring back to FIG. 11, procedure 120 includes a process 1115 of baking the semiconductor device. In some examples, baking the semiconductor device includes baking the first dielectric material of process 1114, the one or more contact elements of process 1113, the one or more first semiconductor elements of process 1112, and the substrate of procedure 110. One of the purposes of the bake is to cause evaporation of the solvents from the edge bead process. Baking the semiconductor device can also increase planarization, decrease film defects, and cross-link the first dielectric material.

[00160] In various embodiments, the baking of the semiconductor device is performed using a two bake sequence. The baking process can be performed at atmospheric pressure using a hot plate. Process 1115 can be performed, for example, in a Rite Track 8800.

[00161] The first bake is a bake for approximately sixty seconds at approximately 160°C. In an alternative example, the first bake can be an approximately sixty second bake at approximately 150°C. After the first bake is complete, in some examples, the semiconductor device is allowed to cool for approximately thirty seconds before the second bake. The semiconductor device can be allowed to cool at room temperature (and not using a chill plate). The semiconductor device is allowed to cool, in these examples, because the handling system uses polytetrafluoroethylene (e.g., Teflon® material from E. I. du Pont de Nemours and

Company of Wilmington, Delaware) coated chucks to handle the semiconductor device. Placing a hot semiconductor device on the polytetrafluoroethylene coated chuck can damage the chuck. If other equipment is used, the cooling process can possibly be skipped.

[00162] After letting the semiconductor device cool, the semiconductor device can be baked for a second time on a hot plate. In some embodiments, the second bake can be for approximately sixty seconds at a temperature greater than approximately 160°C because 160°C is the boiling point of PGMEA. For example, if the first bake was at the 160°C, the second bake can be for approximately sixty seconds at approximately 170°C. If the first bake was at the 150°C, the second bake can be for approximately sixty seconds at approximately 200°C. After the second bake is complete, the semiconductor device can be cooled again for thirty seconds. In other embodiments, other sequences of bakes can be performed.

[00163] After the baking is complete, the next process in procedure 120 is a process 1116 of curing the first dielectric material. Curing of the first dielectric material can improve the cross-linking of the first dielectric material. In some examples, the curing can be performed in a convection oven in a nitrogen atmosphere at atmospheric pressure (i.e., approximately one atmosphere).

[00164] In various examples, the semiconductor device can be placed in the oven. Afterwards, the temperature in the oven can be ramped-up to approximately 200°C, and the semiconductor device can be baked for approximately one hour at approximately 200°C. The temperature is ramped-up a rate of approximately 1-2°C per minute to minimize outgassing of the first dielectric material of process 1114. After the bake is complete, the temperature is slowly ramped down (e.g., 1-2°C per minute) to room temperature.

[00165] In another embodiment, a baking procedure with five separate bakes can be used. The first bake can be a bake at approximately 60°C for approximately ten minutes. The ramp-up time to approximately 60°C from room temperature is approximately ten minutes. After baking at approximately 60°C, the temperature is ramped-up over approximately thirty-two minutes to approximately 160°C. The semiconductor device is baked for approximately thirty-five minutes at approximately 160°C.

[00166] The temperature of the convection oven is then increased to approximately 180°C over approximately ten minutes after the 160°C bake. The semiconductor device is baked for approximately twenty minutes at approximately 180°C.

[00167] After baking at 180°C, the temperature is ramped-up over approximately fifty minutes to approximately 200°C. The semiconductor device is baked for approximately sixty minutes at approximately 200°C. Finally, in this bake procedure, the temperature in the oven is

ramped-down to approximately 60°C over approximately seventy minutes. The semiconductor device is baked for approximately ten minutes at approximately 60°C. After baking is complete, the semiconductor device is allowed to cool to approximately room temperature before proceeding with procedure 120 of FIG. 11. The baking of the semiconductor device can help anneal the one or more contact elements.

[00168] Subsequently, procedure 120 includes a process 1117 of providing a second dielectric material. In some examples, providing the second dielectric material can include depositing the second dielectric material over the organosiloxane dielectric layer (i.e., the first dielectric material of process 1114). In some examples, the second dielectric material can comprise silicon nitride. In the same or different examples, the second dielectric material can include silicon oxynitride (SiO_xN_y), silicon oxide, and/or silicon dioxide (SiO_2). In some examples, a low temperature PECVD process can be used to deposit the second dielectric material. In some examples, as part of providing the second dielectric material, the first dielectric material is capped by the second dielectric material. In some examples, the edges of the first dielectric material can be capped by the second dielectric material so the first dielectric material is not exposed to any subsequent oxygen (O_2) plasma ashings. Oxygen plasma ashings can degrade the first dielectric material in some examples.

[00169] The second dielectric material can be deposited with a thickness of approximately 0.1 μm to approximately 0.2 μm. The second dielectric material can be deposited to protect the first dielectric material from later etches.

[00170] The next process in procedure 120 is a process 1118 of providing a mask over the second dielectric material. The mask applied in process 1118 can be an etch mask for an etching activity of process 1119 of FIG. 11.

[00171] In some examples, process 1118 can include applying a patterned photoresist over the siloxane-based dielectric layer (i.e., the first dielectric material of process 1114) or patterning a mask over the organic siloxane-based dielectric (i.e., the first dielectric material of process 1114). Similarly, process 1118 can include providing a patterned mask over the organosiloxane dielectric layer (i.e., the first dielectric material of process 1114).

[00172] In some examples, the mask covers one or more portions of the first dielectric material and the second dielectric material that are not to be etched. The mask can be provided with a thickness such that the mask is not etched through during the etching process of process 1119 of FIG. 11. In some examples, the mask can have a thickness of approximately 3.5 μm or approximately 2.5 μm to approximately 5.0 μm.

[00173] In some examples, the mask comprises photoresist. In some examples, the photoresist can be AZ Electronic Materials MiR 900 Photoresist, manufactured by AZ Materials of Luxembourg, Luxembourg. In some examples, the photoresist is coated over the second dielectric material using the Rite Track 8800. For example, the semiconductor device can be vapor primed and spin-coated with the mask (e.g., the photoresist). After coating the semiconductor device, the semiconductor device is baked at approximately 105°C for approximately sixty seconds.

[00174] Next, the semiconductor device is aligned to the correct position with a template and exposed to UV (ultraviolet) light to transfer the mask image from the template to the mask. After exposing the mask, the semiconductor device is baked for approximately ninety seconds at approximately 110°C. The mask is then developed using an approximately ninety second puddle with standard development chemicals to remove the portions of the photoresist that were not exposed to the UV light.

[00175] After the development is completed, the last portion of providing the mask over the second dielectric material is performing a photoresist reflow process on the mask. Photoresist reflow is the process of heating the mask after the photoresist has been developed to cause the photoresist to become at least semi-liquid and flow.

[00176] In some examples, the semiconductor device is baked at approximately 140 °C for approximately sixty seconds. This photoresist reflow process will decrease the sharpness of the edges of the mask, and thus, when etched in process 1119 of FIG. 11, the vias in the first dielectric and the second dielectric will have sloped sides. In some examples, the sloped sizes are at an angle of approximately thirty degrees from horizontal.

[00177] Next, procedure 120 includes a process 1119 of etching the base dielectric material, the first dielectric material, and the second dielectric material. The base dielectric material, the first dielectric material, and the second dielectric material are etched to create vias in the base dielectric material, the first dielectric material, and the second dielectric material.

[00178] In some examples, the base dielectric material, the first dielectric material, and the second dielectric material are etched in the same process using the same etch mask. In other examples, the first dielectric material is etched in a first process, and the second dielectric is etched in a second process, and the base dielectric is etched in a third process.

[00179] In these other examples, a mask can be applied to the base dielectric material; the base dielectric material can be etched; and the mask can be removed before the first dielectric material is provided in process 1114 of FIG. 11. Subsequently, a mask can be applied to the first dielectric material; the first dielectric material can be etched; and the mask can be removed

before the second dielectric material is provided in process 1118 of FIG. 11. Then, a mask can be applied to the second dielectric material, and the second dielectric material can be etched. In another example, the second dielectric material can be etched using the mask of process 1118; the mask can be removed; and the patterned second dielectric material can be used as the mask for patterning the first dielectric material.

[00180] In many embodiments, the base dielectric material, the first dielectric material, and the second dielectric material are plasma etched. In the same of different embodiments, the base dielectric material, the first dielectric material, and the second dielectric material are reactive ion etched (RIE). In some examples, the base dielectric material, the first dielectric material, and the second dielectric material are etched with a fluorine-based etchant. In some examples, the etchant can be trifluoromethane (CHF_3), sulfur hexafluoride (SF_6), or other fluorine-based etchants.

[00181] In some examples where there is no base dielectric material (i.e., process 1198 is skipped), the first material can be the organosiloxane dielectric material described previously, and the second material can be silicon nitride. In these examples, the first dielectric material and the second dielectric material can be RIE etched with sulfur hexafluoride (SF_6) for approximately four minutes. If sulfur hexafluoride is used as the etchant, the etching can be performed in a plasma chamber with a 1:2 ratio of sulfur hexafluoride to oxygen (O_2).

[00182] The etch rate of the sulfur hexafluoride for the first dielectric material and the second dielectric material are approximately the same (i.e., approximately 0.5 μm per minute). The etch rate of the second dielectric material, however, is marginally greater than the first dielectric material. In some example, the pressure in the plasma chamber during etching is approximately 50 mTorr to approximately 400 mTorr. The RIE etch can be performed in a Tegal 901, manufactured by Tegal Corporation of Petaluma, California.

[00183] The second dielectric material can be etched before the first dielectric material; the first dielectric material can be etched before the base dielectric material. In many examples, the metal layer underneath the base dielectric material functions as an etch stop for the etching process. If sulfur hexafluoride is used as the etchant, the metal layer can be aluminum. In this embodiment, the metal layer cannot be molybdenum or tantalum because sulfur hexafluoride etches these two metals. In a different embodiment, the metal layer can include molybdenum and/or tantalum if the etch for the overlying second dielectric layer is a timed etch.

[00184] A buffered oxide etch (BOE) and chlorine based etchants cannot be used in some examples because they do not etch the first dielectric material when it comprises an organosiloxane dielectric material. FIG. 24 illustrates a cross-sectional view of the device build

area of an example of semiconductor device 1350 after etching etch base dielectric material 2499, first dielectric material 2461 and second dielectric material 2462. After process 1119 in FIG. 11, semiconductor device 1350 can include vias 2463, as shown in FIG. 24. Vias 2463 are associated with via area 2982 of FIG. 29. The mask over second dielectric layer 2462 is not shown in FIG. 24

[00185] Referring again to FIG. 11, the next process in procedure 120 is a process 1120 of removing the mask. In some examples, the mask is removed by ashing the mask (e.g., the photoresist) at a temperature below 110°C. If the mask is ashed at a temperature above 110°C, cracking can occur in the first dielectric material. Accordingly, in some examples, ashing of the mask is performed at a temperature in the range of approximately 70°C to approximately 90°C. In the same or different example, the ashing of the mask is performed at a temperature in the range of approximately 77°C to approximately 84°C.

[00186] The ashing can be performed at a pressure of no greater than approximately 300 mTorr. Oxygen (O_2) can flow through in the chamber during the ashing process at a rate of approximately 50 sccm. In various examples, the ashing procedure can be performed in a Tegal 901. After ashing the mask, the semiconductor device can be rinsed with deionized water and spin dried. In some examples, the rinsing can be performed in a quick dump rinser, and the drying can be performed in a spin rinse dryer.

[00187] In other examples, a wet strip can be used to remove the photoresist. In some embodiments, an N-methyl pyrolidinone (NMP) based stripper can be used.

[00188] The next process in procedure 120 of FIG. 21 is a process 1121 of providing one or more second semiconductor elements. Examples of one or more second semiconductor elements can include a second metal layer, an indium tin oxide (ITO) layer, and a silicon nitride layer.

[00189] As an example, FIG. 25 illustrates a cross-sectional view of the device build area of an example of semiconductor device 1350 after providing a second metal layer 2564 and an ITO layer 2565. Second metal layer 2564 can be deposited over second dielectric material 2462 and at least partially in vias 2463 (FIG. 24). Second metal layer 2564 can comprise molybdenum and can be approximately 0.15 μm thick. In some examples, second metal layer 2564 can be deposited by sputtering using a KDF 744.

[00190] ITO layer 2565 can be deposited over second metal layer 2564. ITO layer 2565 can comprise indium tin oxide and can be approximately 0.05 μm thick. In some examples, ITO layer can be deposited by sputtering using a KDF 744.

[00191] In some examples, second metal layer 2564 is pattern etched. Then ITO layer 2565 can be deposited onto second metal layer 2564 and then pattern etched. As an example, second metal layer 2564 and ITO layer 2565 can be etched using an AMAT 8330.

[00192] FIG. 26 illustrates a cross-sectional view of the device build area of an example of semiconductor device 350 after providing a silicon nitride layer 2666. Silicon nitride layer 2666 can be deposited over ITO layer 2565 and can be approximately 0.10 μm thick. In some examples, silicon nitride layer 2666 can be deposited via PECVD using an AMAT P5000. In the same or other examples, silicon nitride layer 2666 can be etched using a Tegal 901, with ITO layer 2565 being the stop layer.

[00193] After process 1121, procedure 120 is complete. With reference to FIG. 1, the next procedure of method 100 is a procedure 130 of removing the flexible substrate, including the semiconductor elements coupled to the flexible substrate, from the carrier substrate. In some examples, the flexible substrate can be removed from the carrier substrate by peeling the flexible substrate from the carrier substrate by hand.

[00194] Turning to another embodiment, FIG. 27 illustrates an example of a method 2700 of planarizing a flexible substrate. In the same or different embodiments, method 2700 can be considered a method of etching an organosiloxane dielectric material. Method 2700 can also be considered a method of etching an organic siloxane-based dielectric or a method of etching a siloxane-based dielectric material. Method 2700 is merely exemplary and is not limited to the embodiments presented herein. Method 2700 can be employed in many different embodiments or examples not specifically depicted or described herein.

[00195] Referring to FIG. 27, method 2700 includes a procedure 2711 of providing a substrate. Procedure 2711 can be similar or identical to process 211 of FIG. 2. The substrate can be similar or identical to substrate 450 of FIG. 4. In yet other embodiments, Procedure 2711 can be similar or identical to method 110 of FIG. 1, and the substrate can be similar or identical to substrate 450, which can be a portion of flexible substrate assembly 540.

[00196] Method 2700 can continue with a procedure 2712 of providing a first dielectric material. In some examples, the first dielectric material can be similar or identical to second dielectric material 2462 of FIG. 24 and process 1117 of FIG. 11. For example, second dielectric material 2462 can comprise a silicon nitride layer with a thickness of approximately 0.1 μm to approximately 0.2 μm.

[00197] The next procedure in method 2700 is a procedure 2713 of providing a second dielectric material. The second dielectric material can be similar or identical to the first

dielectric material 2461 of FIG. 24. Procedure 2713 can be similar or identical to process 1114 of FIG. 1.

[00198] Method 2700 continues with a procedure 2714 of baking the second dielectric material. In some examples, procedure 2714 can be similar or identical to process 1115 of FIG. 11.

[00199] Subsequently, method 2700 includes a procedure 2715 of curing the second dielectric material. In some examples, procedure 2715 can be similar or identical to process 1116 of FIG. 11.

[00200] In other examples, a different baking procedure with five separate bakes in a convection oven can be used. The first bake can be a bake at approximately 40°C for approximately ten minutes. The ramp-up time from room temperature to approximately 40°C is approximately two minutes. After baking at 40°C, the temperature is ramped-up over approximately thirty-two minutes to approximately 160°C. Then, the flexible substrate is baked for approximately thirty-five minutes at approximately 160°C.

[00201] The temperature of the convection oven is then increased to approximately 180°C over approximately ten minutes after the 160°C bake. The flexible substrate is baked for approximately twenty minutes at approximately 180°C.

[00202] After baking at 180°C, the temperature is ramped-up over approximately fifty minutes to approximately 230°C. Alternatively, the temperature is ramped-up at approximately 2°C per minute to approximately 230°C. The flexible substrate is baked for approximately fifteen hours at approximately 230°C.

[00203] Finally, in this bake procedure, the temperature in the oven is ramped-down to approximately 60°C over approximately eighty-five minutes. The flexible substrate is baked for approximately ten minutes at approximately 60°C. After baking is complete, the flexible substrate is allowed to cool to approximately room temperature before proceeding with method 2700 of FIG. 27.

[00204] Method 2700 continues with a procedure 2716 of providing a third dielectric material. In some examples, the third dielectric material can be deposited with a thickness of approximately 0.2 μm to approximately 0.4 μm. In some examples, the third dielectric material can be an approximately 0.3 μm thick layer of silicon nitride. After depositing the third dielectric material, the flexible substrate can be in-situ baked for approximately five minutes at approximately 180°C. In some examples, the third dielectric material can be similar or identical to nitride passivation layer 1352 of FIG. 13.

[00205] FIG. 28 illustrates an example of a semiconductor device 2850 after providing the third dielectric material, according to the second embodiment. In these examples, first dielectric material 2871 is provided over flexible substrate assembly 540. Second dielectric material 2872 is provided over first dielectric material 2871, and third dielectric material 2873 is provided over second dielectric material 2872.

[00206] After providing the third dielectric layer, method 2700 is complete. The resulting semiconductor device (2850 of FIG. 28) can be used as the flexible substrate provided in procedure 110 of method 100.

[00207] Returning to the drawings, FIG. 31 illustrates an example of method 3100 of manufacturing a semiconductor device, according to an embodiment. Method 3100 is merely exemplary and is not limited to the embodiments presented herein. Method 3100 can be employed in many different embodiments or examples not specifically depicted or described herein. Method 3100 can be similar to method 120 (FIG. 2). In some embodiments, the procedures, the processes, and/or the activities of method 3100 can be performed in the order presented. In other embodiments, the procedures, the processes, and/or the activities of the method 3100 can be performed in any other suitable order. In still other embodiments, one or more of the procedures, the processes, and/or the activities in method 3100 can be combined or skipped.

[00208] Referring now to FIG. 31, method 3100 comprises procedure 3101 of providing a substrate. In some embodiments, procedure 3101 can be similar or identical to process 211 (FIG. 2) and/or method 110 (FIG. 2). The substrate can be similar or identical to substrate 3208 as illustrated in FIGs. 32 and 33.

[00209] Referring now back to FIG. 31, method 3100 can comprise procedure 3102 of providing a barrier layer over and/or on the substrate. In some embodiments, procedure 3103 comprises providing the gate metal layer on the barrier layer. In many embodiments, procedure 3102 occurs before procedures 3103, as described below, and/or after procedure 3101. The barrier layer can be similar or identical to barrier layer 3209 as illustrated in FIGs. 32 and 33 and described below.

[00210] Referring now back to FIG. 31, method 3100 comprises procedure 3103 of providing a gate metal layer over the substrate. In many embodiments, procedure 3103 occurs before procedures 3104 and/or 3105, as described below, and/or after procedure 3102. In some embodiments, procedure 3103 can be similar or identical to activity 1211 (FIG. 12). In various embodiments, the gate metal layer can be similar or identical to gate metal layer 3202 as

illustrated in FIGs. 32 and 33 and described below. FIG. 49 is a flowchart illustrating procedure 3103 of providing a gate metal layer over the substrate, according to an embodiment.

[00211] In various embodiments, procedure 3103 can comprise process 4901 of depositing the gate metal layer over and/or on the substrate. Procedure 3103 can comprise process 4902 of depositing and developing a first photoresist layer over the gate metal layer. Procedure 3103 can comprise process 4903 of etching the gate metal layer with a first etchant while using the first photoresist layer as a first etch mask.

[00212] FIG. 32 illustrates a cross-sectional view of a device build area of an example of a semiconductor device 3200 after conducting procedure 3103, according to an embodiment. As can be seen in FIG. 46, the cross-sectional view of the device build area is a cross-sectional view of a portion of semiconductor device 3200 taken at the "a" lines. The device build cross-sectional view comprises device build contact areas 4680 and via area 4682. In addition, FIG. 33 illustrates a cross-sectional view of a gate contact building area of an example of semiconductor device 3200 after conducting procedure 3103, according to an embodiment. As can be seen in FIG. 46, the cross-sectional view of the gate contact build area is the cross-sectional view of a portion of semiconductor device 3200 taken at the "b" lines. The gate contact build cross-sectional view comprises a cross-sectional view of gate contact area 4681. FIG. 46 is merely exemplary and is not limited to the embodiments presented herein.

[00213] In many embodiments, an electronic device (not shown) includes one or more of semiconductor device 3200, among other components. In many embodiments, semiconductor device 3200 comprises a transistor or a thin film transistor. In the same or different embodiments, the electronic device can comprise a display, and the display comprises the semiconductor device(s)/transistor(s). In the same or different embodiments, the display can comprise any of a liquid crystal display, an electrophoretic display, or an organic light emitting diode (OLED) display.

[00214] In various examples, semiconductor device 3200 can comprise an effective saturation mobility of 18.6 cm2/V-s and a threshold voltage shift of 2.2 volts or less under positive and negative gate bias direct current (DC) stress for 10,000 seconds. In other examples, semiconductor device 3200 can be processed at temperatures at or below approximately 200 degrees Celsius.

[00215] Referring to FIGs. 32 and 33, for example, gate metal layer 3202 can be over substrate 3208 and/or barrier layer 3209. In the same or different embodiments, gate metal layer 3202 can be on barrier layer 3209.

[00216] In various embodiments, substrate 3208 can comprise a rigid substrate and/or a flexible substrate. In some embodiments, substrate 3208 can be similar or identical to substrate 450 (FIG. 4), a portion of flexible substrate assembly 540 (FIGs. 5, 6, 8, 9, or 10), or carrier substrate 651 (FIG. 6).

[00217] In many embodiments, barrier layer 3209 can comprise a first dielectric material. The first dielectric material can comprise silicon dioxide and/or silicon nitride. In the same or different embodiments, barrier layer 3209 can be similar or identical to passivation layer 1352 (FIG. 13). In the same or different embodiments, barrier layer 3209 can be greater than or equal to approximately 200 nanometers thick and less than or equal to approximately 400 nanometers thick. In further embodiments, barrier layer 3209 can be approximately 300 nanometers thick.

[00218] In many embodiments, gate metal layer 3202 can comprise one or more of molybdenum, aluminum, tantalum, chromium, or tungsten. In the same or different embodiments, gate metal layer 3202 can be similar or identical to patterned metal gate 1353 (FIG. 13). In the same or different embodiments, gate metal layer 3202 can be greater than or equal to approximately 100 nanometers thick and less than or equal to approximately 200 nanometers thick. In further embodiments, gate metal layer 3202 can be approximately 150 nanometers thick.

[00219] Referring now back to FIG. 31, method 3100 can comprise procedure 3104 of providing a gate barrier layer over and/or on the gate metal layer. In many embodiments, procedure 3104 occurs before procedure 3105, as described below, and/or after procedure 3103. The gate barrier layer can be similar or identical to gate barrier layer 3510 as illustrated in FIGs. 35 and 36 and described below.

[00220] Referring now back to FIG. 31, method 3100 comprises procedure 3105 of providing a transistor active layer over the gate metal layer. In many embodiments, procedure 3105 occurs before procedure 3106, as described below, and/or after procedure 3104. FIG. 34 is a flow chart illustrating procedure 3105 of providing the transistor active layer over the gate metal layer, according to an embodiment. The transistor active layer can be similar or identical to transistor active layer 3505 as illustrated in FIGs. 35 and 36 and described below, which can comprise first active layer 4706 and second active layer 4707 as illustrated in FIG. 47 and described below. In many embodiments, an etch stop layer similar or identical to etch stop layer 3511 (not shown) can be over and/or on the transistor active layer as illustrated in FIG. 35 and described below.

[00221] Procedure 3105 of FIG. 34 comprises process 3401 of providing a first active layer over and/or on the gate metal layer. In many embodiments, the first active layer can be similar to first active layer 4706, as described below.

[00222] In some embodiments, process 3401 can comprise (a) positioning the substrate inside of a vacuum chamber and (b) sputtering inside of the vacuum chamber a target material comprising at least one of indium oxide, zinc oxide, gallium oxide, tin oxide, hafnium oxide, or aluminum oxide with a first feed gas comprising argon. In some embodiments, the first feed gas can comprise nitrogen in addition to or instead of argon.

[00223] Procedure 3105 of FIG. 34 comprises process 3402 of providing a second active layer over and/or on the first active layer. In the same or different embodiments, the second active layer can be similar to second active layer 4707, as described below. In respect to procedure 3105, where the transistor active layer comprises only the first active layer, the semiconductor device may not turn off.

[00224] In some embodiments, process 3402 can comprise (a) combining oxygen with the first feed gas to a form a second feed gas comprising argon and two percent oxygen by volume and (b) sputtering inside of the vacuum chamber the target material with the second feed gas inside of the vacuum chamber. In various embodiments, process 3402 can occur directly after process 3401. For example, process 3402 can be conducted such that oxygen provided in process 3402 is simply added to the first feed gas such that process 3401 transitions directly into process 3402.

[00225] In many embodiments, process 3401 and/or process 3402 can occur at a pressure of greater than or equal to approximately 10 milliTorr and less than or equal to approximately 20 milliTorr. In the same or different embodiments, process 3401 and/or process 3402 can occur at a pressure of approximately 16 milliTorr. In the same or different embodiments, process 3401 and/or process 3402 can occur at a temperature of greater than or equal to approximately 25 degrees Celsius and less than or equal to approximately 39 degrees Celsius.

[00226] Procedure 3105 of FIG. 34 can comprise process 3403 of depositing and developing a second photoresist layer over the second active layer and/or the first active layer. In some embodiments, the second photoresist layer can be similar or identical to the first photoresist layer, as described above with respect to process 4902. In many embodiments, process 3403 can comprise depositing and developing a second photoresist layer over an etch stop layer, the second active layer and/or the first active layer. In many embodiments, the etch stop layer similar or identical to etch stop layer 3511 (FIG. 35).

[00227] Procedure 3105 of FIG. 34 can comprise process 3404 of etching the second active layer and the first active layer with a second etchant while using the second photoresist layer as a second etch mask. In many embodiments, process 3404 can comprise etching the etch stop layer, the second active layer, and the first active layer with the second etchant while using the

second photoresist layer as the second etch mask. In many embodiments, process 3404 can be performed using an AMAT 8330. In some embodiments, the second etchant can comprise a dry etchant. In the same or different embodiments, the dry etchant can comprise oxygen, hydrogen chloride, and methane. In the same or different embodiments, the oxygen, hydrogen chloride, and methane can comprise ten, one hundred, and twenty parts per volume. In many embodiments, performing process 3404 can be similar or identical to etching ITO layer 2565 (FIG. 25, as described above.

[00228] In some embodiments, process 3403 and process 3404 can be conducted after process 3401 and can be repeated after process 3402. In the same or different embodiments, the second photoresist and/or the second etchant can be the same for both instances in which process 3403 and process 3404 are conducted, respectively, or one or both can be different. In other embodiments, process 3403 and process 3404 can be conducted only after completing both process 3401 and process 3402.

[00229] FIG. 47 illustrates an example of semiconductor device 3200 after conducting processes 3401 and 3402. Referring to FIG. 47, for example, first active layer 4706 can be over gate metal layer 3202 and/or second active layer 4707 can be over first active layer 4706. In various embodiments, first active layer 4706 comprises at least one first metal oxide and comprises a first conductivity. In the same or different embodiments, second active layer 4707 comprises at least one second metal oxide and comprises a second conductivity. Although not shown in FIG. 47, in some embodiments, an etch stop layer similar or identical to etch stop layer 3511 can be over and/or on second active layer 4707.

[00230] In many examples, using oxides and different conductivities for first active layer 4706 and/or second active layer 4707 can improve mobility, on/off current ratio, and stability over active layers comprised of amorphous silicon. The result can be smaller semiconductor devices and increased display resolutions.

[00231] In many embodiments, the at least one first metal oxide can comprise one or more of indium oxide, zinc oxide, gallium oxide, tin oxide, hafnium oxide, or aluminum oxide, in equal or unequal proportions to one another. For example, in some embodiments, the at least one first metal oxide can comprise approximately sixty percent zinc oxide and approximately forty percent indium oxide. In other examples, the at least one first metal oxide can comprise indium oxide, gallium oxide, and zinc oxide in equal proportions to each other. In various embodiments, the at least one second metal oxide can comprise the at least one first metal oxide. In the same or different embodiments, where the at least one second metal oxide comprises the at least one first metal oxide, the at least one second metal oxide may comprise the constituent

compounds/elements of the at least one first metal oxide but comprise different proportions of the constituent compounds/elements, or the at least one second metal oxide may comprise both the constituent compounds/elements and the relative proportions of the constituent compounds/elements of the at least one first metal oxide. In other embodiments, the at least one second metal oxide can be different from the at least one first metal oxide, the at least one second metal oxide comprising at least one different constituent compound/element than the at least one first metal oxide and/or different proportions of the at least one second metal oxide relative to the proportions of the at least one first metal oxide (e.g., where the at least one first metal oxide comprises approximately sixty percent zinc oxide and approximately forty percent indium oxide and the at least one second metal oxide comprises indium oxide, gallium oxide, and zinc oxide in equal proportions to each other, or vice versa). In other examples, the differences can be far more subtle such as where both the at least one second metal oxide and the at least one first metal oxide comprise zinc oxide and indium oxide but the at least one second metal oxide has a ratio of zinc oxide to indium oxide of approximately 60:40 and the at least one first metal oxide has a ratio of zinc oxide to indium oxide of approximately 59:41.

[00232] In many embodiments, transistor active layer 3505 can be greater than or equal to approximately 40 nanometers thick and less than or equal to approximately 60 nanometers thick. In further embodiments, transistor active layer 3505 can be approximately 50 nanometers thick. In the same or different embodiments, first active layer 4706 can be greater than or equal to approximately 5 nanometers thick and less than or equal to approximately 40 nanometers thick. In further embodiments, first active layer 4706 can be greater than or equal to approximately 5 nanometers thick and less than or equal to approximately 20 nanometers thick. Accordingly, in many embodiments, where first active layer 4706 is, for example, 25 nanometers thick, second active layer 4707 can be approximately 25 nanometers thick. In further examples, where first active layer 4706 is 40 nanometers thick, second active layer 4707 can be approximately 10 nanometers thick.

[00233] In many embodiments, first active layer 4706 comprises a first conductivity. For example, the first conductivity can be approximately 0.002 Ohm-centimeters. In the same or different embodiments, second active layer 4707 comprises a second conductivity. For example, the second conductivity can be greater than or equal to approximately 10 ohm-centimeters and less than or equal to approximately 200 ohm-centimeters. In various embodiments, the first conductivity is greater than the second conductivity. In other embodiments, the first conductivity is less than the second conductivity.

[00234] Referring now back to FIG. 31, method 3100 can comprise procedure 3106 of providing an etch stop layer over the transistor active layer, the first active layer, and/or the second active layer and/or on one of the transistor active layer, the first active layer, and/or the second active layer. In many embodiments, procedure 3106 occurs before procedures 3107 and/or 3108 and/or after procedure 3105. The etch stop layer can be similar or identical to etch stop layer 3511 as illustrated in FIGs. 35 and 36. FIGs. 35 and 36 illustrate an example of semiconductor device 3200 after providing an etch stop layer over the transistor active layer.

[00235] Referring to FIGs. 35 and 36, for example, gate barrier layer 3510 can be over and/or on gate metal layer 3202 and/or barrier layer 3209, under transistor active layer 3505, and/or between gate metal layer 3202 and transistor active layer 3505. In various embodiments, gate barrier layer 3510 can be similar or identical to gate dielectric layer 1554 (FIG. 15). In many embodiments, gate barrier layer 3510 can comprise a second dielectric material. The second dielectric material can comprise silicon dioxide. Gate barrier layer 3510 can be buffered with silicon nitride or other dielectrics on the side closest to gate metal layer 3502. In the same or different embodiments, gate barrier layer 3510 can be greater than or equal to approximately 100 nanometers thick and less than or equal to approximately 300 nanometers thick.

[00236] Referring again to FIGs. 35 and 36, in some embodiments, transistor active layer 3505 can be over gate metal layer 3202 and/or can be over and/or on gate barrier layer 3510. Transistor active layer 3505 can comprise first active layer 4706 (FIG. 47) and second active layer 4707 (FIG. 47), as described above.

[00237] Referring again to FIGs. 35 and 36, in some embodiments, etch stop layer 3511 can be over transistor active layer 3505. In the same or different embodiments, etch stop layer 3511 can be over and/or on at least a portion of transistor active layer 3505 and/or gate barrier layer 3510, under source/drain contact layer 4150 (FIGs. 41 and 42), and/or between the portion of transistor active layer 3505 and source/drain contact layer 4150. In various embodiments, etch stop layer 3511 can be similar or identical to IMD layer 1556 (FIG. 15). In many embodiments, etch stop layer 3511 can comprise a third dielectric material. The third dielectric material can comprise silicon dioxide. Etch stop layer 3511 can be buffered with silicon nitride on the side closest to source/drain contact layer 4150. In the same or different embodiments, etch stop layer 3511 can be greater than or equal to approximately 50 nanometers thick and less than or equal to approximately 200 nanometers thick. In further embodiments, etch stop layer 3511 can be approximately 100 nanometers thick.

[00238] Referring now back to FIG. 31, method 3100 can comprise procedure 3107 of providing a mesa passivation layer over and/or on the etch stop layer. In many embodiments,

procedure 3107 can be similar or identical to activity 1213 (FIG. 12). In many embodiments, procedure 3107 occurs before procedure 3108 and/or after procedure 3106. The mesa passivation layer can be similar or identical to mesa passivation layer 3712 as illustrated in FIGs. 37 and 38. FIGs. 37 and 38 illustrate an example of semiconductor device 3200 after providing a mesa passivation layer over and/or on the etch stop layer.

[00239] Referring to FIGs. 37 and 38, for example, mesa passivation layer 3712 can be over and/or on etch stop layer 3511, under source/drain contact layer 4150 (FIGs. 41 and 42), and/or between etch stop layer 3511 and source/drain contact layer 4150. In various embodiments, mesa passivation layer 3712 can be similar or identical to mesa passivation layer 1757 (FIG. 17). In many embodiments, mesa passivation layer 3712 can comprise a fourth dielectric material. The fourth dielectric material can comprise silicon dioxide. In the same or different embodiments, mesa passivation layer 3712 can be greater than or equal to approximately 50 nanometers thick and less than or equal to approximately 200 nanometers thick. In further embodiments, mesa passivation layer 3712 can be approximately 100 nanometers thick. Mesa passivation layer 3712 can protect the side walls of transistor active layer 3505 during etching processes.

[00240] In many embodiments, method 3100 can comprise procedure 3108 of conducting one or more post-mesa passivation layer etches, similar or identical to activity 1214 (FIG. 12), as described above. FIGs. 39 and 40 illustrate cross-sectional views of semiconductor device 3200 after the one or more port-mesa passivation layer etches have been conducted. For example, FIG. 40 illustrates semiconductor device 3200 after a contact gate etch has taken place in the gate contact build region of semiconductor device 3200. In the same or different examples, FIG. 39 illustrates semiconductor device 3200 after a device build contact area etch has taken place in the device build region of semiconductor device 3200. After procedure 3109, gate contact 4091 can be formed on semiconductor 3200. Gate contact 4091 is associated with gate contact area 4681 of FIG. 46. After procedure 3109, device build contacts 3990 are formed on semiconductor 3200. Device build contacts 3990 are associated with device build contact areas 4680 of FIG. 46.

[00241] Referring now back to FIG. 31, method 3100 comprises procedure 3109 of providing a source/drain contact layer over the transistor active layer, the first active layer, and/or the second active layer. In the same or different embodiments, procedure 3109 can comprise providing the source/drain contact layer on part of the transistor active layer and/or on the mesa passivation layer. In some embodiments, procedure 3109 can be similar or identical to process 1113 (FIG. 11), and source/drain contact layer can be similar or identical to source/drain contact

layer 4150 (FIG. 41). FIG. 48 is a flow chart illustrating procedure 3109 of providing a source/drain contact layer over the transistor active layer, the first active layer, and/or the second active layer, according to an embodiment.

[00242] Referring to FIG. 48, in some embodiments, procedure 3109 can comprise depositing one or more metal layers over the transistor active layer, the first active layer, and/or the second active layer. In the same or different embodiments, procedure 3109 can comprise process 4801 of depositing a first metal layer over the transistor active layer, the first active layer, and/or the second active layer. In some embodiments process 4801 can comprise depositing a first metal layer over the transistor active layer, the first active layer, and/or the second active layer to form the source/drain contact layer. In further embodiments, procedure 3109 can comprise process 4802 of depositing a second metal layer over the first metal layer to form the source/drain contact layer from the first metal layer and the second metal layer. In some embodiments, the first metal layer comprises molybdenum and the second metal layer comprises aluminum. In some embodiments, procedure 3109 can comprise process 4803 of depositing and developing a third photoresist layer over the source/drain contact layer. In further embodiments, procedure 3109 can comprise process 4804 of etching the source/drain contact layer with a third etchant while using the third photoresist layer as a third etch mask. In some embodiments, process 4802 can be omitted. In many embodiments, the third etchant can be a dry etchant. In the same or different embodiments, the dry etchant can comprise chlorine and boron tricholoride and/or chlorine and oxygen. In the same or different embodiments, the chlorine and boron trichloride can be used to etch the first metal layer (e.g., aluminum) and the chlorine and oxygen cab be used to etch the second metal layer.

[00243] FIG. 41 illustrates a cross-sectional view of a device build region of an example of semiconductor device 3200 after procedure 3109 has been completed. In addition, FIG. 42 illustrates a cross-sectional view of a gate contact build region of an example of semiconductor device 3200 after procedure 3109 has been completed.

[00244] Referring to FIGs. 41 and 42, for example, source/drain contact layer 4150 can be over transistor active layer 3505. In the same or different embodiments, source/drain contact layer 4150 can be on transistor active layer 3505. Referring back to FIG. 31, in various embodiments, source/drain contact layer 4150 can comprise first source/drain contact 4104 and/or second source/drain contact 4105. In some embodiments, first source/drain contact 4104 can comprise a transistor drain contact and second source/drain contact 4105 can comprise a transistor source contact, or vice versa. In the same or different embodiments, source/drain contact layer 4150 can be over and/or on one or both of mesa passivation layer 3712 and

transistor active layer 3505. In various embodiments, source/drain contact layer 4150 can comprise at least one of molybdenum or aluminum. In the same or different embodiments, source/drain contact layer 4150 can be greater than or equal to approximately 100 nanometers thick and less than or equal to approximately 200 nanometers thick. In further embodiments, source/drain contact layer 4150 can be approximately 150 nanometers thick.

[00245] Referring now back to FIG. 31, method 3100 can comprise procedure 3110 of providing a base dielectric material, similar or identical to process 1198 (FIG. 11). In the same or different embodiments, method 3100 can comprise procedure 3111 of providing a fifth dielectric material, similar or identical to process 1114 (FIG. 11). In the same or different embodiments, method 3100 can comprise a procedure of baking the semiconductor device, similar or identical to process 1115 (FIG. 11). In the same or different embodiments, method 3100 can comprise procedure 3112 of curing the fifth dielectric material, similar or identical to process 1116 (FIG. 11). In the same or different embodiments, method 3100 can comprise procedure 3113 of providing a sixth dielectric material, similar or identical to process 1117 (FIG. 11). In the same or different embodiments, method 3100 can comprise procedure 3114 of providing a mask over the sixth dielectric material, similar or identical to process 1118 (FIG. 11). In the same or different embodiments, method 3100 can comprise procedure 3115 of etching the base dielectric material, the fifth dielectric material, and the sixth dielectric material, similar or identical to process 1119 (FIG. 11). In the same or different embodiments, method 3100 can comprise procedure 3116 of removing the mask, similar or identical to process 1120 (FIG. 11). In the same or different embodiments, method 3100 can comprise a procedure 3117 of providing one or more semiconductor elements, similar or identical to process 1121 (FIG. 11). In various embodiments, one or more of procedures 3110-3117 can be omitted.

[00246] FIG. 43 illustrates a cross-sectional view of the device build area of an example of semiconductor device 3200 after conducting procedures 3101-3116. With reference to FIG. 43, dielectric material 4399, fifth dielectric material 4361 and sixth dielectric material 4362 are deposited over source/drain contact layer 4150. Dielectric material 4399, fifth dielectric material 4361, and/or sixth dielectric material 4362 can be similar to dielectric material 2499 (FIG. 24), first dielectric material 2461 (FIG. 24), and/or second dielectric material 2462 (FIG. 24), respectively. After procedure 3114 (FIG. 31), semiconductor device 3200 can comprise vias 4363, which can be similar or identical to vias 2463 (FIG. 24), as shown in FIG. 43. Vias 4363 are associated with via areas 4682 of FIG. 46. The mask over sixth dielectric layer 4362 is not shown in FIG. 43.

[00247] In one embodiment, FIG. 44 illustrates a cross-sectional view of the device build area of an example of semiconductor device 3200 after conducting procedure 3117. With reference to FIG. 44, third metal layer 4464 and ITO layer 4465 can be provided over sixth dielectric material 4362. In the same or different embodiments, third metal layer 4464 can be provided over sixth dielectric material 4362 and at least partially in vias 4363 (FIG. 43). In many embodiments, third metal layer 4464 and ITO layer 4465 can be similar to second metal layer 2564 (FIG. 25) and ITO layer 2565 (FIG. 25), respectively.

[00248] In another embodiment different from the embodiment illustrated in FIG. 44, FIG. 45 illustrates a cross-sectional view of the device build area of another example of semiconductor device 3200 after conducting procedure 3117. With reference to FIG. 45, silicon nitride layer 4566 can be provided over ITO layer 4465.

[00249] Although the invention has been described with reference to specific embodiments, it will be understood by those skilled in the art that various changes can be made without departing from the spirit or scope of the invention. Accordingly, the disclosure of embodiments is intended to be illustrative of the scope of the invention and is not intended to be limiting. It is intended that the scope of the invention shall be limited only to the extent required by the appended claims. To one of ordinary skill in the art, it will be readily apparent that the semiconductor device and its methods of providing the semiconductor device discussed herein may be implemented in a variety of embodiments, and that the foregoing discussion of certain of these embodiments does not necessarily represent a complete description of all possible embodiments. Rather, the detailed description of the drawings, and the drawings themselves, disclose at least one preferred embodiment, and may disclose alternative embodiments. For example, except for their respective active layers, semiconductor devices 1350 (FIGs. 13-22, 24-26, and 29) and 3200 (FIGs. 32-33 and 35-47) can be similar or identical to each other, and methods 120 (FIG. 11) and 3100 (FIG. 31) can be similar or identical to each other.

[00250] All elements claimed in any particular claim are essential to the embodiment claimed in that particular claim. Consequently, replacement of one or more claimed elements constitutes reconstruction and not repair. Additionally, benefits, other advantages, and solutions to problems have been described with regard to specific embodiments. The benefits, advantages, solutions to problems, and any element or elements that may cause any benefit, advantage, or solution to occur or become more pronounced, however, are not to be construed as critical, required, or essential features or elements of any or all of the claims, unless such benefits, advantages, solutions, or elements are expressly stated in such claim.

[00251] Moreover, embodiments and limitations disclosed herein are not dedicated to the public under the doctrine of dedication if the embodiments and/or limitations: (1) are not expressly claimed in the claims; and (2) are or are potentially equivalents of express elements and/or limitations in the claims under the doctrine of equivalents.

CLAIMS

What is claimed is:

1) An electronic device comprising:
a transistor comprising:
a gate metal layer;
a transistor active layer over the gate metal layer; and
a source/drain contact layer over the transistor active layer, the source/drain contact layer comprising a first source/drain contact and a second source/drain contact;
wherein:
the transistor active layer comprises:
a first active layer over the gate metal layer, the first active layer comprising at least one first metal oxide; and
a second active layer over the first active layer, the second active layer comprising at least one second metal oxide;
the first active layer comprises a first conductivity;
the second active layer comprises a second conductivity; and
the first conductivity is greater than the second conductivity.

2) The electronic device of claim 1 further comprising:
a substrate;
wherein:
the gate metal layer is over the substrate;
the substrate comprises one of a rigid substrate or a flexible substrate;
when the substrate comprises the rigid substrate, the rigid substrate comprises silicon; and
when the substrate comprises the flexible substrate, the flexible substrate comprises one of plastic or stainless steel, the plastic comprising polyethylene napthalate.

3) The electronic device of claim 1 or 2 wherein:
the transistor active layer is on the gate metal layer;
the first source/drain contact is on the transistor active layer; and

the second source/drain contact is on the transistor active layer.

4) The electronic device of any one of claims 1-3 further comprising:
one of a liquid crystal display, an electrophoretic display, or an organic light emitting diode display comprising the transistor.

5) The electronic device of any one of claims 1-4 wherein:
the at least one first metal oxide comprises at least one of indium oxide, zinc oxide, gallium oxide, tin oxide, hafnium oxide, or aluminum oxide.

6) The electronic device of any one of claims 1-5 wherein:
the at least one first metal oxide comprises approximately sixty percent zinc oxide and approximately forty percent indium oxide.

7) The electronic device of any one of claims 1-6 wherein:
the at least one first metal oxide comprises indium oxide, gallium oxide, and zinc oxide in equal proportions to each other.

8) The electronic device of any one of claims 1-7 wherein:
the at least one second metal oxide comprises the at least one first metal oxide.

9) The electronic device of any one of claims 1-8 wherein:
the first active layer is greater than or equal to approximately 5 nanometers thick and less than or equal to approximately 40 nanometers thick.

10) The electronic device of any one of claims 1-9 wherein:
the transistor active layer is greater than or equal to approximately 40 nanometers thick and less than or equal to approximately 60 nanometers thick.

11) The electronic device of any one of claims 1-10 wherein:
the gate metal layer comprises at least one of molybdenum, aluminum, tantalum, chromium, or tungsten.

12) The electronic device of any one of claims 1-11 wherein:

the source/drain contact layer comprises at least one of molybdenum or aluminum; and

the source/drain contact layer is greater than or equal to approximately 100 nanometers thick and less than or equal to approximately 200 nanometers thick.

13) The electronic device of any one of claims 1-12 further comprising:

a barrier layer;

wherein:

the gate metal layer is over the barrier layer;

the barrier layer comprises a first dielectric material;

the first dielectric material comprises at least one of silicon dioxide or silicon nitride; and

the barrier layer is greater than or equal to approximately 200 nanometers thick and less than or equal to approximately 400 nanometers thick.

14) The electronic device of any one of claims 1-13 further comprising:

a gate barrier layer between the gate metal layer and the transistor active layer;

wherein:

the gate barrier layer comprises a second dielectric material;

the second dielectric material comprises silicon dioxide; and

the gate barrier layer is greater than or equal to approximately 100 nanometers thick and less than or equal to approximately 300 nanometers thick.

15) The electronic device of any one of claims 1-14 further comprising:

an etch stop layer over the transistor active layer;

wherein:

the etch stop layer is between a portion of (a) the transistor active layer and (b) the source contact and the drain contact;

the etch stop layer comprises a third dielectric material;

the third dielectric material comprises silicon dioxide; and

the etch stop layer is greater than or equal to approximately 50 nanometers thick and less than or equal to approximately 200 nanometers thick.

16) The electronic device of claim 15 further comprising:

a mesa passivation layer over the etch stop layer;

wherein:

the mesa passivation layer is between (a) the etch stop layer and (b) the source/drain contact layer;

the mesa passivation layer comprises a fourth dielectric material;

the fourth dielectric material comprises silicon dioxide; and

the mesa passivation layer is greater than or equal to approximately 50 nanometers thick and less than or equal to approximately 200 nanometers thick.

17) A semiconductor device comprising:

a substrate;

a barrier layer on the substrate;

a gate metal layer on the barrier layer;

a gate barrier layer on the gate metal layer;

a transistor active layer on the gate barrier layer;

an etch stop layer on the transistor active layer;

a mesa passivation layer on the etch stop layer; and

a source/drain contact layer on the mesa passivation layer and the transistor active layer;

wherein:

the transistor active layer comprises:

a first active layer on the gate metal layer, the first active layer comprising at least one first metal oxide; and

a second active layer on the first active layer and between the first active layer and the etch stop layer, the second active layer comprising at least one second metal oxide;

the first active layer comprises a first conductivity;

the second active layer comprises a second conductivity; and

the first conductivity is greater than the second conductivity.

18) The semiconductor device of claim 17 wherein:

the at least one first metal oxide comprises at least one of indium oxide, zinc oxide, gallium oxide, tin oxide, hafnium oxide, or aluminum oxide.

19) The semiconductor device of claim 17 or 18 wherein:

the at least one second metal oxide comprises the at least one first metal oxide.

20) The semiconductor device of any one of claims 17-19 wherein:
the first active layer is greater than or equal to approximately 5 nanometers thick and less than or equal to approximately 40 nanometers thick.

21) The semiconductor device of any one of claims 17-20 wherein:
the transistor active layer is greater than or equal to approximately 40 nanometers thick and less than or equal to approximately 60 nanometers thick.

22) A method of manufacturing a semiconductor device, the method comprising:
providing a substrate;
providing a gate metal layer over the substrate;
providing a first active layer over the gate metal layer, the first active layer comprising at least one first metal oxide and a first conductivity;
providing a second active layer over the first active layer, the second active layer comprising at least one second metal oxide and a second conductivity less than the first conductivity; and
providing a source/drain contact layer over the second active layer.

23) The method of claim 22 wherein:
the substrate comprises one of a rigid substrate or a flexible substrate;
when the substrate comprises the rigid substrate, the rigid substrate comprises silicon; and
when the substrate comprises the flexible substrate, the flexible substrate comprises one or plastic or stainless steel, the plastic comprising polyethylene napthalate.

24) The method of claim 22 or 23 wherein:
providing a gate metal layer over the substrate comprises:
depositing at least one of molybdenum, aluminum, tantalum, chromium, or tungsten over the substrate;
depositing and developing a first photoresist layer over the gate metal layer; and
etching the gate metal layer with a first etchant while using the first photoresist layer as a first etch mask..

25) The method of any one of claims 22-24 wherein:
providing the second active layer over the first active layer comprises:

depositing the at least one second metal oxide on the first active layer;

depositing and developing a second photoresist layer over the second active layer; and

etching the second active layer and the first active layer with a second etchant while using the second photoresist layer as a second etch mask.

26) The method of any one of claims 22-25 wherein:

providing a source/drain contact layer over the second active layer comprises:

depositing at least one of molybdenum or aluminum over the second active layer;

depositing and developing a third photoresist layer over the source/drain contact layer; and

etching the source/drain contact layer with a third etchant while using the third photoresist layer as a third etch mask.

27) The method of any one of claims 22-26 wherein:

providing the first active layer over the gate metal layer comprises:

positioning the substrate inside of a vacuum chamber; and

sputtering inside of the vacuum chamber a target material comprising at least one of indium oxide, zinc oxide, gallium oxide, tin oxide, hafnium oxide, or aluminum oxide with a first feed gas comprising argon.

28) The method of claim 27 wherein:

providing the second active layer over the first active layer comprises:

combining oxygen with the first feed gas to a form a second feed gas comprising argon and two percent oxygen by volume; and

sputtering inside of the vacuum chamber the target material with the second feed gas inside of the vacuum chamber.

29) The method of any one of claims 22-28 wherein:

the at least one second metal oxide comprises the at least one first metal oxide.

30) The method of any one of claims 22-29 wherein:

providing a first active layer over the gate metal layer and providing a second active layer over the first active layer occur at a pressure of greater than or equal to approximately 10 milliTorr and less than or equal to approximately 20 milliTorr and at a temperature of

greater than or equal to approximately 25 degrees Celsius and less than or equal to approximately 39 degrees Celsius.

31) The method of any one of claims 22-30 further comprising:

providing at least one layer of material over the substrate comprising at least one of:

providing a barrier layer over the substrate before providing the gate metal layer over the substrate, the barrier layer comprising at least one of silicon dioxide or silicon nitride;

providing a gate barrier layer over the gate metal layer before providing the first active layer over the gate metal layer, the gate barrier layer comprising silicon dioxide;

providing an etch stop layer over the second active layer before providing the source/drain contact layer over the second active layer, the etch stop layer comprising silicon dioxide; and

providing a mesa passivation layer over the etch stop layer, the mesa passivation layer comprising silicon dioxide.

32) The method of any one of claims 23-30 further comprising:

providing the at least one layer of material over the substrate comprises at least one of:

providing a barrier layer on the substrate before providing the gate metal layer over the substrate, the barrier layer comprising at least one of silicon dioxide or silicon nitride;

providing a gate barrier layer on the gate metal layer before providing the first active layer over the gate metal layer, the gate barrier layer comprising silicon dioxide;

providing an etch stop layer on the second active layer before providing the source/drain contact layer over the second active layer, the etch stop layer comprising silicon dioxide; and

providing a mesa passivation layer on the etch stop layer, the mesa passivation layer comprising silicon dioxide.

33) The method of any one of claims 22-32 wherein:

providing the gate metal layer over the substrate comprises providing the gate metal layer on the barrier layer;

providing the first active layer over the gate metal layer comprises providing the first active layer on the gate barrier layer; and

providing a second active layer over the first active layer comprises providing the second active layer on the first active layer.