

ABSTRACT

A semiconductor device includes an active pattern including a lower pattern extending in a first direction and a plurality of sheet patterns spaced apart therefrom in a second direction, a gate structure on the lower pattern and including a gate insulating layer, a gate spacer, and a gate electrode extending in a third direction, a source/drain pattern on the lower pattern and in contact with each of the sheet patterns and the gate insulating layer, and a first etch blocking pattern between the gate spacer and the source/drain pattern. The gate spacer includes an inner sidewall facing the gate electrode and extending in the third direction, and a connection sidewall extending from the inner sidewall in the first direction. The source/drain pattern includes a semiconductor filling layer on a semiconductor liner layer that is in contact with the sheet pattern and includes a facet surface extending from the connection sidewall.

FIG. 2