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(54) Title: AUTOMATED TRANSISTOR-LEVEL PLACEMENT FOR DESIGN OF INTEGRATED CIRCUITS

(57) Abstract: In some embodiments, a computer-implemented method for designing an integrated circuit using transistor placement optimization is provided. A computing system receives a specification for the integrated circuit. The specification includes a netlist describing a plurality of transistors and connections between terminals of the plurality of transistors. The computing system determines an initial location and an orientation on a canvas for each transistor in the plurality of transistors. The computing system uses an objective function based at least in part on the initial locations and the orientations of the plurality of transistors to generate a rough placement having globally optimized locations and orientations for the plurality of transistors. The computing system uses a local refinement technique to optimize the rough placement to generate a fine placement, and uses a routing technique to generate a routing for the fine placement to generate a completed design.

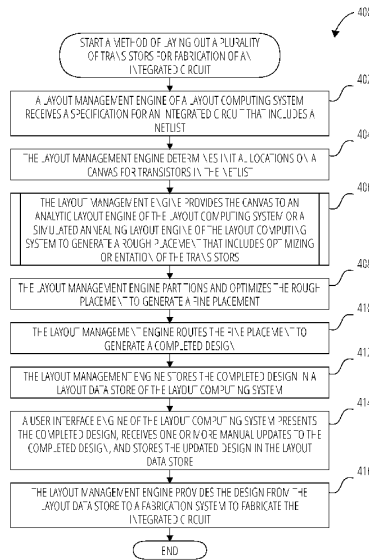


FIG. 4

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