CLAIMS

1. A method for manufacturing a semiconductor device, comprising:

providing a substrate;

forming a plurality of first structures extending in a first direction on the substrate;

forming a sacrificial layer on sidewalls of the first structures;

forming an outer spacer layer on a sidewall of the sacrificial layer;

removing part of the outer spacer layer to obtain a patterned outer spacer layer that exposes part of the sacrificial layer; and

removing the sacrificial layer to form air gaps between the patterned outer spacer layer and the first structures.

2. The method according to claim 1, wherein each of the first structures comprises a conductive structure and an isolation sidewall located on a sidewall of the conductive structure; the sacrificial layer is formed on a sidewall of the isolation sidewall away from the conductive structure.

3. The method according to claim 2, wherein the forming a sacrificial layer on sidewalls of the first structures comprises:

forming the sacrificial layer on exposed surfaces of the substrate and the first structures through a deposition process; and

etching back the sacrificial layer to form the sacrificial layer on the sidewalls of the first structures.

4. The method according to claim 3, wherein each of the first structures further comprises a hard mask structure on the conductive structure;

the etching back the sacrificial layer to form the sacrificial layer on the sidewalls of the first structures comprises:

performing a first etching on the sacrificial layer, such that a top surface of

the sacrificial layer after the first etching is flush with top surfaces of the conductive structures, or higher than the top surfaces of the conductive structures and lower than top surfaces of the hard mask structures;

forming an inner spacer layer on the top surface of the sacrificial layer after the first etching and exposed surfaces of the hard mask structures through the deposition process;

etching the inner spacer layer to remove part of the inner spacer layer on the top surface of the sacrificial layer after the first etching and the inner spacer layer on the top surfaces of the hard mask structures, so as to form the inner spacer layer on sidewalls of the hard mask structures; and

performing a second etching on the sacrificial layer using the inner spacer layer after the first etching as a mask, so as to form the sacrificial layer on the sidewalls of the first structures.

5. The method according to claim 1, wherein the removing part of the outer spacer layer to obtain a patterned outer spacer layer that exposes part of the sacrificial layer comprises:

forming a filling dielectric layer between the plurality of first structures through a deposition process;

removing the filling dielectric layer above a top surface of the outer spacer layer through a polishing process, such that a top surface of the filling dielectric layer is flush with the top surface of the outer spacer layer;

forming a mask layer and a photoresist layer on the outer spacer layer and the filling dielectric layer, exposing and developing the photoresist layer to form a patterned photoresist layer extending in a second direction, and etching the mask layer based on the patterned photoresist layer to form a patterned mask layer extending in the second direction; and

etching the outer spacer layer and the filling dielectric layer using the patterned mask layer as a mask, and removing part of the outer spacer layer and part of the filling dielectric layer to obtain the patterned outer spacer layer.

6. The method according to claim 1, wherein the sacrificial layer comprises a hydrocarbon layer, and the removing the sacrificial layer comprises:

removing the sacrificial layer through an ashing process.

7. The method according to claim 1, wherein the method further comprises:

forming a plurality of second structures extending in a second direction in the substrate, wherein each of the second structure comprises a buried word line extending in the second direction and a word line protection structure formed on the buried word line.

8. The method according to claim 2, wherein the conductive structure comprises a bit line extending in the first direction; a bit line protection structure is formed on the bit line.

9. The method according to claim 3, wherein the deposition process comprises an atomic layer deposition process.

10. The method according to claim 5, wherein after the removing the sacrificial layer to obtain air gaps, the method further comprises:

forming a plurality of storage node contact structures between the plurality of first structures, wherein the storage node contact structures are in contact with the substrate; the air gaps are located between the storage node contact structures and the first structures.

11. The method according to claim 10, wherein the forming a plurality of storage node contact structures between the plurality of first structures comprises:

removing the filling dielectric layer;

etching part of the substrate to form a plurality of recessed substrate contact holes between adjacent first structures;

forming an epitaxial layer on the substrate through an epitaxial process, wherein the epitaxial layer at least fills up the substrate contact holes; and

etching back the epitaxial layer to form the plurality of storage node contact structures, wherein top surfaces of the storage node contact structures are lower than top surfaces of the first structures.

12. The method according to claim 11, wherein before the removing the filling dielectric layer, the forming the plurality of storage node contact structures further comprises:

forming a node spacer layer in the filling dielectric layer through the deposition process, the node spacer layer covering the top surface of the filling dielectric layer; and

etching back the node spacer layer such that a top surface of the node spacer layer is flush with the top surface of the filling dielectric layer.

13. The method according to claim 11, wherein after the etching back the epitaxial layer, the method further comprises:

etching the patterned outer spacer layer to turn a top surface of the patterned outer spacer layer into an inclined surface.

14. A semiconductor device, comprising:

a substrate;

a plurality of first structures formed on the substrate and extending in a first direction, wherein each of the first structures comprises a conductive structure and an isolation sidewall located on a sidewall of the conductive structure; and

a patterned outer spacer layer formed on partial regions on two sidewalls of the first structures, wherein air gaps are formed between the patterned outer spacer layer and the first structures;

wherein, the patterned outer spacer layer comprises a plurality of outer spacer blocks; the plurality of outer spacer blocks are distributed on the substrate at

intervals in the first direction;

wherein an inner spacer layer is further provided between the patterned outer spacer layer and the first structures; the air gaps are located between the inner spacer layer and the substrate, and a bottom surface of the inner spacer layer is not lower than top surfaces of the conductive structures.

15. The semiconductor device according to claim 14, wherein the semiconductor device further comprises:

a plurality of storage node contact structures formed between the plurality of first structures, wherein the storage node contact structures are in contact with the substrate; the air gaps are located between the storage node contact structures and the first structures.

16. The semiconductor device according to claim 15, wherein a top surface of the patterned outer spacer layer is an inclined surface.

17. The semiconductor device according to claim 14, wherein the air gaps are formed between the isolation sidewalls and the patterned outer spacer layer.

18. The semiconductor device according to claim 17, wherein the conductive structure comprises a bit line extending in the first direction; a bit line protection structure is formed on the bit line.

19. The semiconductor device according to claim 14, wherein the semiconductor device further comprises:

a plurality of second structures formed in the substrate and extending in a second direction; each of the second structures comprises a buried word line extending in the second direction and a word line protection structure formed on the buried word line.