CLAIMS

1. A method comprising:

providing a first assembly comprising a first semiconductor die, a second semiconductor die located laterally adjacent to the first semiconductor die, and an alignment carrier, wherein the first semiconductor die comprises a plurality of first sacrificial bond pads located at a periphery region of the first semiconductor die, first solder balls located in a low density interconnect (LDI) region of the first semiconductor die and first bond pads located in a high density interconnect (HDI) region of the first semiconductor die, the second semiconductor die comprises a plurality of second sacrificial bond pads located at a periphery region of the second semiconductor die, second solder balls located in a LDI region of the second semiconductor die and second bond pads located in a HDI region of the second semiconductor die, and the alignment carrier comprises a substrate having a coefficient of thermal expansion that substantially matches that of an interconnect bridge, and a plurality of solder balls located on the substrate, wherein a first set of the plurality of solder balls located on the substrate are aligned to, and in contact with, the plurality of first sacrificial bond pads located at the periphery region of the first semiconductor die, and a second set of the plurality of solder balls located on the substrate are aligned to, and in contact with, the plurality of second sacrificial bond pads located at the periphery region of the second semiconductor die;

first attaching a backer structure to a backside of the first semiconductor die and the second semiconductor die;

removing the alignment carrier to provide a second assembly comprising the first semiconductor die, the second semiconductor die and the backer structure;

second attaching the interconnect bridge between the first semiconductor die and the second semiconductor die to provide a third assembly comprising the first semiconductor die, the second semiconductor die, the backer structure and the interconnect bridge, wherein the interconnect bridge connects the HDI region of the first semiconductor die to the HDI region of the second semiconductor die; and

third attaching a laminate to the third assembly.

2. The method of claim 1, further comprising removing the backer structure from the third assembly.

3. The method of claim 1, wherein the third attaching comprises a mass reflow of the first and second solder balls.

4. The method of claim 1, wherein the plurality of first sacrificial bond pads are formed at the same time as the first bond pads in the HDI region of the first semiconductor die, and the plurality of second sacrificial bond pads are formed at the same time as the second bond pads in the HDI region of the second semiconductor die.

5. The method of claim 1, further comprising removing the backer structure after the third attaching of the laminate.

6. A method comprising:

providing a first assembly comprising a first semiconductor die, a second semiconductor die located laterally adjacent to the first semiconductor die, and an alignment carrier, wherein the first semiconductor die comprises a plurality of first sacrificial bond pads located at a periphery region of the first semiconductor die, first solder balls located in a low density interconnect (LDI) region of the first semiconductor die and first bond pads located in a high density interconnect (HDI) region of the first semiconductor die, the second semiconductor die comprises a plurality of second sacrificial bond pads located at a periphery region of the second semiconductor die, second solder balls located in a LDI region of the second semiconductor die and second bond pads located in a HDI region of the second semiconductor die, and the alignment carrier comprises a substrate having a coefficient of thermal expansion that substantially matches that of an interconnect bridge, a window located in a central portion of the substrate, and a plurality of solder balls located on the substrate, wherein a first set of the plurality of solder balls located on the substrate is aligned to, and in contact with, the plurality of first sacrificial bond pads located at the periphery region of the first semiconductor die, and a second set of the plurality of solder balls located on the substrate is aligned to, and in contact with, the plurality of second sacrificial bond pads located at the periphery region of the second semiconductor die;

forming the interconnect bridge through the window and spanning the first semiconductor die and the second semiconductor die to provide a second assembly comprising the first semiconductor die, the second semiconductor die, the interconnect bridge, and the alignment carrier, wherein the interconnect bridge connects the HDI region of the first semiconductor die to the HDI region of the second semiconductor die;

first attaching a backer structure to a backside of the first semiconductor die and the second semiconductor die of the second assembly;

removing the alignment carrier to provide a third assembly comprising the first semiconductor die, the second semiconductor die, the interconnect bridge and the backer structure; and

second attaching a laminate to the third assembly.

7. The method of claim 6, wherein the second attaching comprises a mass reflow of the first and second solder balls.

8. The method of claim 6, wherein the plurality of first sacrificial bond pads are formed at the same time as the first bond pads in the HDI region of the first semiconductor die, and the plurality of second sacrificial bond pads are formed at the same time as the second bond pads in the HDI region of the second semiconductor die.

9. The method of claim 6, further comprising removing the backer structure after the second attaching of the laminate.

10. A method comprising:

providing a first assembly comprising a first semiconductor die, a second semiconductor die located laterally adjacent to the first semiconductor die, and an alignment carrier, wherein the first semiconductor die comprises a plurality of first sacrificial bond pads located at a periphery region of the first semiconductor die, first solder balls located in a low density interconnect (LDI) region of the first semiconductor die and first bond pads located in a high density interconnect (HDI) region of the first semiconductor die, the second semiconductor die comprises a plurality of second sacrificial bond pads located at a periphery region of the second semiconductor die, second solder balls located in a LDI region of the second semiconductor die and second bond pads located in a HDI region of the second semiconductor die, and the alignment carrier comprises a substrate having a coefficient of thermal expansion that substantially matches that of an interconnect bridge, a window located in a central portion of the substrate, and a plurality of solder balls located on the substrate, wherein a first set of the plurality of solder balls located on the substrate is aligned to, and in contact with, the plurality of first sacrificial bond pads located at the periphery region of the first semiconductor die, and a second set of the plurality of solder balls located on the substrate is aligned to, and in contact with, the plurality of second sacrificial bond pads located at the periphery region of the second semiconductor die;

forming the interconnect bridge through the window and spanning the first semiconductor die and the second semiconductor die to provide a second assembly comprising the first semiconductor die, the second semiconductor die, the interconnect bridge, and the alignment carrier, wherein the interconnect bridge connects the HDI region of the first semiconductor die to the HDI region of the second semiconductor die;

removing the alignment carrier to provide a third assembly comprising the first semiconductor die, the second semiconductor die, and the interconnect bridge; and

attaching a laminate to the third assembly.

11. The method of claim 10, wherein the plurality of first sacrificial bond pads are formed at the same time as the first bond pads in the HDI region of the first semiconductor die, and the plurality of second sacrificial bond pads are formed at the same time as the second bond pads in the HDI region of the second semiconductor die.