

Description

The present invention relates to an apparatus for verifying the operation of an error detection circuit according to the preamble of claim 1.

In computer systems, data is being transferred between various components at very high rates. Usually these transfers occur in and out of a memory associated with the computer system to a central processing unit (CPU) or peripherals via a bus. In order to avoid errors, checks are generally made on the transferred data. However, for these checks to be valid, the detection circuitry must be operational.

Therefore, there is a need to provide logic which verifies the operability of these detection circuits without interference with the operation of the detection circuits in a normal mode of operation.

From US-A-4 360 915 such a logic is known. This known logic makes use of a parity generator at the output of a processor module and of a parity check circuit at the input of said processor module.

Departing from this known logic it is the object of the present invention to simplify such logic by doing the check and generate function by one and the same generator circuit.

This object is achieved by the characterizing features of claim 1. Further advantageous embodiments of the inventive apparatus may be taken from the dependent claims.

Therefore, there is supplied by the present invention, an apparatus for verifying the operability of an error detection circuit. In a computer system, having a plurality of components including a central processing unit (CPU) which is generating data as a result of its processing function, data is being transferred between a plurality of components via data lines operatively connected to each component involved in the transfer of the data. The data includes data bits and at least one associated check bit. The computer system includes at least one error detection circuit for checking the data bits and the associated check bit to verify that the data does not contain an error. An apparatus for verifying the operation of the error detection circuit, comprises a generator unit, operatively connected to the data lines for receiving data bits, for outputting a verification signal and a check bit signal. The verification signal indicates the validity of the data bits during a read operation, and the check bit signal is generated during a write operation. A gate element, having at least one input terminal adapted to receive at least one check bit, the gate element being operatively connected to the generator unit controls at least one input to the generator unit. A first control signal is transmitted to the generator unit causing the check bit signal generated by the

generator unit to be valid or invalid in response to the first control signal. Further, the check bit associated with the data is transmitted to the generator unit in response to a second control signal. The second control signal indicates that the read operation is in process thereby permitting the generator unit to perform a checking operation independent from the first control signal, thereby permitting verification of the error detection circuit, the checking operation being the verification of the data during the read operation.

The present invention will become more apparent when taken in conjunction with the following description and attached drawings, wherein like characters indicate like parts, and which drawings form a part of the present application.

Figure 1 shows a functional block diagram of a processing module of a computer system in which the preferred embodiment of the present invention is found;

Figure 2 shows a logic block diagram of a parity control register of the preferred embodiment of the present invention;

Figure 3 shows a logic block diagram of an address parity generator of the preferred embodiment of the present invention;

Figure 4 shows a logic block diagram of a data parity generation and check logic of the preferred embodiment of the present invention; and

Figure 5 shows a logic block diagram of a parity error detection circuit of the preferred embodiment of the present invention.

Referring to Figure 1, there is shown a block diagram of a processing module of a computer system, the computer system being made up of a plurality of modules. The processing module, which includes a microprocessor 10, communicates with other modules via a high speed parallel bus 20. During read, write, or read-modify-write operations by the processing module, 23 address bits (A01-A23) determine the address of the byte (or word) to be read or written. Three address parity bits (AP0-AP2) are generated by an address parity generation logic 25 for each address asserted on the bus 20 (in the preferred embodiment one parity bit for each byte of address). All other modules which interface to the bus 20 monitor the address and address parity information on the bus, each module on the bus being assigned a unique address. If the address asserted on the bus 20 matches the address assigned and the parity is correct, the module responds to the specific operation. If the address parity is incorrect there will no response from any module. The address parity check logic (not shown) on each module will prevent that module from responding if the address parity is incorrect even when there is a match between the asserted address and the modules assigned address.

Two data parity bits (DPOL, DPOU) are generated for each write operation to the bus 20 or to a local memory 30 associated with the processing module. In the preferred embodiment, the parity information for the local memory 30 is stored in a 16KX two-bit parity RAM 31. During power on initialization, data parity checking on the processing module is disabled via a parity control register 40 until the parity RAM 31 can be properly initialized. The parity bits for the local memory 30 are initialized by performing read/write operations to each address of memory 30. A write operation to a memory location with the data that has been previously stored in that location (fetched during the read) sets the parity bits to the proper state for that address. After data parity checking is enabled via the parity control register 40 in response to an instruction control signal, (INSTR) from microprocessor 10, data parity is checked during all read operations from the bus 20 and from the local memory 30. Data parity generation/check logic 50 generates parity for data outputted from the microprocessor 10, and checks parity for data inputted to the processing module from bus 20 or read from local memory 30, in response to control signals from the parity control register 40. Two output lines from the data parity generation/check logic 50 are coupled to parity error detection circuitry 60. Parity error detection circuitry 60 detects the presence of parity errors in response to control signals from the parity control register 40 and generates an error signal, ERROR, and couples the error signal to the microprocessor 10.

The parity control register 40 provides the capability for the microprocessor 10 to instruct the data parity generation/check logic 50 and the address parity generation logic 25 to generate improper parity on any specified parity bit. If the data parity generation/check logic 50 has been instructed to generate bad data parity, bad parity will be generated on the first write operation immediately following the write to the parity control register 40. If the address parity generation logic 25 has been instructed to generate bad address parity, bad parity will be generated until after the first write operation immediately following the write to the parity control register 40. There is no address parity on the local address bus, therefore instructions fetched from local memory 30 during the time that the address parity generation logic 25 is generating bad address parity on the processing module will be executed in a normal manner. The first write operation to an address of a memory location contained on a module coupled to bus 20 other than the processing module will test the capability of that module to detect an address parity error. As mentioned above, that module will not respond and in this fashion the address parity generation logic

25 and address parity detection circuitry of that module is verified. The data parity generation/check logic 50 on the processing module is checked by reading a memory location in which incorrect parity has been stored. When the microprocessor 10 receives the expected error signal, ERROR, the operation of the data parity generation/check logic 50 has been verified.

Referring to Figure 2, there is shown a logic block diagram of the parity control register 40. The parity control register 40 consists of two parts. The first part of the parity control register 40 includes a latch 41 which contain the bits specifying which byte of the address or data information is to be generated with bad parity. The second part of the parity control register 40 is implemented with a D-type flip-flop 42. The D-type flip-flop 42 contains a bit which specifies if data parity checking is to be enabled or disabled on the processing module, the enable/disable signal (ENPTYC, also denoted ENA/DIS) being coupled to the parity error detection circuitry 60. The output signals of latch 41, BADAP0-2 form the address parity control signals and are coupled to the address parity generation logic 25 and specify which byte of the address information is to be generated with bad parity, BADAP0 being related to the least significant byte of the address information. The output signals of latch 41, BADDPU and BADDPL form the data parity control signals and are coupled to the data parity generation/check logic 50 and specify which byte of the data information is to be generated with bad parity, BADDPL being related to the least significant byte of data information. Both the latch 41 and the D-type flip-flop 42 are cleared following the application of a master reset signal (MCPRST). Signal BHPTYA is a signal which becomes active when the address of the parity control register 40 is decoded. Signals BHPTYC is generated by ANDing the decoded address signal BHPTYA with a write strobe, UFCWRT, the write strobe being a control signal from the microprocessor 10. Signal UPFC05, which indicates a supervisor data operation is being performed is combined with signal BHPTYC, forming the signal CKBHPY used to clock the contents of the buffered data bits, BUFD02-BUFD07, into the parity control register 40. J-K flip-flop 43 is set via the active transmission of signal BHPTYA when a write to the parity control register 40 is being performed. This removes the clear to the latch 41 and allows a parity control word (BUFD02-BUFD06) to be latched on the trailing edge of the clock signal CKBHPY. J-K flip-flop 43 remains set until a write to an address other than the parity control register 40 is performed. Signal UPADST is a signal from the microprocessor 10 which indicates a valid address is being asserted on address lines 1-23. The trailing edge of

signal UPADST is used to clock J-K flip-flop 43 reset terminal if BHPTYA is not asserted and UPCWRT is a logic one (when UPCWRT is a logic one, a write operation is occurring). The microprocessor of the preferred embodiment is a Motorola 68000.

Referring to Figure 3, there is shown a logic block diagram of the address parity generation logic 25. The address parity generation logic 25 of the preferred embodiment consists of three Fairchild F280 parity generator integrated circuit chips, 25-1, 25-2, 25-3. Signals BADAP0-2 are coupled from the parity control register 40. When the signal BADAP0 is a logic zero, the proper parity is generated on the output MBAPY0, which corresponds to the address parity signal AP0. When signal BADAP0 is a logic one, the parity generator 25-1 generates an incorrect or bad parity on output MBAPY0. A similar effect occurs relative to signals BADAP1 and BADAP2, with respect to the output parity bits MBAPY1 and MBAPY2, respectively. The input signals UPBA01-UPBA23 represent the address lines A01-A23.

Referring to Figure 4, there is shown a logic block diagram of the data parity generation/check logic 50. A program in the microprocessor 10 is executing performing a test of the parity check logic. The program purposely commands data with bad parity to be generated and written into memory 30. While the program is executing, and the command for data with bad (or invalid) parity generation is still active, instructions are being read from memory 30 and it is desirable to read these instruction words from memory 30 without interrupting the parity check function even though the parity control register 40 is set up to command the generation of bad parity. Hence, logic is included so that once the control is set-up, the invalid parity generate function and the valid parity check function are non-interfering and without having to alternate control function in between valid and invalid parity operations since the parity generation/check logic 50 is performing both the generation and checking function.

Also, a program is also executed in microprocessor 10 to perform a test of the parity check circuitry of the other modules coupled to bus 20 other than the processing module by purposely commanding data with bad parity to be generated and written to those bus-coupled-modules. Under this situation an error signal (not shown) is expected to be returned from the module's parity error detection circuit 60' (not shown) to microprocessor 10 in response to the write operation with incorrect parity, thereby checking the ability of that module's parity error detection circuit 60' to detect and report data parity errors.

The data parity generation/check logic 50 of

the preferred embodiment of the present invention is comprised of two Fairchild F280 parity generators 51, 52, two AND gates 53, 54, and two exclusive-OR gates 55, 56 which allow incorrect data parity to be generated during write operations and data parity checking to be performed correctly during read operations without having to modify the input control signals from the parity control register 40 while a test is being performed requiring both read and write operations. The parity generators 51, 52 generate parity, GENDPL, GENDPU, during write operations, and check parity during read operations, DPELWR and DPEUPR. The generated parity signals GENDPL and GENDPU are coupled to bus drivers (not shown) and memory 30, and the parity indicator signals DPELWR and DPEUPR are coupled to the parity error detection circuitry 60.

When proper data parity is to be generated, signals BADDPL and BADDPU from parity control register 40 are a logic zero. This causes GBADPL and GBADPU to be a logic zero and further causes DAPTYL and DAPTYU to be a logic one (or high). Input signals LCBPYL and LCBPYU are a logic one for write operations since the parity RAM 31 output and module bus receiver (not shown) are tristated during this period of time. Since DAPTYL is a logic one the sum 0 output of parity generator 51 will generate the correct parity.

A logic one for the signal BADDPL will cause improper parity to be generated on GENDPL for write operations. This is because GBADPL is a logic one resulting in DAPTYL being a logic zero. A similar relationship holds true between signals BADDPU and GENDPU. Parity checking is not affected by the state of the signals BADDPL or BADDPU since signal UPCWRT is a logic zero during read operations.

During read operations the parity bit is contained in signals LCBPYL and LCBPYU received from the bus receivers (not shown) or the parity RAM 31 output. The state of LCBPYL and LCBPYU are reflected in the state of DAPTYL. Hence if all the eight input bits UPBD00-UPBD07 plus the parity bit LCBPYL are an odd number of bits in the logic one state the sum E output is low, i.e., DPELWR is low, indicating no error for the read. The number of logic ones presented on the inputs of the respective parity generators 51, 52 are reflected in the respective outputs sum E and sum 0 of the respective parity generators 51, 52. There should be an odd number of ones present if the parity is correct for the data presented. Therefore, DPELWR and DPEUPR should be low, or a logic zero. These parity check output signals are coupled to the parity error detection circuitry 60.

Referring to Figure 5, there is shown a logic block diagram of the parity error detection circuit 60. Signals DPELWR and DPEUPR are allowed to

pass through gate 62 if parity checking is enabled, i.e., signal ENPTYC from parity control register 40 is a logic one, upper and lower data strobe signals from the microprocessor 10 (UPDSTU and UPDSTL) are asserted, and a read operation is occurring, i.e., UPCWRT- is high. A clock signal, READCK, clocks the data parity flip-flop 61 after sufficient time has passed for signal DATAPE to have been stable for at least some predetermined period of time. If an error in the parity has been detected, the error signal, ERROR, is outputted to the microprocessor 10.

Claims

1. Apparatus for verifying the proper operation of an error detection circuit of a module in a data processing system having a plurality of modules and a processing module which comprises a CPU (10), where information is transferred on a bus from one module to another or from the processing module to one of a plurality of modules in the form of a group of signals representing a set of information bits and at least one check bit, said check bit in association with said information bit set representing the correctness of said information bit set, and wherein said error detection circuit upon receipt of said signal group delivers a signal denoting whether said information bit set contains an error or not, said apparatus being comprised in said processing module and being characterized by

comprising:

a generator circuit (51) for receiving from said CPU (10) said set of information bits (UPBD 00-07) at a set of input terminals and for receiving an additional signal (DAPTYL) at an additional input terminal, said generator circuit (51), in a read mode of operation, generating a first output signal (DPELWR) denoting whether the set of information bits received contains an error, and in a write mode of operation, generating a second output signal (GENDPL) representing the check bit for the set of information bits received thereby; and

a gate circuit (53,55) for delivering said additional signal (DAPTYL) to said generator circuit, said gate circuit receiving at least first and second input signals, said first input signal (LCBPYL) representing the check bit signal associated with the set of information bits received by said generator circuit, said second input signal (BADDPL) denoting whether the check bit generated by said

generator circuit is to be a valid or invalid check bit, said gate circuit in said read mode of operation causing said additional signal to correspond to said first input signal and in said write mode of operation causing said additional signal to correspond to said second input signal, so that in the write mode the group of signals, having a valid or invalid parity depending on the value of said second input signal, is transferred on said bus to test the capability of the error detection circuit of the addressed module to detect an error.

2. An apparatus according to claim 1, further characterized by :

error detection means (60), operatively connected to said generator circuit (51), for outputting an error signal in response to an enable signal.

3. An apparatus according to claim 2, further characterized by :

register means (40), operatively connected to said gate means (53,55) and to said error detection means (60) and to said CPU for generating said second input signal and said enable signal.

Revendications

1. Dispositif pour la vérification du fonctionnement correct d'un circuit de détection d'erreur d'un module dans un système de traitement de données ayant plusieurs modules et un module de traitement qui comporte une unité centrale de traitement (CPU) (10), où de l'information est transférée sur un bus d'un module vers l'autre ou du module de traitement vers un module parmi plusieurs modules sous la forme d'un groupe de signaux représentant un ensemble de bits d'information et au moins un bit de contrôle, ledit bit de contrôle en association avec ledit ensemble de bits d'information représentant la justesse dudit ensemble de bits d'information, et dans lequel ledit circuit de détection d'erreur délivre à la réception dudit groupe de signaux un signal indiquant si ledit ensemble de bits d'information contient une erreur ou non, ledit dispositif étant compris dans ledit module de traitement et étant caractérisé en ce qu'il comprend :

un circuit générateur (51) destiné à recevoir de ladite unité centrale de traitement (CPU) (10) ledit ensemble de bits d'information (UPBD 00 à 07) sur un ensemble de bornes d'entrée et destiné à recevoir un signal ad-

pass through gate 62 if parity checking is enabled, i.e., signal ENPTYC from parity control register 40 is a logic one, upper and lower data strobe signals from the microprocessor 10 (UPDSTU and UPDSTL) are asserted, and a read operation is occurring, i.e., UPCWRT- is high. A clock signal, READCK, clocks the data parity flip-flop 61 after sufficient time has passed for signal DATAPE to have been stable for at least some predetermined period of time. If an error in the parity has been detected, the error signal, ERROR, is outputted to the microprocessor 10.

Claims

1. Apparatus for verifying the proper operation of an error detection circuit of a module in a data processing system having a plurality of modules and a processing module which comprises a CPU (10), where information is transferred on a bus from one module to another or from the processing module to one of a plurality of modules in the form of a group of signals representing a set of information bits and at least one check bit, said check bit in association with said information bit set representing the correctness of said information bit set, and wherein said error detection circuit upon receipt of said signal group delivers a signal denoting whether said information bit set contains an error or not, said apparatus being comprised in said processing module and being **characterized by** comprising:

a generator circuit (51) for receiving from said CPU (10) said set of information bits (UPBD 00-07) at a set of input terminals and for receiving an additional signal (DAPTYL) at an additional input terminal, said generator circuit (51), in a read mode of operation, generating a first output signal (DPELWR) denoting whether the set of information bits received contains an error, and in a write mode of operation, generating a second output signal (GENDPL) representing the check bit for the set of information bits received thereby; and

a gate circuit (53,55) for delivering said additional signal (DAPTYL) to said generator circuit, said gate circuit receiving at least first and second input signals, said first input signal (LCBPYL) representing the check bit signal associated with the set of information bits received by said generator circuit, said second input signal (BADDPL) denoting whether the check bit generated by said

generator circuit is to be a valid or invalid check bit, said gate circuit in said read mode of operation causing said additional signal to correspond to said first input signal and in said write mode of operation causing said additional signal to correspond to said second input signal, so that in the write mode the group of signals, having a valid or invalid parity depending on the value of said second input signal, is transferred on said bus to test the capability of the error detection circuit of the addressed module to detect an error.

2. An apparatus according to claim 1, further **characterized by** :
error detection means (60), operatively connected to said generator circuit (51), for outputting an error signal in response to an enable signal.
3. An apparatus according to claim 2, further **characterized by** :
register means (40), operatively connected to said gate means (53,55) and to said error detection means (60) and to said CPU for generating said second input signal and said enable signal.

Revendications

1. Dispositif pour la vérification du fonctionnement correct d'un circuit de détection d'erreur d'un module dans un système de traitement de données ayant plusieurs modules et un module de traitement qui comporte une unité centrale de traitement (CPU) (10), où de l'information est transférée sur un bus d'un module vers l'autre ou du module de traitement vers un module parmi plusieurs modules sous la forme d'un groupe de signaux représentant un ensemble de bits d'information et au moins un bit de contrôle, ledit bit de contrôle en association avec ledit ensemble de bits d'information représentant la justesse dudit ensemble de bits d'information, et dans lequel ledit circuit de détection d'erreur délivre à la réception dudit groupe de signaux un signal indiquant si ledit ensemble de bits d'information contient une erreur ou non, ledit dispositif étant compris dans ledit module de traitement et étant caractérisé en ce qu'il comprend :

un circuit générateur (51) destiné à recevoir de ladite unité centrale de traitement (CPU) (10) ledit ensemble de bits d'information (UPBD 00 à 07) sur un ensemble de bornes d'entrée et destiné à recevoir un signal ad-



- ditionnel (DAPTYL) sur une borne d'entrée additionnelle, ledit circuit générateur (51), dans un mode de fonctionnement en lecture, engendrant un premier signal de sortie (DPELWR) indiquant si l'ensemble de bits d'information reçu contient une erreur, et dans un mode de fonctionnement en écriture, engendrant un deuxième signal de sortie (GENDPL) représentant le bit de contrôle pour l'ensemble de bits d'information reçu; et
- un circuit de porte (53, 55) destiné à délivrer ledit signal additionnel (DAPTYL) audit circuit générateur, ledit circuit de porte recevant au moins des premier et deuxième signaux d'entrée, ledit premier signal d'entrée (LCBPYL) représentant le signal de bit de contrôle associé à l'ensemble de bits d'information reçu par ledit circuit générateur, ledit deuxième signal d'entrée (BADDPL) indiquant si le bit de contrôle engendré par ledit circuit générateur doit être un bit de contrôle valide ou non valide, ledit circuit de porte dans ledit mode de fonctionnement en lecture amenant ledit signal additionnel à correspondre audit premier signal d'entrée et dans ledit mode de fonctionnement en écriture amenant ledit signal additionnel à correspondre audit deuxième signal d'entrée, de telle sorte que dans le mode en écriture, le groupe de signaux, ayant une parité valide ou non valide en fonction de la valeur dudit deuxième signal d'entrée, est transféré sur ledit bus afin de tester la capacité du circuit de détection d'erreur du module adressé à détecter une erreur.
2. Dispositif selon la revendication 1, caractérisé en outre par :
 - des moyens de détection d'erreur (60), reliés de manière active audit circuit générateur (51), afin de délivrer un signal d'erreur en réponse à un signal de validation.
 3. Dispositif selon la revendication 2, caractérisé en outre par :
 - des moyens de registre (40), reliés de manière active auxdits moyens de porte (53, 55) et aux
 - dits moyens de détection d'erreur (60) et à ladite unité centrale de traitement (CPU), afin d'engendrer ledit deuxième signal d'entrée et ledit signal de validation.

Ansprüche

1. Gerät zur Überprüfung des richtigen Betriebs eines Fehler-Feststellschaltkreises eines Moduls in einem Datenverarbeitungssystem, welches mehrere Module und einen Verarbeitungsmodul mit einer Zentraleinheit CPU (10) aufweist, wobei Information auf einem Bus von einem Modul zu einem anderen oder von dem Verarbeitungsmodul zu einem der mehreren Module in der Form einer Gruppe von Signalen übertragen wird, die eine Gruppe von Informationsbits und wenigstens ein Prüfbit umfassen, wobei das Prüfbit in Verbindung mit der Informationsbitgruppe die Richtigkeit der Informationsbitgruppe repräsentiert und wobei der Fehler-Feststellschaltkreis beim Empfang der Signalgruppe ein Signal abgibt, das anzeigt, ob die Informationsbitgruppe einen Fehler enthält oder nicht und das Gerät in dem Verarbeitungsmodul enthalten ist und dadurch gekennzeichnet ist, daß es enthält:

einen Generatorschaltkreis (51) zum Empfang der Gruppe von Informationsbits (UPBD00-07) an einer Gruppe von Eingangsanschlüssen der CPU (10) und zum Empfang eines zusätzlichen Signales (DAPTYL) an einem zusätzlichen Eingangsanschluß, wobei der Generatorschaltkreis (51) in einem Lese-Operationsmodus ein erstes Ausgangssignal (DPELWR) erzeugt, welches anzeigt, ob die Gruppe der empfangenen Informationsbits einen Fehler enthält und in einem Schreib-Operationsmodus ein zweites Ausgangssignal (GENDPL) erzeugt, welches das Prüfbit für die Gruppe der empfangenen Informationsbits darstellt; und

einen Gatterschaltkreis (53,55) zur Abgabe des zusätzlichen Signales (DAPTYL) an den Generatorschaltkreis, wobei der Gatterschaltkreis wenigstens erste und zweite Eingangssignale empfängt und das erste Eingangssignal (LCBPYL) das Prüfbit darstellt, das der von dem Generatorschaltkreis empfangenen Gruppe von Informationsbits zugeordnet ist, und das zweite Eingangssignal (BADDPL) angibt, ob das durch den Generatorschaltkreis erzeugte Prüfbit ein gültiges oder ungültiges Prüfbit ist, wobei der Gatterschaltkreis im Lese-Operationsmodus das zusätzliche Signal veranlaßt, dem ersten Eingangssignal zu entsprechen und im Schreib-Operationsmodus das zusätzliche Signal veranlaßt, dem zweiten Eingangssignal zu entsprechen, so daß im Schreibmodus die Gruppe von Signalen, die eine gültige oder ungültige Parität in Abhängigkeit von dem Wert des zweiten Eingangssigna-



les besitzen, auf den Bus übertragen wird, um die Fähigkeit des Fehler-Feststellschaltkreises des adressierten Moduls zur Feststellung eines Fehlers zu testen.

2. Gerät nach Anspruch 1, ferner **gekennzeichnet durch** :

Fehler-Feststellmittel (60), die an den Generatorschaltkreis (51) angeschlossen sind, um ein Fehlersignal auf Grund eines Freigabesignales auszugeben.

3. Gerät nach Anspruch 2, ferner **gekennzeichnet durch** :

ein Register (40), das an den Gatterschaltkreis (53,55), den Fehler-Feststellschaltkreis (60) und die CPU angeschlossen ist, um das zweite Eingangssignal und das Freigabesignal zu erzeugen.

5

10

15

20

25

30

35

40

45

50

55

7

