

ABSTRACT

Disclosed is a clock converting circuit, which includes a first switch that is connected between a first input node for receiving a second input clock and a first node and operates in response to a first logic state of a first input clock, the second input clock delayed with
5 respect to the first input clock as much as 90 degrees, a second switch that is connected between a second input node for receiving the first input clock and a second node and operates in response to a second logic state of the second input clock, and a third switch that is connected between the second node and a ground node and operates in response to a first
10 logic state of the second input clock opposite to the second logic state of the second input clock.

FIG. 5A