

DESCRIPTION

Title of Invention: MULTILEVEL POWER CONVERTOR

5 Technical Field

[0001]

The present invention relates to a multilevel power convertor for high voltage and large capacity.

Background Art

10 [0002]

A power convertor is configured by main circuit switching elements which are semiconductor elements (a module formed by a semiconductor switching element such as IGBT and a diode which is connected in reverse parallel to the semiconductor switching element; this is the same in the following description). As means for generating a high voltage in the power convertor, there is a circuit configuration in which a plurality of semiconductor elements are connected in series to each other.

20 [0003]

A multilevel power convertor, like the above power convertor, which outputs five-level voltages in the circuit configuration in which the plurality of semiconductor elements are connected in series to each other, has been proposed. As one of configurations of the multilevel power convertor, a circuit configuration as disclosed in PATENT DOCUMENT 1 has been proposed. In PATENT DOCUMENT 1, as illustrated in Fig. 27 of the present application, DC voltage sources DCC1 and DCC2, and flying capacitors FC1 and FC2 are in common to three phases,

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and thus the number of capacitors used in the multilevel power convertor can be reduced, thereby allowing size reduction of the device.

#### Citation List

5 Patent Literature

[0004]

[PATENT DOCUMENT 1] Japanese Patent Application No. 2012-209368

#### Summary of Invention

10 [0005]

However, in the circuit configuration illustrated in Fig. 27, since capacitors and some semiconductor elements S1 to S4 are in common to three phases, as a problem, a combination of output voltages which cannot be outputted is present. Specifically, when attempting to output phase voltages of  $2E$ ,  $0$  and  $-2E$  from output terminals U, V and W respectively, since the flying capacitor FC1 is short-circuited, it is impossible to output a combination of these phase voltages.

20 [0006]

A specific example will be described with reference to Fig. 28. Here, Fig. 28 illustrates an example in which a U phase outputs a voltage of  $2E$ , a V phase outputs a voltage of  $0$ , and a W phase outputs a voltage of  $-2E$ . In addition, in Fig. 28, a circular mark indicates a turned-on semiconductor element.

[0007]

As illustrated in Fig. 28, when attempting to simultaneously output the voltages of  $2E$ ,  $0$  and  $-2E$  from the output terminals U, V and W respectively,

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semiconductor elements S1 and S2 at both ends of a flying capacitor FC1 are simultaneously turned on, and thus the flying capacitor FC1 is short-circuited. As a result, an overcurrent flows through a short-circuited loop of  
5 DCC1→S1→FC1→S2→DCC1.

[0008]

Because of this problem, in the case of the circuit configuration illustrated in Fig. 27, it is impossible to select the semiconductor element that is turned-on  
10 as illustrated in Fig. 28, and thus the voltages of 2E, 0, and -2E are cannot be simultaneously output.

[0009]

In the case of the circuit configuration illustrated in Fig. 27, since the voltages of 2E, 0 and -2E cannot  
15 be simultaneously outputted from the output terminals U, V and W respectively, these outputs are replaced with a combination of other output voltages as an alternative method. For example, as the alternative method, by repeatedly outputting voltages of 2E, E and -2E and  
20 voltages of 2E, -E and -2E from the output terminals U, V and W respectively then outputting each average voltage of 2E, 0 and -2E, the voltages of 2E, 0 and -2E are replaced with the respective average voltages.

[0010]

25 However, it is required, all the time, to equalize times for which voltages of 2E, E and -2E, and voltages of 2E, -E and -2E are outputted from the output terminals U, V and W respectively, and also time management is required all the time. As a result, this causes a problem  
30 of complicating the control. This problem also occurs

in a case of a circuit configuration in which the number of output phases is increased to four or greater, using Fig. 27.

[0011]

5        On the other hand, in [Embodiment 5] of PATENT DOCUMENT 1 illustrated in Fig. 29(a) of the present application and [Embodiment 6] of PATENT DOCUMENT 1 illustrated in Fig. 29(b) of the present application, in a case where an application voltage of each of DC voltage sources DCC1 and DCC2 is  $2E$  and an application voltage of each of flying capacitors CFC1 and CFC2 is  $E$ , voltages of  $2E$ ,  $0$  and  $-2E$  can be simultaneously output from output terminals OUT U, OUT V and OUT W respectively. However, the following problems (1) and (2) occur in the circuit configurations illustrated in Figs. 29(a) and 29(b).

[0012]

(1) In the circuit configurations illustrated in Figs. 29(a) and 29(b), a steady voltage maximum value which is applied to semiconductor elements SU5, SU6, SV5, SV6, SW5 and SW6 connected to the output terminals OUT U, OUT V and OUT W is  $3E$ . A semiconductor element with high withstand voltage is consequently necessary, and as a problem, this has a disadvantage in size reduction of the device and in cost of the device.

[0013]

(2) Since currents of three phases of the U phase, the V phase and the W phase flow through semiconductor elements S2.1 to S2.3, and S1.1 to S1.3 that are shown by circular marks in Figs 29(a) and 29(b), a large-sized cooling fin with a high cooling effect is required to

cool these semiconductor elements S2.1 to S2.3, and S1.1 to S1.3.

[0014]

The above problems (1) and (2) also occur in a circuit  
5 configuration in which the number of output phases is increased to four or greater by employing Figs. 29(a) and 29(b).

[0015]

In view of the foregoing, an object of the present  
10 invention is to output an arbitrary voltage from all phases and to simplify a control for outputting an arbitrary voltage level from the all phases in a multiphase and multilevel power convertor.

[0016]

15 The present invention was made in view of the above problem. According to one aspect of the present invention, a multilevel power convertor that generates AC outputs with a plurality of voltage levels obtained by conversion of voltages of a DC voltage source and a flying capacitor,  
20 comprises: N DC voltage sources ( $N \geq 2$ ) that are connected in series to each other; basic circuits of M phases ( $M \geq 3$ ), each of which includes first to fourth semiconductor elements that are sequentially connected in series between positive and negative electrodes of each of the N DC voltage  
25 sources; a fifth semiconductor element whose one end is connected to a common connection point of the first and second semiconductor elements; and a sixth semiconductor element whose one end is connected to a common connection point of the third and fourth semiconductor elements;  
30 a flying capacitor that is inserted between the other

ends of the fifth semiconductor elements of all the phases and the other ends of the sixth semiconductor elements of all the phases, the flying capacitor being in common to the M phases; and voltage selection circuits of the M phases, each of which has common connection points of the second and third semiconductor elements of each basic circuit as input terminals, includes semiconductor elements between the input terminals and an output terminal, and outputs a potential of any one of the input terminals from the output terminal by selectively controlling ON/OFF of the semiconductor elements.

[0017]

According to another aspect of the present invention, A multilevel power convertor that generates AC outputs with a plurality of voltage levels obtained by conversion of voltages of a DC voltage source and a flying capacitor, comprises: N DC voltage sources (N = an even number of 2 or greater) that are connected in series to each other; basic circuits that include a first semiconductor element whose one end is connected to a positive electrode end of a DC voltage source in an even-numbered stage of the N serially connected DC voltage sources, the first semiconductor element being in common to M phases ( $M \geq 3$ ); second to fourth semiconductor elements of the M phases which are sequentially connected in series between the other end of the first semiconductor element in the even-numbered stage and a negative electrode end of the DC voltage source in the even-numbered stage; sixth semiconductor elements of the M phases whose one ends are connected to common connection points of the third

and fourth semiconductor elements in the even-numbered stage; a fourth semiconductor element whose one end is connected to a negative electrode end of a DC voltage source in an odd-numbered stage, the fourth semiconductor element being in common to the M phases; first to third semiconductor elements of the M phases which are sequentially connected in series between a positive electrode end of the DC voltage source in the odd-numbered stage and the other end of the fourth semiconductor element in the odd-numbered stage; and fifth semiconductor elements of the M phases whose one ends are connected to common connection points of the first and second semiconductor elements in the odd-numbered stage; a flying capacitor in the even-numbered stage that is inserted between a common connection point of the first and second semiconductor elements in the even-numbered stage and the other ends of the sixth semiconductor elements of all the phases in the even-numbered stage, the flying capacitor being in common to the M phases; a flying capacitor in the odd-numbered stage that is inserted between the other ends of the fifth semiconductor elements of all the phases in the odd-numbered stage and a common connection point of the third and fourth semiconductor elements in the odd-numbered stage, the flying capacitor being in common to the M phases; and voltage selection circuits of the M phases, each of which has common connection points of the second and third semiconductor elements of each basic circuit as input terminals, includes semiconductor elements between the input terminals and an output terminal, and outputs a potential

of any one of the input terminals from the output terminal by selectively controlling ON/OFF of the semiconductor elements.

[0018]

5           In addition, according to still aspect of the present invention, a multilevel power convertor that generates AC outputs with a plurality of voltage levels obtained by conversion of voltages of a DC voltage source and a flying capacitor, comprises: N DC voltage sources (N =  
10   an even number of 2 or greater) that are connected in series to each other; basic circuits that include a fourth semiconductor element whose one end is connected to a negative electrode end of a DC voltage source in an even-numbered stage of the N serially connected DC voltage  
15   sources, the fourth semiconductor element being in common to M phases (where  $M \geq 3$ ); first to third semiconductor elements of the M phases which are sequentially connected in series between a positive electrode end of the DC voltage source in the even-numbered stage and the other end of  
20   the fourth semiconductor element in the even-numbered stage; fifth semiconductor elements of the M phases whose one ends are connected to common connection points of the first and second semiconductor elements in the even-numbered stage; a first semiconductor element whose  
25   one end is connected to a positive electrode end of a DC voltage source in an odd-numbered stage, the first semiconductor element being in common to the M phases; second to fourth semiconductor elements of the M phases which are sequentially connected in series between the  
30   other end of the first semiconductor element in the

odd-numbered stage and a negative electrode end of the DC voltage source in the odd-numbered stage; and sixth semiconductor elements of the M phases whose one ends are connected to common connection points of the third and fourth semiconductor elements in the odd-numbered stage; a flying capacitor in the even-numbered stage that is inserted between all the fifth semiconductor elements and a common connection point of the third and fourth semiconductor elements in the even-numbered stage, the flying capacitor being in common to the M phases; a flying capacitor in the odd-numbered stage that is inserted between a common connection point of the first and second semiconductor elements and all the sixth semiconductor elements in the odd-numbered stage, the flying capacitor being in common to the M phases; and voltage selection circuits of the M phases, each of which has common connection points of the second and third semiconductor elements of each basic circuit as input terminals, includes semiconductor elements between the input terminals and an output terminal, and outputs a potential of any one of the input terminals from the output terminal by selectively controlling ON/OFF of the semiconductor elements.

[0019]

Further, according to still further aspect of the present invention, a multilevel power convertor that generates AC outputs with a plurality of voltage levels obtained by conversion of voltages of a DC voltage source and a flying capacitor, comprises: N DC voltage sources (N = an even number of 2 or greater) that are connected

in series to each other; basic circuits of  $M$  phases ( $M \geq 3$ ), each of which includes second and third semiconductor elements which are sequentially connected in series to a positive electrode end of a DC voltage source in an even-numbered stage of the  $N$  serially connected DC voltage sources; and third and second semiconductor elements which are sequentially connected in series to a negative electrode end of a DC voltage source in the odd-numbered stage of the  $N$  serially connected DC voltage sources; a flying capacitor that is connected parallel to the second and third semiconductor elements in each of the even-numbered stage and odd-numbered stage, the flying capacitor being in common to the  $M$  phases; and voltage selection circuits of the  $M$  phases, each of which has common connection points of the second and third semiconductor elements of each basic circuit and a common connection point of a negative electrode end of the DC voltage source in the even-numbered stage and a positive electrode end of the DC voltage source in the odd-numbered stage as input terminals, includes semiconductor elements between the input terminals and an output terminal, and outputs a potential of any one of the input terminals from the output terminal by selectively controlling ON/OFF of the semiconductor elements.

[0020]

According to still further aspect of the present invention, a multilevel power convertor that generates AC outputs with a plurality of voltage levels obtained by conversion of voltages of a DC voltage source and a flying capacitor, comprises:  $N$  DC voltage sources ( $N =$

an even number of 2 or greater) that are connected in series to each other; basic circuits of  $M$  phases ( $M \geq 3$ ), each of which includes second to fourth semiconductor elements which are sequentially connected in series  
5 between positive and negative electrode ends of a DC voltage source in an even-numbered stage of the  $N$  serially connected DC voltage sources; a sixth semiconductor element whose one end is connected to a common connection point of the third and fourth semiconductor elements in  
10 the even-numbered stage; first to third semiconductor elements which are sequentially connected in series between positive and negative electrode ends of a DC voltage source in an odd-numbered stage of the  $N$  serially connected DC voltage sources; and a fifth semiconductor  
15 element whose one end is connected to a common connection point of the first and second semiconductor elements in the odd-numbered stage; a flying capacitor in the even-numbered stage that is inserted between the other ends of all the sixth semiconductor elements in the  
20 even-numbered stage and a common connection point of a positive electrode end of the DC voltage source and the second semiconductor element in the even-numbered stage, the flying capacitor being in common to the  $M$  phases; a flying capacitor in the odd-numbered stage that is  
25 inserted between the other ends of all the fifth semiconductor elements in the odd-numbered stage and a common connection point of a negative electrode end of the DC voltage source and the third semiconductor element in the odd-numbered stage, the flying capacitor being  
30 in common to the  $M$  phases; and voltage selection circuits

of the  $M$  phases, each of which has common connection points of the second and third semiconductor elements of each basic circuit as input terminals, includes semiconductor elements between the input terminals and an output terminal, and outputs a potential of any one of the input terminals from the output terminal by selectively controlling ON/OFF of the semiconductor elements.

[0021]

In addition, according to still further aspect of the present invention, a multilevel power convertor that generates AC outputs with a plurality of voltage levels obtained by conversion of voltages of a DC voltage source and a flying capacitor, comprises:  $N$  DC voltage sources ( $N$  = an even number of 2 or greater) that are connected in series to each other; basic circuits of  $M$  phases ( $M \geq 3$ ), each of which includes first to third semiconductor elements which are sequentially connected in series between positive and negative electrode ends of a DC voltage source in an even-numbered stage of the  $N$  serially connected DC voltage sources; a fifth semiconductor element whose one end is connected to a common connection point of the first and second semiconductor elements in the even-numbered stage; second to fourth semiconductor elements which are sequentially connected in series between positive and negative electrode ends of a DC voltage source in an odd-numbered stage of the  $N$  serially connected DC voltage sources; and a sixth semiconductor element whose one end is connected to a common connection point of the third and fourth semiconductor elements in the odd-numbered stage; a flying capacitor in the

even-numbered stage that is inserted between the other ends of all the fifth semiconductor elements in the even-numbered stage and a common connection point of a negative electrode end of the DC voltage source and the  
5 third semiconductor element in the even-numbered stage, the flying capacitor being in common to the M phases; a flying capacitor in the odd-numbered stage that is inserted between the other ends of all the sixth semiconductor elements in the odd-numbered stage and a  
10 common connection point of a positive electrode end of the DC voltage source and the second semiconductor element in the odd-numbered stage, the flying capacitor being in common to the M phases; and voltage selection circuits of the M phases, each of which has common connection points  
15 of the second and third semiconductor elements of each basic circuit as input terminals, includes semiconductor elements between the input terminals and an output terminal, and outputs a potential of any one of the input terminals from the output terminal by selectively  
20 controlling ON/OFF of the semiconductor elements.

[0022]

Further, the number of series-connection of all or some of the semiconductor elements in the basic circuits and the voltage selection circuits could be equal to or  
25 greater than 2.

[0023]

Furthermore, the number of parallel-connection of all or some of the semiconductor elements in the basic circuits and the voltage selection circuits could be equal  
30 to or greater than 2.

[0024]

According to the present invention, it is possible to output the arbitrary voltage from all phases and to simplify the control for outputting the arbitrary voltage level from the all phases in the multiphase and multilevel power convertor.

#### Brief Description of Drawings

[0025]

Fig. 1 is a diagram illustrating a basic cell.

10 Fig. 2 is a diagram illustrating a basic circuit in which N basic cells are connected in series to each other.

Fig. 3 shows circuit configuration diagrams illustrating voltage selection circuits.

15 Fig. 4 is a diagram illustrating a multilevel power convertor in Embodiment 1.

Fig. 5 is a diagram illustrating a multilevel power convertor in Embodiment 2.

20 Fig. 6 is a diagram illustrating a multilevel power convertor in Embodiment 3.

Fig. 7 is a diagram illustrating a multilevel power convertor in Embodiment 4.

Fig. 8 is a diagram illustrating a multilevel power convertor in Embodiment 5.

25 Fig. 9 is a circuit configuration diagram illustrating a basic cell in Embodiment 6.

Fig. 10 is a circuit configuration diagram illustrating a multilevel power convertor in Embodiment 6.

Fig. 11 is a diagram illustrating an operation example for each output voltage in Embodiment 6.

Fig. 12 is a diagram illustrating an operation example of the multilevel power convertor in Embodiment  
5 6.

Fig. 13 is a circuit configuration diagram illustrating a multilevel power convertor in Embodiment  
7.

Fig. 14 is a diagram illustrating an operation example of the multilevel power convertor in Embodiment  
10 7.

Fig. 15 is a circuit configuration diagram illustrating a multilevel power convertor in Embodiment  
8.

Fig. 16 is a diagram illustrating an operation example of the multilevel power convertor in Embodiment  
15 8.

Fig. 17 is a circuit configuration diagram illustrating a multilevel power convertor in Embodiment  
20 9.

Fig. 18 is a diagram illustrating an operation example of the multilevel power convertor in Embodiment  
9.

Fig. 19 is a circuit configuration diagram illustrating a multilevel power convertor in Embodiment  
25 10.

Fig. 20 is a diagram illustrating an operation example of the multilevel power convertor in Embodiment  
10.

Fig. 21 is a circuit configuration diagram illustrating a multilevel power convertor in Embodiment 11.

Fig. 22 is a diagram illustrating an operation example of the multilevel power convertor in Embodiment 11.

Fig. 23 is a circuit configuration diagram illustrating a multilevel power convertor in Embodiment 12.

Fig. 24 is a diagram illustrating an operation example of the multilevel power convertor in Embodiment 12.

Fig. 25 is a circuit configuration diagram illustrating a multilevel power convertor in Embodiment 13

Fig. 26 is a circuit configuration diagram illustrating a multilevel power convertor in Embodiment 14

Fig. 27 is a circuit configuration diagram illustrating an example of a multilevel power convertor of the related art.

Fig. 28 is an explanatory diagram explaining an output voltage which cannot be output by the multilevel power convertor of the related art.

Fig. 29 shows circuit configuration diagrams illustrating other examples of multilevel power convertors of the related art.

Description of Embodiments

[0026]

[Basic Cell]

Fig. 1 is a circuit diagram illustrating a basic cell used in a multilevel power convertor according to the present invention. The basic cell is configured by six semiconductor elements SN.1 to SN.6 (for example, a module formed by a semiconductor switching element such as IGBT and a diode which is connected in reversely parallel to the semiconductor switching element; this is the same in the following description).

10 [0027]

More specifically, as illustrated in Fig. 1, a terminal 3 is connected to a positive electrode side of a DC voltage source (a DC capacitor or a DC power source), and a terminal 1 is connected to a negative electrode side of the DC voltage source. In addition, a terminal 2' is connected to a positive electrode side of a flying capacitor (or the DC voltage source), and a terminal 2'' is connected to a negative electrode side of the flying capacitor.

20 [0028]

The semiconductor elements SN.1 to SN.4 are sequentially connected in series between the terminal 3 and the terminal 1. In addition, a semiconductor element SN.5 is inserted between the terminal 2' and a common connection point of the semiconductor elements SN.1 and SN.2. A semiconductor element SN.6 is inserted between the terminal 2'' and a common connection point of the semiconductor elements SN.3 and SN.4. Here, a common connection point of the semiconductor elements SN.2 and SN.3 is the terminal 2.

[0029]

[Basic Circuit]

Fig. 2 illustrates a basic circuit in which  $N$  basic cells illustrated in Fig. 1 are connected in series to each other. Here,  $N$  is equal to or greater than 2 ( $N \geq 2$ ).

[0030]

A DC voltage source is connected between terminal numbers  $2N+1$  and  $2N-1$ . A flying capacitor is connected between terminal numbers  $2N'$  and  $2N''$ . Here, when a voltage of the DC voltage source is  $2E$  and a voltage of each flying capacitor is  $E$ , in a configuration in which the basic cells of  $N$  stages are connected in series to each other, a terminal  $2n$  can output voltages of " $2En$ ,  $2En-E$ , or  $2En-2E$ " (where  $n = 1$  to  $N$ ).

[0031]

By connecting a voltage selection circuit for selecting a voltage to each of the terminal  $2N$ , the terminal  $2(N-1)$ , ... and the terminal  $2$ , a  $(2N+1)$ -level power convertor can be achieved.

[0032]

[Voltage Selection Circuit]

Next, the voltage selection circuit will be explained with reference to Fig. 3. The voltage selection circuit is a circuit that has input terminals corresponding to the terminals  $(2, \dots, \text{and } 2N)$  of the basic circuit and selects one of potentials of the input terminals as an output potential which is outputted from an output terminal. The voltage selection circuit is configured by a configuration illustrated in Figs. 3(a), 3(b), 3(c) or

3(d), or a combination thereof. Semiconductor elements S1 to S28 are provided between each input terminal and the output terminal. By selectively turning on the semiconductor elements S1 to S28, a potential of one of the input terminals (in Fig. 3(a),  $2N_3$ ,  $2(N-1)_3$ ,  $4_3$ , and  $2_3$ , in Fig. 3(b),  $2N_3$ ,  $2(N-1)_3$ ,  $3_3$ , and  $2_3$ , in Fig. 3(c),  $4_3$ ,  $3_3$ ,  $2_3$ , and in Fig. 3(d),  $4N+1_3$ ,  $4N-1_3$ ,  $4N-3_3$ ,  $5_3$ ,  $3_3$ , and  $2_3$ ) can be outputted.

[0033]

10 [Embodiment 1]

Fig. 4 is a schematic diagram illustrating a configuration of a multilevel power convertor in Embodiment 1. As illustrated in Fig. 4, the multilevel power convertor in Embodiment 1 is an M-phase and N-stage multilevel power convertor configured using the basic circuit illustrated in Fig. 2 and the voltage selection circuit illustrated in Fig. 3. Here,  $N \geq 2$ , and  $M \geq 3$ .

[0034]

20 Each of phase modules 11 to 1M is configured by a combination of the basic circuit and the voltage selection circuit. Configurations of the basic circuit and the voltage selection circuit are the same as those illustrated in Figs. 2 and 3, and thus description thereof will be omitted here. N DC voltage sources DCC1 to DCCN are connected in series between both end terminals 1 and  $2N+1$  of the phase modules 11 to 1M. Common connection points of the DC voltage sources DCC1 to DCCN are respectively connected to terminals 3, ..., and  $2N-1$  of the phase modules 11 to 1M (the basic circuits). In addition,

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$N$  flying capacitors  $FC1$  to  $FCN$  are respectively connected to terminals  $2''$ ,  $2'$ , ...,  $2N''$  and  $2N'$  of the phase modules  $11$  to  $1M$ .

[0035]

5           Here, when a voltage of each of the DC voltage sources  $DCC1$  to  $DCCN$  is  $2E$  and each voltage of the flying capacitors  $FC1$  to  $FCN$  is controlled to  $E$ , it is possible to output voltages of  $(2p-2)E$  and  $(2p-1)E$  from a terminal  $2p''$  (where  $p = 1, 2, \dots$ , and  $N$ ). Further, it is possible to output  
10           voltages of  $(2p-1)E$  and  $2pE$  from a terminal  $2p'$ . In addition, a voltage of  $(2p-2)E$  can be outputted from a terminal  $2p-1$ , and a voltage of  $2pE$  can be outputted from a terminal  $2p+1$ .

[0036]

15           Next, potentials of the terminals  $1$ ,  $2''$ ,  $2'$ , and  $3, \dots$ , and  $2N-1$ ,  $2N''$ ,  $2N'$  and  $2N+1$  are inputted to the phase modules  $11$  to  $1M$ . Then, in the basic circuit, by selectively turning on the semiconductor elements  $S1.1$ ,  $S1.2$ ,  $S1.3$ , and  $S1.4$  to  $SN.1$ ,  $SN.2$ ,  $SN.3$  and  $SN.4$  for  
20           the each stage, one of the potentials of the terminals  $1$ ,  $2''$ ,  $2'$ , and  $3, \dots$ , and  $2N-1$ ,  $2N''$ ,  $2N'$  and  $2N+1$  is outputted from each of the terminals  $2, \dots$ , and  $2N$ . Further, by selectively turning on the semiconductor elements of the basic circuit of each stage by the voltage selection  
25           circuit, one of the potentials of the terminals  $2, \dots$ , and  $2N$  is outputted from each of output terminals  $OUT1$  to  $OUTM$ . As a result, voltages of  $(2N+1)$  levels can be output from the output terminals  $OUT1$  to  $OUTM$ .

[0037]

As described above, according to Embodiment 1, operations and effects of the following (1) and (2) are achieved and obtained.

[0038]

5       (1) When compared with the circuit configuration of the related art illustrated in Fig. 27, an arbitrary phase voltage level can be output, and control for outputting the arbitrary phase voltage level is facilitated.

10       [0039]

      (2) Unlike the circuit configuration of the related art illustrated in Figs. 29(a) and 29(b), there is no semiconductor element through which three-phase output currents of the U phase, the V phase, and the W phase flow then which has high power loss, it is possible to achieve size reduction of a cooling fin for cooling the semiconductor element.

[0040]

[Embodiment 2]

20       Next, a multilevel power convertor in Embodiment 2 will be explained with reference to Fig. 5. The multilevel power convertor in Embodiment 2 has a configuration where a circuit in which the first semiconductor elements S2.1 to SN.1 are in common to M phases and the fifth semiconductor elements S2.5 to SN.5 are omitted (removed) in the basic cells in the even-numbered stages of the basic circuit illustrated in Fig. 2 and a circuit in which fourth semiconductor elements S1.4 to SN-1.4 are in common to the M phases and the sixth semiconductor elements S1.6 to SN-1.6 are

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omitted (removed) in the basic cells in the odd-numbered stages of the basic circuit are connected to each other in N stages. Here, the multilevel power convertor in Embodiment 2 is an M-phase and N-stage multilevel power convertor. N is an even number of 2 or greater, and M  $\geq$  3. Other configurations are the same as those in Embodiment 1.

[0041]

In the configuration of Embodiment 2, it is possible to output voltages with (2N+1) levels from the output terminals OUT1 to OUTM. According to the multilevel power convertor in Embodiment 2, when compared with the circuit configuration of the related art illustrated in Fig. 27, an arbitrary phase voltage level can be output, and control for outputting the arbitrary phase voltage level is facilitated. In addition, when compared with Embodiment 1, the number of semiconductor elements can be reduced.

[0042]

[Embodiment 3]

Next, a multilevel power convertor in Embodiment 3 will be explained with reference to Fig. 6. The multilevel power convertor in Embodiment 3 has a configuration where a circuit in which fourth semiconductor elements S2.4 to SN.4 are in common to M phases and the sixth semiconductor elements S2.6 to SN.6 are omitted in the basic cells in the odd-numbered stages of the basic circuit illustrated in Fig. 2 and a circuit in which the first semiconductor elements S1.1 to SN-1.1 are in common to M phases and the fifth semiconductor elements S1.5 to SN-1.5 are omitted in the basic cells

in the even-numbered stages of the basic circuit are connected to each other in  $N$  stages. Here, the multilevel power convertor in Embodiment 3 is an  $M$ -phase and  $N$ -stage multilevel power convertor.  $N$  is an even number of 2 or greater, and  $M \geq 3$ . Other configurations are the same as those in Embodiment 1.

[0043]

In the configuration of Embodiment 3, it is possible to output voltages with  $(2N+1)$  levels from the output terminals OUT1 to OUTM.

[0044]

According to the multilevel power convertor in Embodiment 3, the same operations and the effects as in Embodiment 2 are achieved and obtained.

15 [0045]

[Embodiment 4]

Next, a multilevel power convertor in Embodiment 4 will be explained with reference to Fig. 7. In Embodiment 4, the first semiconductor elements S2.1 to SN.1 of the basic cells in the even-numbered stages which are in common to  $M$  phases, and the fourth semiconductor elements S1.4 to SN-1.4 of the basic cells in the odd-numbered stages which are in common to the  $M$  phases, are omitted (removed) in the multilevel power convertor of Embodiment 2. That is, in Fig. 7, the semiconductor elements connected to the terminals 1, 5,  $2N-3$  and  $2N+1$ , are omitted (removed). Other configurations are the same as those in Embodiment 2. Here,  $N$  is an even number of 2 or greater, and  $M \geq 3$ .

30 [0046]

In the configuration related to Embodiment 4, it is possible to output voltages with  $(2N+1)$  levels from the output terminals OUT1 to OUTM.

[0047]

5 According to the multilevel power convertor in Embodiment 4, when compared with the circuit configuration of the related art illustrated in Fig. 27, an arbitrary phase voltage level can be output, and control for outputting the arbitrary phase voltage level is  
10 facilitated.

[0048]

Unlike the circuit configuration of the related art illustrated in Figs. 29(a) and 29(b), there is no semiconductor element through which three-phase output  
15 currents of the U phase, the V phase, and the W phase flow then which has high power loss, it is possible to achieve size reduction of a cooling fin for cooling the semiconductor element.

[0049]

20 In addition, when compared with Embodiment 2, the number of semiconductor elements can be reduced.

[0050]

[Embodiment 5]

Next, a multilevel power convertor in Embodiment  
25 5 will be explained with reference to Fig. 8. In Embodiment 5, the fourth semiconductor elements S2.4 to SN.4 of the basic cells in the even-numbered stages which are in common to M phases, and the first semiconductor elements S1.1 to SN-1.1 of the basic cells in the odd-numbered stages  
30 which are in common to the M phases, are omitted (removed)

in the multilevel power convertor of Embodiment 3. That is, in Fig. 8, the semiconductor elements connected to the terminals 3 and  $2N-1$  are omitted (removed). Other configurations are the same as those in Embodiment 3.

5 Here,  $N$  is an even number of 2 or greater, and  $M \geq 3$ .

[0051]

In the configuration related to Embodiment 5, it is possible to output voltages with  $(2N+1)$  levels from the output terminals OUT1 to OUTM.

10 [0052]

According to the multilevel power convertor in Embodiment 5, when compared with the circuit configuration of the related art illustrated in Fig. 27, an arbitrary phase voltage level can be output, and control for outputting the arbitrary phase voltage level is facilitated.

[0053]

Unlike the circuit configuration of the related art illustrated in Figs. 29(a) and 29(b), there is no semiconductor element through which three-phase output currents of the U phase, the V phase, and the W phase flow then which has high power loss, it is possible to achieve size reduction of a cooling fin for cooling the semiconductor element.

25 [0054]

In addition, when compared with Embodiment 3, the number of semiconductor elements can be reduced.

[0055]

[Embodiment 6]

Fig. 9 illustrates a basic cell obtained in a case where  $N=1$  and  $M=3$  in Embodiment 1. The basic cell is configured by a DC voltage source DCC1, a flying capacitor FC1, semiconductor elements SUN.1 to SUN.6 of a U phase, a semiconductor elements SVN.1 to SVN.6 of a V phase, and a semiconductor elements SWN.1 to SWN.6 of a W phase.

[0056]

By connecting the basic cells in series to each other in two stages ( $N=2$  and  $M=3$  in Embodiment 1), a 5-level power convertor illustrated in Fig. 10 can be configured. Here, as the voltage selection circuit, Fig. 3(a) is used.

[0057]

In this case, voltage of each of the DC voltage sources DCC1 and DCC2 is  $2E$ , and voltage of each of the flying capacitors FC1 and FC2 is  $E$ . Further, a basic circuit of a U phase includes first to fourth semiconductor elements SU1.1 to SU1.4 and SU2.1 to SU2.4 which are sequentially connected in series between positive and negative terminals of the two DC voltage sources DCC1 and DCC2, fifth semiconductor elements SU1.5 and SU2.5 whose one ends are respectively connected to each of common connection points of the first and second semiconductor elements SU1.1, SU1.2, SU2.1, and SU2.2, and sixth semiconductor elements SU1.6 and SU2.6 whose one ends are respectively connected to common connection points of the third and fourth semiconductor elements SU1.3, SU1.4, SU2.3 and SU2.4. This is also the same for a V phase and a W phase.

[0058]

The flying capacitors FC1 and FC2 are inserted between the other ends of the fifth semiconductor elements SU1.5, SV1.5, SW1.5, SU2.5, SV2.5, SW2.5 and the other ends of sixth semiconductor elements SU1.6, SV1.6, SW1.6,  
5 SU2.6, SV2.6, SW2.6.

[0059]

A voltage selection circuit of the U phase is configured by SU1 to SU4. This is also the same for the V phase and the W phase.

10 [0060]

Here, the reference signs U, V and W indicate output terminals. As a modification example of the configuration illustrated in Fig. 10, it includes a circuit in which two or more semiconductor elements are  
15 connected in series to each other for resistance to a high voltage, and includes a circuit in which two or more semiconductor elements are connected parallel to each other for resistance to a large current.

[0061]

20 In addition, if a withstand voltage of the semiconductor element is appropriate, the semiconductor elements SU1 and SU2 illustrated in Fig. 10 which are two semiconductor elements connected in series to each other may be replaced with a single semiconductor element.  
25 Further, this is also the same for the semiconductor elements SV1 and SV2, SW1 and SW2, SU3 and SU4, SV3 and SV4, and SW3 and SW4.

[0062]

In the circuit, the flying capacitors FC1 and FC2 are in common to three phases, and thus phase voltages with five levels can be output.

[0063]

5 A representative switching pattern example of the U phase is illustrated in Table 1. By switching the semiconductor elements in the pattern illustrated in Table 1, five-level voltages of  $2E$ ,  $E$ ,  $0$ ,  $-E$  and  $-2E$  can be output in paths illustrated in Fig. 11. Here, Table 1  
10 and Fig. 11 are only examples, and other patterns could be used.

[0064]

[Table 1]

| SU2.1 | SU2.2 | SU1 | SU2 | SU3 | SU4 | SU1.3 | SU1.4 | SU2.3 | SU2.4 | SU1.1 | SU1.2 | SU2.5 | SU2.6 | SU1.5 | SU1.6 | $v_{ou}$ |
|-------|-------|-----|-----|-----|-----|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|----------|
| ON    | ON    | ON  | ON  | OFF | OFF | OFF   | OFF   | OFF   | OFF   | OFF   | OFF   | OFF   | OFF   | OFF   | OFF   | $2E$     |
| OFF   | ON    | ON  | ON  | OFF | OFF | OFF   | OFF   | OFF   | ON    | OFF   | OFF   | ON    | ON    | OFF   | OFF   | $E$      |
| OFF   | OFF   | ON  | ON  | OFF | OFF | OFF   | OFF   | ON    | ON    | OFF   | OFF   | OFF   | OFF   | OFF   | OFF   | $0$      |
| OFF   | OFF   | OFF | OFF | ON  | ON  | ON    | OFF   | OFF   | OFF   | ON    | OFF   | OFF   | OFF   | ON    | ON    | $-E$     |
| OFF   | OFF   | OFF | OFF | ON  | ON  | ON    | ON    | OFF   | OFF   | OFF   | OFF   | OFF   | OFF   | OFF   | OFF   | $-2E$    |

15 [0065]

Fig. 12 illustrates an operation of each semiconductor element in a case where the output terminal U outputs voltage of  $2E$ , the output terminal V outputs voltage of  $0$ , and the output terminal W outputs voltage of  $-2E$ . A circular mark in Fig. 12 indicates a turned-on  
20 semiconductor element.

[0066]

Even in a case where the operation is performed in the above-described switching state, by connecting the  
25 semiconductor elements SU1.5, SV1.5, SW1.5, SU1.6, SV1.6 and SW1.6 to both ends of the flying capacitor FC1, and by connecting the semiconductor elements SU2.5, SV2.5,

SW2.5, SU2.6, SV2.6 and SW2.6 to both ends of the flying capacitor FC2, the operation can be performed without short-circuit of each of the flying capacitors FC1 and FC2.

5 [0067]

Hence, it is possible to output a combination of phase voltages of  $2E$ ,  $0$  and  $-2E$  which cannot be outputted in the circuit configuration illustrated in Fig. 27, and also to simplify control for outputting the voltages of  $2E$ ,  $0$  and  $-2E$ .

[0068]

Next, a withstand voltage of the semiconductor element during operation in the circuit illustrated in Fig. 12 will be explained.

15 [0069]

As an example, a case where voltage of  $2E$  is output in the U phase, voltage of  $0$  is output in the V phase, and voltage of  $-2E$  is output in the W phase will be explained. In this case, as a condition, impedances of the semiconductor elements SW2.1, SW2.2, SW1 and SW2 in OFF states are equal to each other.

[0070]

In this case, a potential of a collector terminal of the semiconductor element SW2.1 is  $2E$  and a potential of the output terminal W (i.e. a potential of an emitter terminal of the semiconductor element SW2) is  $-2E$ , and a voltage is divided by the impedances of the semiconductor elements SW2.1, SW2.2, SW1 and SW2, and thus a potential of the common connection point of the semiconductor elements SW2.2 and SW1 becomes  $0$ . Therefore, a voltage

applied to the series connection circuit of the semiconductor elements SW1 and SW2 is  $2E$ . Here, a reference point of each potential is a terminal 0 illustrated in Fig. 10. This condition is a condition  
5 in which a voltage applied to the series circuits of the semiconductor elements SW2.1, SW2.2, SW1 and SW2 becomes the maximum ( $4E$ ).

[0071]

Therefore, in the circuit illustrated in Fig. 10,  
10 the maximum value of a voltage applied to the series connection circuit of the semiconductor elements SW1 and SW2 in a steady state is  $2E$ . This is also the same for the semiconductor elements SU1 and SU2, SV1 and SV2, SU3 and SU4, SV3 and SV4, and SW3 and SW4.

15 [0072]

On the other hand, in the circuit of the related art illustrated in Fig. 29(a), there is a mode in which voltage of the terminal W0 becomes  $E$  and voltage of the output terminal OUT\_W becomes  $-2E$  according to on/off  
20 states of the switching element. In this case, a voltage of  $3E$  is applied to the switching element SW5.

[0073]

In the circuit of the related art illustrated in Fig. 29(b), there is a mode in which a voltage of the  
25 terminal W0 becomes  $E$ , and a voltage of the output terminal OUT\_W becomes  $-2E$  according to on/off states of the switching element. In this case, a voltage of  $3E$  is applied to the switching element SW5.

[0074]

From the above description, when compared with the related art circuit of Figs. 29(a) and 29(b), Embodiment 6 has advantage of lowering a required withstand voltage of the semiconductor element that is directly connected  
5 to the output terminal.

[0075]

In addition, unlike the circuit configuration of the related art illustrated in Figs. 29(a) and 29(b), in the case of Embodiment 6, there is no semiconductor  
10 element through which currents of three phases of the U phase, the V phase and the W phase flow. Thus, a cooling fin with a high cooling effect is not necessary.

[0076]

This is also advantageous in terms of cost or  
15 miniaturization of the device.

[0077]

Although the three-phase output circuit has been explained in Embodiment 6, also in a circuit in which the number of output phases is increased to four or more,  
20 phase voltages of respective phases can be outputted separately without short-circuit of each of the flying capacitors FC1 and FC2. The circuit is also advantageous in a withstand voltage of the semiconductor element and is advantageous in that there is no semiconductor element  
25 through which currents of three phases flow, when compared with the circuits of the related art illustrated in Figs. 29(a) and 29(b).

[0078]

[Embodiment 7]

Next, a multilevel power convertor in Embodiment 7 will be explained with reference to Fig. 13. A configuration of the multilevel power convertor in Embodiment 7 is a configuration in which  $N=2$  and  $M=3$  in the case of Embodiment 3, and the voltage selection circuit illustrated in Fig. 3(a) is used. Here, the reference signs U, V and W indicate output terminals.

[0079]

The basic circuit includes the fourth semiconductor element S2.4 whose one end is connected to a negative electrode end of the DC voltage source DCC2 in the even-numbered stage of the two serially connected DC voltage sources DCC1 and DCC2, and which is in common to three phases; the first to third semiconductor elements SU2.1 to SU2.3, SV2.1 to SV2.3, and SW2.1 to SW2.3 of the three phases which are sequentially connected in series between a positive electrode end of the DC voltage source DCC2 in the even-numbered stage and the other end of the fourth semiconductor element S2.4 in the even-numbered stage; the fifth semiconductor elements SU2.5, SV2.5 and SW2.5 whose one ends are respectively connected to common connection points of the first and second semiconductor elements SU2.1, SU2.2, SV2.1, SV2.2, SW2.1 and SW2.2 in the even-numbered stage; the first semiconductor element S1.1 whose one end is connected to the positive electrode end of the DC voltage source DCC1 in the odd-numbered stage and which is in common to three phases; the second to fourth semiconductor elements SU1.2 to SU1.4, SV1.2 to SV1.4, and SW1.2 to SW1.4 of the three phases which are sequentially connected

in series between the other end of the first semiconductor element S1.1 in the odd-numbered stage and the negative electrode end of the DC voltage source DCC1 in the odd-numbered stage; and the sixth semiconductor elements  
5 SU1.6, SV1.6 and SW1.6 whose one ends are respectively connected to common connection points of the third and fourth semiconductor elements SU1.3, SU1.4, SV1.3, SV1.4, SW1.3 and SW1.4 in the odd-numbered stage.

[0080]

10 The flying capacitor FC2 is inserted between all the fifth semiconductor elements SU2.5, SV2.5, SW2.5 and the common connection point of the third and fourth semiconductor elements SU2.3, SV2.3, SW2.3, SU2.4 in the even-numbered stage. The flying capacitor FC1 is  
15 inserted between the common connection point of the first and second semiconductor elements S1.1, SU1.2, SV1.2 and SW1.2 and all the sixth semiconductor elements SU1.6, SV1.6, SW1.6 in the odd-numbered stage.

[0081]

20 The voltage selection circuit is configured by semiconductor elements SU1 to SU4, SV1 to SV4, and SW1 to SW4.

[0082]

As a modification example of the configuration  
25 illustrated in Fig. 13, it also includes a circuit in which two or more semiconductor elements are connected in series to each other for resistance to a high voltage. In addition, it also includes a circuit in which two or more semiconductor elements are connected parallel to  
30 each other for resistance to a large current.

[0083]

In addition, if a withstand voltage of the semiconductor element is appropriate, the semiconductor elements SU1 and SU2 illustrated in Fig. 13 which are  
5 two semiconductor elements connected in series to each other may be replaced with a single semiconductor element. Further, this is also the same for the semiconductor elements SV1 and SV2, SW1 and SW2, SU3 and SU4, SV3 and SV4, and SW3 and SW4.

10 [0084]

Also in Embodiment 7, it is possible to output a combination of phase voltages of  $2E$ ,  $0$  and  $-2E$  which cannot be outputted in the circuit configuration illustrated in Fig. 27. Fig. 14 illustrates such a state. In Fig.  
15 14, the circular mark indicates a turned-on semiconductor element.

[0085]

Fig. 14 illustrates an operation of each semiconductor element in a case where the output terminal  
20 U outputs voltage of  $2E$ , the output terminal V outputs voltage of  $0$ , and the output terminal W outputs voltage of  $-2E$ . In this case, since the flying capacitor FC2 is connected to the semiconductor elements SU2.5, SV2.5 and SW2.5 and the flying capacitor FC1 is connected to the  
25 semiconductor elements SU1.6, SV1.6 and SW1.6, it is possible to output a combination of phase voltages of  $2E$ ,  $0$  and  $-2E$  without short-circuit of each of the flying capacitors FC1 and FC2, and also to simplify control for outputting the voltages of  $2E$ ,  $0$  and  $-2E$ .

30 [0086]

Also in Embodiment 7, in a condition in which impedances of the semiconductor elements SW2.1, SW2.2, SW1 and SW2 in OFF states are the same as each other, the maximum value of a voltage applied to the series connection circuit of the semiconductor elements SW1 and SW2 in a steady state is  $2E$  in the same manner as in Embodiment 6. This is also the same for the semiconductor elements SU1 and SU2, SV1 and SV2, SW1 and SW2, SU3 and SU4, SV3 and SV4, and SW3 and SW4.

10 [0087]

Although the three-phase output circuit has been explained in Embodiment 7, also in a circuit in which the number of output phases is increased to four or more, phase voltages of respective phases can be outputted separately without short-circuit of each of the flying capacitors FC1 and FC2. The circuit is also advantageous in a withstand voltage of the semiconductor element when compared with the circuits of the related art illustrated in Figs. 29(a) and 29(b).

20 [0088]

[Embodiment 8]

Fig. 15 is a circuit configuration diagram illustrating a multilevel power convertor in Embodiment 8. A configuration of the multilevel power convertor in Embodiment 8 is a configuration in which  $N=2$  and  $M=3$  and the voltage selection circuit illustrated in Fig. 3(a) is used in Embodiment 2. The reference signs U, V and W indicate output terminals.

[0089]

The basic circuit includes the first semiconductor element S2.1 whose one end is connected to a positive electrode end of the DC voltage source DCC2 in the even-numbered stage of the two serially connected DC voltage sources DCC1 and DCC2, and which is in common to three phases; second to fourth semiconductor elements SU2.2a to SU2.4, SV2.2a to SV2.4, and SW2.2a to SW2.4 of the three phases which are sequentially connected in series between the other end of the first semiconductor element S2.1 in the even-numbered stage and a negative electrode end of the DC voltage source DCC2 in the even-numbered stage; the sixth semiconductor elements SU2.6, SV2.6 and SW2.6 of the three phases whose one ends are respectively connected to common connection points of the third and fourth semiconductor elements SU2.3, SU2.4, SV2.3, SV2.4, SW2.3 and SW2.4; the fourth semiconductor element S1.4 whose one end is connected to a negative electrode end of the DC voltage source DCC1 in the odd-numbered stage and which is in common to the three phase; first to third semiconductor elements SU1.1 to SU1.3b, SV1.1 to SV1.3b, and SW1.1 to SW1.3b of the three phases which are sequentially connected in series between a positive electrode end of the DC voltage source DCC1 in the odd-numbered stage and the other end of the fourth semiconductor element S1.4 in the odd-numbered stage; and the fifth semiconductor elements SU1.5, SV1.5 and SW1.5 of the three phases whose one ends are respectively connected to common connection points of the first and second semiconductor elements SU1.1, SU1.2, SV1.1, SV1.2, SW1.1 and SW1.2 in the odd-numbered stage.

[0090]

The flying capacitor FC2 is inserted between the common connection points of the first and second semiconductor elements S2.1, SU2.2a, SV2.2a and SW2.2a in the even-numbered stage and the other ends of the sixth semiconductor elements SU2.6, SV2.6, SW2.6 of all the phases in the even-numbered stage. The flying capacitor FC1 is inserted between the other ends of the fifth semiconductor elements SU1.5, SV1.5, SW1.5 of all the phases in the odd-numbered stage and the common connection points of the third and fourth semiconductor elements SU1.3b, SV1.3b, SW1.3b and S1.4 in the odd-numbered stage.

[0091]

The voltage selection circuit is configured by the semiconductor elements SU1 to SU4, SV1 to SV4, and SW1 to SW4.

[0092]

Also in Embodiment 8, it is possible to output a combination of phase voltages of  $2E$ ,  $0$  and  $-2E$  which cannot be output in the circuit configuration illustrated in Fig. 27.

[0093]

Fig. 16 illustrates such a state. In Fig. 16, the circular mark indicates a turned-on semiconductor element. Fig. 16 illustrates an operation of each semiconductor element in a case where the output terminal U outputs voltage of  $2E$ , the output terminal V outputs voltage of  $0$ , and the output terminal W outputs voltage of  $-2E$ . In this case, since the flying capacitor FC1 is connected to the fifth semiconductor elements SU1.5, SV1.5 and SW1.5

and the flying capacitor FC2 is connected to the sixth semiconductor elements SU2.6, SV2.6 and SW2.6, it is possible to output a combination of phase voltages of 2E, 0 and -2E from the output terminals U, V and W without short-circuit of each of the flying capacitors FC1 and FC2, and also to simplify control for outputting the voltages of 2E, 0 and -2E.

[0094]

As a modification example of Embodiment 8, it also includes a circuit in which two or more semiconductor elements are connected in series to each other for resistance to a high voltage. In addition, it also includes a circuit in which two or more semiconductor elements are connected parallel to each other for resistance to a large current. Further, if a withstand voltage of the semiconductor element is appropriate, the semiconductor elements SU1.3a and SU1.3b illustrated in Fig. 15 which are two semiconductor elements connected in series to each other may be replaced with a single semiconductor element.

[0095]

Further, this is also the same for the semiconductor elements SV1.3a and SV1.3b, SW1.3a and SW1.3b, SU2.2a and SU2.2b, SV2.2a and SV2.2b, SW2.2a and SW2.2b, SU1 and SU2, SV1 and SV2, SW1 and SW2, SU3 and SU4, SV3 and SV4, and SW3 and SW4.

[0096]

Also in Embodiment 8, in a condition in which impedances of the semiconductor elements SW2.2a, SW2.2b, SW1 and SW2 in OFF states are the same as each other,

the maximum value of a voltage applied to the series connection circuit of the semiconductor elements SW1 and SW2 in a steady state is  $2E$  in the same manner as in Embodiment 6. This is also the same for the semiconductor  
5 elements SU1 and SU2, SV1 and SV2, SU3 and SU4, SV3 and SV4, and SW3 and SW4.

[0097]

Although the three-phase output circuit has been explained in Embodiment 8, also in a circuit in which  
10 the number of output phases is increased to four or more, phase voltages of respective phases can be outputted separately without short-circuit of each of the flying capacitors FC1 and FC2. The circuit is also advantageous in a withstand voltage of the semiconductor element when  
15 compared with the circuits of the related art illustrated in Figs. 29(a) and 29(b).

[0098]

[Embodiment 9]

Next, a multilevel power convertor in Embodiment  
20 9 will be explained with reference to Fig. 17. A configuration of the multilevel power convertor in Embodiment 9 is a configuration in which  $N=2$  and  $M=3$  in the case of Embodiment 4, and the voltage selection circuit illustrated in Fig. 3(a) is used. The reference signs  
25 U, V and W indicate output terminals.

[0099]

The basic circuit includes the second to fourth semiconductor elements SU2.2 to SU2.4, SV2.2 to SV2.4, and SW2.2 to SW2.4 which are sequentially connected in  
30 series to a positive electrode end of the DC voltage source

DCC2 in the even-numbered stage of the two serially connected DC voltage sources DCC1 and DCC2; and the third to first semiconductor elements SU1.3 to SU1.1, SV1.3 to SV1.1, and SW1.3 to SW1.1 which are sequentially  
 5 connected in series to a negative electrode end of the DC voltage source DCC1 in the odd-numbered stage of the two serially connected DC voltage sources DCC1 and DCC2.

[0100]

The flying capacitor FC1 is connected parallel to  
 10 the second and third semiconductor elements SU1.3, SU1.2, SV1.3, SV1.2, SW1.3 and SW1.2 in the odd-numbered stage. The flying capacitor FC2 is connected parallel to the second and third semiconductor elements SU2.2, SU2.3, SV2.2, SV2.3, SW2.2 and SW2.3 in the even-numbered stage.

15 [0101]

In addition, the fifth semiconductor elements SU1.5, SV1.5 and SW1.5 are inserted between the flying capacitor FC1 and the second semiconductor elements SU1.2, SV1.2, SW1.2 in the odd-numbered stage. The sixth semiconductor  
 20 elements SU2.6, SV2.6 and SW2.6 are inserted between the flying capacitor FC2 and the third semiconductor elements SU2.3, SV2.3, SW2.3 in the even-numbered stage.

[0102]

Further, the first semiconductor elements SU1.1, SV1.1 and SW1.1 are inserted between the second  
 25 semiconductor elements SU1.2, SV1.2, SW1.2 in the odd-numbered stage and the terminal 0. The fourth semiconductor elements SU2.4, SV2.4 and SW2.4 are inserted between the third semiconductor elements SU2.3, SV2.3, SW2.3 in the even-numbered stage and the terminal 0.  
 30

[0103]

The voltage selection circuit is configured by the semiconductor elements SU1, SU3, SV1, SV3, SW1 and SW3.

[0104]

5 By controlling each of voltages of the DC voltage sources DCC1 and DCC2 to  $2E$  and controlling each of voltages of the flying capacitors FC1 and FC2 to  $E$ , it is possible to output five-level voltages of  $2E$ ,  $E$ ,  $0$ ,  $-E$  and  $-2E$ .

[0105]

10 As a modification example of the configuration illustrated in Fig. 17, it also includes a circuit in which two or more semiconductor elements are connected in series to each other for resistance to a high voltage. In addition, it also includes a circuit in which two or  
15 more semiconductor elements are connected parallel to each other for resistance to a large current.

[0106]

Fig. 18 illustrates an operation of each semiconductor element in a case where the output terminal  
20 U outputs voltage of  $2E$ , the output terminal V outputs voltage of  $0$ , and the output terminal W outputs voltage of  $-2E$ . In Fig. 18, the circular mark indicates a turned-on semiconductor element. In this case, since the flying capacitor FC1 is connected to the semiconductor elements  
25 SU1.5, SV1.5 and SW1.5 and the flying capacitor FC2 is connected to the semiconductor elements SU2.6, SV2.6 and SW2.6, it is possible to output a combination of phase voltages of  $2E$ ,  $0$  and  $-2E$  from the output terminals U, V and W without short-circuit of each of the flying

capacitors FC1 and FC2, and also to simplify control for outputting the voltages of  $2E$ ,  $0$  and  $-2E$ .

[0107]

Also in Embodiment 9, in a condition in which  
5 impedances of the semiconductor elements SW2.2 and SW1  
in OFF states are the same as each other, the maximum  
value of a voltage applied to the semiconductor element  
SW1 in a steady state is  $2E$  in the same manner as in  
Embodiment 6. This is also the same for the semiconductor  
10 elements SU1, SV1, SU3, SV3 and SW3.

[0108]

In addition, unlike the circuit configuration of  
the related art illustrated in Figs. 29(a) and 29(b),  
in the case of Embodiment 9, there is no semiconductor  
15 element through which currents of three phases of the  
U phase, the V phase and the W phase flow. Thus, a cooling  
fin with a high cooling effect is not necessary.

[0109]

Although the three-phase output circuit has been  
20 explained in Embodiment 9, also in a circuit in which  
the number of output phases is increased to four or more,  
phase voltages of respective phases can be outputted  
separately without short-circuit of each of the flying  
capacitors FC1 and FC2. The circuit is also advantageous  
25 in a withstand voltage of the semiconductor element and  
is advantageous in that there is no semiconductor element  
through which currents of three phases flow, when compared  
with the circuits of the related art illustrated in Figs.  
29(a) and 29(b).

30 [0110]

[Embodiment 10]

Next, a multilevel power convertor in Embodiment 10 will be explained with reference to Fig. 19. A configuration of the multilevel power convertor in Embodiment 10 is a configuration in which  $N=2$  and  $M=3$  in the case of Embodiment 4. The reference signs U, V and W indicate output terminals. As the voltage selection circuit, Fig. 3(b) is used.

[0111]

10        The basic circuit includes the second and third semiconductor elements SU2.2, SU2.3, SV2.2, SV2.3, SW2.2 and SW2.3 which are sequentially connected in series to a positive electrode end of the DC voltage source DCC2 in the even-numbered stage of the two serially connected  
15        DC voltage sources DCC1 and DCC2; and the third and second semiconductor elements SU1.3, SU1.2, SV1.3, SV1.2, SW1.3 and SW1.2 which are sequentially connected in series to a negative electrode end of the DC voltage source DCC1 in the odd-numbered stage of the two serially connected  
20        DC voltage sources DCC1 and DCC2.

[0112]

      The flying capacitor FC1 is connected parallel to the second and third semiconductor elements SU1.2, SU1.3, SV1.2, SV1.3, SW1.2 and SW1.3 in the odd-numbered stage.  
25        The flying capacitor FC2 is connected parallel to the second and third semiconductor elements SU2.2, SU2.3, SV2.2, SV2.3, SW2.2 and SW2.3 in the even-numbered stage.

[0113]

The voltage selection circuit is configured by the semiconductor elements SU7, SU8, SU11, SU12, SV7, SV8, SV11, SV12, SW7, SW8, SW11 and SW12.

[0114]

5 By controlling each of voltages of the DC voltage sources DCC1 and DCC2 to  $2E$  and controlling each of voltages of the flying capacitors FC1 and FC2 to  $E$ , it is possible to output five-level voltages of  $2E$ ,  $E$ ,  $0$ ,  $-E$  and  $-2E$ .

[0115]

10 As a modification example of the configuration illustrated in Fig. 19, it also includes a circuit in which two or more semiconductor elements are connected in series to each other for resistance to a high voltage. In addition, it also includes a circuit in which two or  
15 more semiconductor elements are connected parallel to each other for resistance to a large current.

[0116]

Fig. 20 illustrates an operation of each semiconductor element in a case where the output terminal  
20 U outputs voltage of  $2E$ , the output terminal V outputs voltage of  $0$ , and the output terminal W outputs voltage of  $-2E$ . In Fig. 20, the circular mark indicates a turned-on semiconductor element. In this case, since the negative electrode side of the flying capacitor FC2 is not connected  
25 to the negative electrode side of the DC voltage source DCC2 and the positive electrode side of the flying capacitor FC1 is not connected to the DC voltage source DCC1, it is possible to output a combination of phase voltages of  $2E$ ,  $0$  and  $-2E$  from the output terminals U,  
30 V and W without short-circuit of each of the flying

capacitors FC1 and FC2, and also to simplify control for outputting the voltages of  $2E$ ,  $0$  and  $-2E$ .

[0117]

In addition, unlike the circuit configuration of the related art illustrated in Figs. 29(a) and 29(b), in the case of Embodiment 10, there is no semiconductor element through which currents of three phases of the U phase, the V phase and the W phase flow. Thus, a cooling fin with a high cooling effect is not necessary.

10 [0118]

Although the three-phase output circuit has been explained in Embodiment 10, also in a circuit in which the number of output phases is increased to four or more, phase voltages of respective phases can be outputted separately without short-circuit of each of the flying capacitors FC1 and FC2. The circuit is also advantageous in a withstand voltage of the semiconductor element and is advantageous in that there is no semiconductor element through which currents of three phases flow, when compared with the circuits of the related art illustrated in Figs. 29(a) and 29(b).

[0119]

[Embodiment 11]

Next, a multilevel power convertor in Embodiment 11 will be explained with reference to Fig. 21. A configuration of the multilevel power convertor in Embodiment 11 is a configuration in which  $N=2$  and  $M=3$  in the case of Embodiment 4. As the voltage selection circuit, Fig. 3(c) is used.

30 [0120]

The basic circuit includes the second and third semiconductor elements SU2.2, SU2.3, SV2.2, SV2.3, SW2.2 and SW2.3 which are sequentially connected in series to a positive electrode end of the DC voltage source DCC2  
5 in the even-numbered stage of the two serially connected DC voltage sources DCC1 and DCC2; and the third and second semiconductor elements SU1.3, SU1.2, SV1.3, SV1.2, SW1.3 and SW1.2 which are sequentially connected in series to a negative electrode end of the DC voltage source DCC1  
10 in the odd-numbered stage of the two serially connected DC voltage sources DCC1 and DCC2.

[0121]

The flying capacitor FC1 is connected parallel to the second and third semiconductor elements SU1.2, SU1.3, SV1.2, SV1.3, SW1.2 and SW1.3 in the odd-numbered stage.  
15 The flying capacitor FC2 is connected parallel to the second and third semiconductor elements SU2.2, SU2.3, SV2.2, SV2.3, SW2.2 and SW2.3 in the even-numbered stage.

[0122]

20 The voltage selection circuit is configured by diodes DU1, DU2, DV1, DV2, DW1 and DW2, and the semiconductor elements SU12 to SU15, SV12 to SV15, and SW12 to SW15.

[0123]

By controlling each of voltages of the DC voltage sources DCC1 and DCC2 to  $2E$  and controlling each of voltages  
25 of the flying capacitors FC1 and FC2 to  $E$ , it is possible to output five-level voltages of  $2E$ ,  $E$ ,  $0$ ,  $-E$  and  $-2E$  from the output terminals U, V and W.

[0124]

As a modification example of the configuration illustrated in Fig. 21, it also includes a circuit in which two or more semiconductor elements are connected in series to each other for resistance to a high voltage.

5 In addition, is also includes a circuit in which two or more semiconductor elements are connected parallel to each other for resistance to a large current.

[0125]

Fig. 22 illustrates an operation of each  
10 semiconductor element in a case where the output terminal U outputs voltage of  $2E$ , the output terminal V outputs voltage of  $0$ , and the output terminal W outputs voltage of  $-2E$ . In Fig. 22, the circular mark indicates a turned-on semiconductor element. In this case, since the negative  
15 electrode side of the flying capacitor FC2 is not connected to the negative electrode side of the DC voltage source DCC2 and the positive electrode side of the flying capacitor FC1 is not connected to the positive side of the DC voltage source DCC1, it is possible to output a  
20 combination of phase voltages of  $2E$ ,  $0$  and  $-2E$  from the output terminals U, V and W respectively, without short-circuit of each of the flying capacitors FC1 and FC2, and also to simplify control for outputting the voltages of  $2E$ ,  $0$  and  $-2E$ .

25 [0126]

In addition, unlike the circuit configuration of the related art illustrated in Figs. 29(a) and 29(b), in the case of Embodiment 11, there is no semiconductor element through which currents of three phases of the

U phase, the V phase and the W phase flow. Thus, a cooling fin with a high cooling effect is not necessary.

[0127]

Although the three-phase output circuit has been  
5 explained in Embodiment 11, also in a circuit in which  
the number of output phases is increased to four or more,  
phase voltages of respective phases can be outputted  
separately without short-circuit of each of the flying  
capacitors FC1 and FC2. The circuit is also advantageous  
10 in a withstand voltage of the semiconductor element and  
is advantageous in that there is no semiconductor element  
through which currents of three phases flow, when compared  
with the circuits of the related art illustrated in Figs.  
29(a) and 29(b).

15 [0128]

[Embodiment 12]

Next, a multilevel power convertor in Embodiment  
12 will be explained with reference to Fig. 23. A  
configuration of the multilevel power convertor in  
20 Embodiment 12 is a configuration in which  $N=2$  and  $M=3$   
in the case of Embodiment 5. As the voltage selection  
circuit, Fig. 3(c) is used.

[0129]

The basic circuit includes the first to third  
25 semiconductor elements SU2.1 to SU2.3, SV2.1 to SV2.3,  
and SW2.1 to SW2.3 which are sequentially connected in  
series between positive and negative electrode ends of  
the DC voltage source DCC2 in the even-numbered stage  
of the two serially connected DC voltage sources DCC1  
30 and DCC2; the fifth semiconductor elements SU2.5, SV2.5

and SW2.5 whose one ends are connected to common connection points of the first and second semiconductor elements SU2.1, SU2.2, SV2.1, SV2.2, SW2.1 and SW2.2 in the even-numbered stage; the second to fourth semiconductor elements SU1.2 to SU1.4, SV1.2 to SV1.4, and SW1.2 to SW1.4 which are sequentially connected in series between positive and negative electrode ends of the DC voltage source DCC1 in the odd-numbered stage of the two serially connected DC voltage sources DCC1 and DCC2; and the sixth semiconductor elements SU1.6, SV1.6 and SW1.6 whose one ends are connected to common connection points of the third and fourth semiconductor elements SU1.3, SU1.4, SV1.3, SV1.4, SW1.3 and SW1.4 in the odd-numbered stage.

[0130]

The flying capacitor FC2 is inserted between the other ends of all the fifth semiconductor elements SU2.5, SV2.5, SW2.5 in the even-numbered stage and the common connection point of the negative electrode end of the DC voltage source DCC2 in the even-numbered stage and the third semiconductor elements SU2.3, SV2.3, SW2.3. The flying capacitor FC1 is inserted between the other ends of the sixth semiconductor elements SU1.6, SV1.6, SW1.6 in the odd-numbered stage and the common connection point of the positive electrode end of the DC voltage source DCC1 in the odd-numbered stage and the second semiconductor elements SU1.2, SV1.2, SW1.2.

[0131]

The voltage selection circuit is configured by the semiconductor elements SU14, SU15, SV14, SV15, SW14 and SW15.

[0132]

By controlling each of voltages of the DC voltage sources DCC1 and DCC2 to  $2E$  and controlling each of voltages of the flying capacitors FC1 and FC2 to  $E$ , it is possible  
5 to output five-level voltages of  $2E$ ,  $E$ ,  $0$ ,  $-E$  and  $-2E$  from the output terminals U, V and W.

[0133]

As a modification example of the configuration illustrated in Fig. 23, it also includes a circuit in  
10 which two or more semiconductor elements are connected in series to each other for resistance to a high voltage. In addition, it also includes a circuit in which two or more semiconductor elements are connected parallel to each other for resistance to a large current.

15 [0134]

Fig. 24 illustrates an operation of each semiconductor element in a case where the output terminal U outputs voltage of  $2E$ , the output terminal V outputs voltage of  $0$ , and the output terminal W outputs voltage of  $-2E$ . In Fig. 24, the circular mark indicates a turned-on  
20 semiconductor element.

[0135]

In this case, since the flying capacitor FC1 is connected to the sixth semiconductor elements SU1.6, SV1.6,  
25 and SW1.6 and the flying capacitor FC2 is connected to the fifth semiconductor elements SU2.5, SV2.5 and SW2.5, it is possible to output a combination of phase voltages of  $2E$ ,  $0$  and  $-2E$  from the output terminals U, V and W respectively, without short-circuit of each of the flying

capacitors FC1 and FC2, and also to simplify control for outputting the voltages of  $2E$ ,  $0$  and  $-2E$ .

[0136]

In addition, unlike the circuit configuration of the related art illustrated in Figs. 29(a) and 29(b), in the case of Embodiment 12, there is no semiconductor element through which currents of three phases of the U phase, the V phase and the W phase flow. Thus, a cooling fin with a high cooling effect is not necessary.

10 [0137]

Although the three-phase output circuit has been explained in Embodiment 12, also in a circuit in which the number of output phases is increased to four or more, phase voltages of respective phases can be outputted separately without short-circuit of each of the flying capacitors FC1 and FC2. The circuit is also advantageous in a withstand voltage of the semiconductor element and is advantageous in that there is no semiconductor element through which currents of three phases flow, when compared with the circuits of the related art illustrated in Figs. 29(a) and 29(b).

[0138]

[Embodiment 13]

Next, a multilevel power convertor in Embodiment 13 will be explained with reference to Fig. 25. A configuration of the multilevel power convertor in Embodiment 13 is a configuration in which  $N=4$  and  $M=3$  in the case of Embodiment 4. As the voltage selection circuit, Figs. 3(a) and 3(d) are used.

30 [0139]

The basic circuit includes the second and third semiconductor elements SU2.2, SU2.3, SV2.2, SV2.3, SW2.2, SW2.3, SU4.2, SU4.3, SV4.2, SV4.3, SW4.2 and SW4.3 which are sequentially connected in series to positive electrode ends of the DC voltage sources DCC2 and DCC4 in the even-numbered stages among four serially connected DC voltage sources DCC1 to DCC4; and the third and second semiconductor elements SU1.3, SU1.2, SV1.3, SV1.2, SW1.3, SW1.2, SU3.3, SU3.2, SV3.3, SV3.2, SW3.3 and SW3.2 which are sequentially connected in series to negative electrode ends of the DC voltage sources DCC1 and DCC3 in the odd-numbered stages among the four serially connected DC voltage sources DCC1 to DCC4.

[0140]

The flying capacitors FC1 to FC4 are connected parallel to the second and third semiconductor elements SU2.2, SU2.3, SV2.2, SV2.3, SW2.2, SW2.3, SU4.2, SU4.3, SV4.2, SV4.3, SW4.2, SW4.3, SU1.3, SU1.2, SV1.3, SV1.2, SW1.3, SW1.2, SU3.3, SU3.2, SV3.3, SV3.2, SW3.3 and SW3.2 in the odd-numbered stages and the even-numbered stages.

[0141]

The voltage selection circuits are configured by semiconductor elements SU19 to SU28, SV19 to SV28, and SW19 to SW28.

[0142]

By controlling each of voltages of the DC voltage sources DCC1, DCC2, DCC3, and DCC4 to 2E and controlling each of voltages of the flying capacitors FC1, FC2, FC3, and FC4 to E, it is possible to output nine-level voltages of 4E, 3E, 2E, E, 0, -E, -2E, -3E and -4E.

[0143]

Table 2 shows voltages between the terminal U and the terminal 0 in ON/OFF states of each semiconductor element in the U phase.

5

[0144]

[Table 2]

| SU43 | SU19 | SU20 | SU27 | SU28 | SU25 | SU26 | SU42 | SU21 | SU22 | SU23 | SU24 | SU17 | SU22 | SU23 | SU23 | SU18 | SU12 | SU13 | U   |
|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|-----|
| ON   | ON   | ON   | ON   | OFF  | OFF  | OFF  | OFF  | OFF  | OFF  | OFF  | OFF  | OFF  | OFF  | OFF  | OFF  | OFF  | OFF  | OFF  | 4E  |
| OFF  | ON   | ON   | ON   | OFF  | OFF  | OFF  | ON   | OFF  | OFF  | OFF  | OFF  | OFF  | OFF  | OFF  | OFF  | OFF  | OFF  | OFF  | 3E  |
| OFF  | OFF  | ON   | ON   | OFF  | OFF  | OFF  | OFF  | OFF  | OFF  | OFF  | ON   | OFF  | OFF  | OFF  | OFF  | OFF  | OFF  | OFF  | 2E  |
| OFF  | OFF  | OFF  | ON   | OFF  | OFF  | OFF  | OFF  | ON   | ON   | OFF  | OFF  | OFF  | ON   | OFF  | OFF  | OFF  | OFF  | OFF  | E   |
| OFF  | OFF  | OFF  | ON   | OFF  | OFF  | OFF  | OFF  | ON   | ON   | OFF  | OFF  | OFF  | ON   | OFF  | ON   | OFF  | OFF  | OFF  | 0   |
| OFF  | OFF  | OFF  | OFF  | ON   | OFF  | OFF  | OFF  | OFF  | OFF  | ON   | ON   | OFF  | OFF  | OFF  | OFF  | ON   | OFF  | OFF  | -E  |
| OFF  | OFF  | OFF  | OFF  | ON   | ON   | OFF  | OFF  | OFF  | OFF  | OFF  | OFF  | OFF  | OFF  | OFF  | OFF  | ON   | OFF  | OFF  | -2E |
| OFF  | OFF  | OFF  | OFF  | ON   | ON   | OFF  | OFF  | OFF  | OFF  | OFF  | OFF  | OFF  | OFF  | OFF  | OFF  | ON   | OFF  | OFF  | -3E |
| OFF  | OFF  | OFF  | OFF  | ON   | ON   | ON   | OFF  | OFF  | OFF  | OFF  | OFF  | OFF  | OFF  | OFF  | OFF  | OFF  | ON   | OFF  | -4E |

[0145]

In Embodiment 13, in the same manner as in Embodiments 6 to 12, it is possible to output arbitrary voltages (4E, 3E, 2E, E, 0, -E, -2E, -3E and -4E) from the output terminals U, V and W respectively without short-circuit of each of the flying capacitors FC1 to FC4, and also to simplify control for outputting the voltages of 4E, 3E, 2E, E, 0, -E, -2E, -3E and -4E.

15

[0146]

In addition, unlike the circuit configuration of the related art illustrated in Figs. 29(a) and 29(b), in the case of Embodiment 13, there is no semiconductor element through which currents of three phases of the U phase, the V phase and the W phase flow. Thus, a cooling fin with a high cooling effect is not necessary.

20

[0147]

Although the three-phase output circuit has been explained in Embodiment 13, also in a circuit in which

25

the number of output phases is increased to four or more, phase voltages of respective phases can be outputted separately without short-circuit of each of the flying capacitors FC1 to FC4. The circuit is also advantageous  
5 in a withstand voltage of the semiconductor element and is advantageous in that there is no semiconductor element through which currents of three phases flow, when compared with the circuits of the related art illustrated in Figs. 29(a) and 29(b).

10 [0148]

[Embodiment 14]

Next, a multilevel power convertor in Embodiment 14 will be explained with reference to Fig. 26. A configuration of the multilevel power convertor in  
15 Embodiment 14 is a configuration in which  $N=4$  and  $M=3$  in the case of Embodiment 3. As the voltage selection circuit Fig. 3(a) is used.

[0149]

The basic circuit includes the fourth semiconductor  
20 elements SU2.4 and SU4.4 whose one ends are connected to negative electrode ends of the DC voltage sources DCC2 and DCC4 in the even-numbered stages among four serially connected DC voltage sources DCC1 to DCC4 and which are in common to three phases; the first to third semiconductor  
25 elements SU2.1 to SU2.3, SV2.1 to SV2.3, SW2.1 to SW2.3, SU4.1 to SU4.3, SV4.1 to SV4.3, and SW4.1 to SW4.3 of the three phases which are sequentially connected in series between positive electrode ends of the DC voltage sources DCC2 and DCC4 in the even-numbered stages and  
30 the other ends of the fourth semiconductor elements SU2.4

and SU4.4; the fifth semiconductor elements SU2.5, SV2.5, SW2.5, SU4.5, SV4.5 and SW4.5 whose one ends are connected to common connection points of the first and second semiconductor elements SU2.1, SU2.2, SV2.1, SV2.2, SW2.1, SW2.2, SU4.1, SU4.2, SV4.1, SV4.2, SW4.1, and SW4.2 in the even-numbered stages; the first semiconductor elements SU1.1, and SU3.1 whose one ends are connected to positive electrode ends of the DC voltage sources DCC1 and DCC3 in the odd-numbered stages and which are in common to three phases; the second to fourth semiconductor elements SU1.2 to SU1.4, SV1.2 to SV1.4, SW1.2 to SW1.4, SU3.2 to SU3.4, SV3.2 to SV3.4, and SW3.2 to SW3.4 of the three phases which are sequentially connected in series between the other ends of the first semiconductor elements SU1.1, SU3.1 in the odd-numbered stages and negative electrode ends of the DC voltage sources DCC1 and DCC3 in the odd-numbered stages; and the sixth semiconductor elements SU1.6, SV1.6, SW1.6, SU3.6, SV3.6 and SW3.6 of the three phases whose one ends are connected to common connection points of the third and fourth semiconductor elements SU1.3, SU1.4, SV1.3, SV1.4, SW1.3, SU3.3, SU3.4, SV3.3, SV3.4, SW3.3 and SW3.4 in the odd-numbered stages.

[0150]

The flying capacitors FC2 and FC4 are inserted between all the fifth semiconductor elements SU2.5, SV2.5, SW2.5, SU4.5, SV4.5, SW4.5 in the even-numbered stages and the common connection points of the third and fourth semiconductor elements SU2.3, SV2.3, SW2.3, SU2.4, SU4.3, SV4.3, SW4.3, SU4.4. The flying capacitors FC1 and FC3

are inserted between the common connection points of the first and second semiconductor elements SU1.1, SU1.2, SV1.2, SW1.2, SU3.1, SU3.2, SV3.2, SW3.2 in the odd-numbered stages and all the sixth semiconductor elements SU1.6, SV1.6, SW1.6, SU3.6, SV3.6, SW3.6.

[0151]

The voltage selection circuit is configured by semiconductor elements SU1 to SU12, SV1 to SV12, and SW1 to SW12.

10 [0152]

By controlling each of voltages of the DC voltage sources DCC1, DCC2, DCC3 and DCC4 to  $2E$  and controlling each of voltages of the flying capacitors FC1, FC2, FC3 and FC4 to  $E$ , it is possible to output nine-level voltages of  $4E$ ,  $3E$ ,  $2E$ ,  $E$ ,  $0$ ,  $-E$ ,  $-2E$ ,  $-3E$  and  $-4E$ .

[0153]

In Embodiment 14, in the same manner as in Embodiment 13, it is possible to output arbitrary voltages ( $4E$ ,  $3E$ ,  $2E$ ,  $E$ ,  $0$ ,  $-E$ ,  $-2E$ ,  $-3E$  and  $-4E$ ) from the output terminals U, V and W respectively without short-circuit of each of the flying capacitors FC1 to FC4, and also to simplify control for outputting the voltages of  $4E$ ,  $3E$ ,  $2E$ ,  $E$ ,  $0$ ,  $-E$ ,  $-2E$ ,  $-3E$  and  $-4E$ .

[0154]

25 The circuit illustrated in Fig. 26 is a configuration in which the circuit illustrated in Fig. 13 in Embodiment 7 is doubled.

[0155]

The semiconductor elements SU1 and SU2, SU3 and SU4, SU5 and SU6, SU7 and SU8, SV1 and SV2, SV3 and SV4, SV5

and SV6, SV7 and SV8, SW1 and SW2, SW3 and SW4, SW5 and SW6, and SW7 and SW8 illustrated in Fig. 26 respectively correspond to the semiconductor elements SU1 and SU2, SU3 and SU4, SV1 and SV2, SV3 and SV4, SW1 and SW2, and  
5 SW3 and SW4 illustrated in Fig. 13.

[0156]

Therefore, in the same manner as in Embodiment 7, the maximum value of a voltage applied to the series connection circuit of the semiconductor elements such  
10 as the semiconductor elements SU1 and SU2 in a steady state is each  $2E$ .

[0157]

Although the three-phase output circuit has been explained in Embodiment 14, also in a circuit in which  
15 the number of output phases is increased to four or more, phase voltages of respective phases can be outputted separately without short-circuit of each of the flying capacitors FC1 to FC4. The circuit is also advantageous in a withstand voltage of the semiconductor element and  
20 is advantageous in that there is no semiconductor element through which currents of three phases flow, when compared with the circuits of the related art illustrated in Figs. 29(a) and 29(b).

CLAIMS

[Claim 1]

A multilevel power convertor that generates AC outputs with a plurality of voltage levels obtained by  
5 conversion of voltages of a DC voltage source and a flying capacitor, the multilevel power convertor comprising:

N DC voltage sources ( $N \geq 2$ ) that are connected in series to each other;

basic circuits of M phases ( $M \geq 3$ ), each of which  
10 includes first to fourth semiconductor elements that are sequentially connected in series between positive and negative electrodes of each of the N DC voltage sources;  
a fifth semiconductor element whose one end is connected to a common connection point of the first and second  
15 semiconductor elements; and a sixth semiconductor element whose one end is connected to a common connection point of the third and fourth semiconductor elements;

a flying capacitor that is inserted between the other ends of the fifth semiconductor elements of all the phases  
20 and the other ends of the sixth semiconductor elements of all the phases, the flying capacitor being in common to the M phases; and

voltage selection circuits of the M phases, each of which has common connection points of the second and  
25 third semiconductor elements of each basic circuit as input terminals, includes semiconductor elements between the input terminals and an output terminal, and outputs a potential of any one of the input terminals from the output terminal by selectively controlling ON/OFF of the  
30 semiconductor elements.

[Claim 2]

A multilevel power convertor that generates AC outputs with a plurality of voltage levels obtained by  
5 conversion of voltages of a DC voltage source and a flying capacitor, the multilevel power convertor comprising:

N DC voltage sources ( $N =$  an even number of 2 or greater) that are connected in series to each other;

basic circuits that include a first semiconductor  
10 element whose one end is connected to a positive electrode end of a DC voltage source in an even-numbered stage of the N serially connected DC voltage sources, the first semiconductor element being in common to M phases ( $M \geq 3$ );  
second to fourth semiconductor elements of the M phases  
15 which are sequentially connected in series between the other end of the first semiconductor element in the even-numbered stage and a negative electrode end of the DC voltage source in the even-numbered stage; sixth  
semiconductor elements of the M phases whose one ends  
20 are connected to common connection points of the third and fourth semiconductor elements in the even-numbered stage; a fourth semiconductor element whose one end is connected to a negative electrode end of a DC voltage source in an odd-numbered stage, the fourth semiconductor  
25 element being in common to the M phases; first to third semiconductor elements of the M phases which are sequentially connected in series between a positive electrode end of the DC voltage source in the odd-numbered stage and the other end of the fourth semiconductor element  
30 in the odd-numbered stage; and fifth semiconductor

elements of the M phases whose one ends are connected to common connection points of the first and second semiconductor elements in the odd-numbered stage;

5 a flying capacitor in the even-numbered stage that is inserted between a common connection point of the first and second semiconductor elements in the even-numbered stage and the other ends of the sixth semiconductor elements of all the phases in the even-numbered stage, the flying capacitor being in common to the M phases;

10 a flying capacitor in the odd-numbered stage that is inserted between the other ends of the fifth semiconductor elements of all the phases in the odd-numbered stage and a common connection point of the third and fourth semiconductor elements in the odd-numbered stage, the flying capacitor being in common to the M phases; and

15 voltage selection circuits of the M phases, each of which has common connection points of the second and third semiconductor elements of each basic circuit as input terminals, includes semiconductor elements between the input terminals and an output terminal, and outputs a potential of any one of the input terminals from the output terminal by selectively controlling ON/OFF of the semiconductor elements.

25

[Claim 3]

A multilevel power convertor that generates AC outputs with a plurality of voltage levels obtained by conversion of voltages of a DC voltage source and a flying capacitor, the multilevel power convertor comprising:

30

N DC voltage sources ( $N =$  an even number of 2 or greater) that are connected in series to each other;

basic circuits that include a fourth semiconductor element whose one end is connected to a negative electrode end of a DC voltage source in an even-numbered stage of the  $N$  serially connected DC voltage sources, the fourth semiconductor element being in common to  $M$  phases (where  $M \geq 3$ ); first to third semiconductor elements of the  $M$  phases which are sequentially connected in series between a positive electrode end of the DC voltage source in the even-numbered stage and the other end of the fourth semiconductor element in the even-numbered stage; fifth semiconductor elements of the  $M$  phases whose one ends are connected to common connection points of the first and second semiconductor elements in the even-numbered stage; a first semiconductor element whose one end is connected to a positive electrode end of a DC voltage source in an odd-numbered stage, the first semiconductor element being in common to the  $M$  phases; second to fourth semiconductor elements of the  $M$  phases which are sequentially connected in series between the other end of the first semiconductor element in the odd-numbered stage and a negative electrode end of the DC voltage source in the odd-numbered stage; and sixth semiconductor elements of the  $M$  phases whose one ends are connected to common connection points of the third and fourth semiconductor elements in the odd-numbered stage;

a flying capacitor in the even-numbered stage that is inserted between all the fifth semiconductor elements and a common connection point of the third and fourth

semiconductor elements in the even-numbered stage, the flying capacitor being in common to the M phases;

a flying capacitor in the odd-numbered stage that is inserted between a common connection point of the first  
5 and second semiconductor elements and all the sixth semiconductor elements in the odd-numbered stage, the flying capacitor being in common to the M phases; and

voltage selection circuits of the M phases, each of which has common connection points of the second and  
10 third semiconductor elements of each basic circuit as input terminals, includes semiconductor elements between the input terminals and an output terminal, and outputs a potential of any one of the input terminals from the output terminal by selectively controlling ON/OFF of the  
15 semiconductor elements.

[Claim 4]

A multilevel power convertor that generates AC outputs with a plurality of voltage levels obtained by  
20 conversion of voltages of a DC voltage source and a flying capacitor, the multilevel power convertor comprising:

N DC voltage sources ( $N = \text{an even number of } 2 \text{ or greater}$ ) that are connected in series to each other;

basic circuits of M phases ( $M \geq 3$ ), each of which  
25 includes second and third semiconductor elements which are sequentially connected in series to a positive electrode end of a DC voltage source in an even-numbered stage of the N serially connected DC voltage sources; and third and second semiconductor elements which are  
30 sequentially connected in series to a negative electrode

end of a DC voltage source in the odd-numbered stage of the N serially connected DC voltage sources;

a flying capacitor that is connected parallel to the second and third semiconductor elements in each of the even-numbered stage and odd-numbered stage, the flying capacitor being in common to the M phases; and

voltage selection circuits of the M phases, each of which has common connection points of the second and third semiconductor elements of each basic circuit and a common connection point of a negative electrode end of the DC voltage source in the even-numbered stage and a positive electrode end of the DC voltage source in the odd-numbered stage as input terminals, includes semiconductor elements between the input terminals and an output terminal, and outputs a potential of any one of the input terminals from the output terminal by selectively controlling ON/OFF of the semiconductor elements.

[Claim 5]

A multilevel power convertor that generates AC outputs with a plurality of voltage levels obtained by conversion of voltages of a DC voltage source and a flying capacitor, the multilevel power convertor comprising:

N DC voltage sources ( $N = \text{an even number of } 2 \text{ or greater}$ ) that are connected in series to each other;

basic circuits of M phases ( $M \geq 3$ ), each of which includes second to fourth semiconductor elements which are sequentially connected in series between positive and negative electrode ends of a DC voltage source in

an even-numbered stage of the N serially connected DC voltage sources; a sixth semiconductor element whose one end is connected to a common connection point of the third and fourth semiconductor elements in the even-numbered stage; first to third semiconductor elements which are sequentially connected in series between positive and negative electrode ends of a DC voltage source in an odd-numbered stage of the N serially connected DC voltage sources; and a fifth semiconductor element whose one end is connected to a common connection point of the first and second semiconductor elements in the odd-numbered stage;

a flying capacitor in the even-numbered stage that is inserted between the other ends of all the sixth semiconductor elements in the even-numbered stage and a common connection point of a positive electrode end of the DC voltage source and the second semiconductor element in the even-numbered stage, the flying capacitor being in common to the M phases;

a flying capacitor in the odd-numbered stage that is inserted between the other ends of all the fifth semiconductor elements in the odd-numbered stage and a common connection point of a negative electrode end of the DC voltage source and the third semiconductor element in the odd-numbered stage, the flying capacitor being in common to the M phases; and

voltage selection circuits of the M phases, each of which has common connection points of the second and third semiconductor elements of each basic circuit as input terminals, includes semiconductor elements between

the input terminals and an output terminal, and outputs a potential of any one of the input terminals from the output terminal by selectively controlling ON/OFF of the semiconductor elements.

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[Claim 6]

A multilevel power convertor that generates AC outputs with a plurality of voltage levels obtained by conversion of voltages of a DC voltage source and a flying capacitor, the multilevel power convertor comprising:

10

N DC voltage sources ( $N =$  an even number of 2 or greater) that are connected in series to each other;

basic circuits of  $M$  phases ( $M \geq 3$ ), each of which includes first to third semiconductor elements which are sequentially connected in series between positive and negative electrode ends of a DC voltage source in an even-numbered stage of the  $N$  serially connected DC voltage sources; a fifth semiconductor element whose one end is connected to a common connection point of the first and second semiconductor elements in the even-numbered stage;

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second to fourth semiconductor elements which are sequentially connected in series between positive and negative electrode ends of a DC voltage source in an odd-numbered stage of the  $N$  serially connected DC voltage sources; and a sixth semiconductor element whose one end is connected to a common connection point of the third and fourth semiconductor elements in the odd-numbered stage;

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a flying capacitor in the even-numbered stage that is inserted between the other ends of all the fifth

semiconductor elements in the even-numbered stage and  
a common connection point of a negative electrode end  
of the DC voltage source and the third semiconductor  
element in the even-numbered stage, the flying capacitor  
5 being in common to the M phases;

a flying capacitor in the odd-numbered stage that  
is inserted between the other ends of all the sixth  
semiconductor elements in the odd-numbered stage and a  
common connection point of a positive electrode end of  
10 the DC voltage source and the second semiconductor element  
in the odd-numbered stage, the flying capacitor being  
in common to the M phases; and

voltage selection circuits of the M phases, each  
of which has common connection points of the second and  
15 third semiconductor elements of each basic circuit as  
input terminals, includes semiconductor elements between  
the input terminals and an output terminal, and outputs  
a potential of any one of the input terminals from the  
output terminal by selectively controlling ON/OFF of the  
20 semiconductor elements.

[Claim 7]

The multilevel power convertor as claimed in any  
one of the preceding claims 1 to 6, wherein:  
25 the number of series-connection of all or some of the  
semiconductor elements in the basic circuits and the  
voltage selection circuits is equal to or greater than  
2.

30 [Claim 8]

The multilevel power convertor as claimed in any one of the preceding claims 1 to 7, wherein:

the number of parallel-connection of all or some of the semiconductor elements in the basic circuits and  
5 the voltage selection circuits is equal to or greater than 2.