

**Epitaxially coated semiconductor wafer of monocrystalline silicon and method
for the production thereof**

5 The invention provides an epitaxially coated semiconductor wafer of monocrystalline silicon having a diameter of not less than 300 mm. The invention further relates to a method of producing an epitaxially coated semiconductor wafer of monocrystalline silicon having a diameter of not less than 300 mm.

10 Prior art/problems

Epitaxially coated semiconductor wafers of monocrystalline silicon are required as precursors for production of electronic components. Owing to superior electrical properties, they are frequently preferred over polished semiconductor wafers of monocrystalline silicon. This is the case, for example, where the production of what
15 are called CMOS image sensors, or CIS components for short, is concerned.

Epitaxially coated semiconductor wafers of monocrystalline silicon are typically produced by gas phase deposition (CVD) of the epitaxial layer on a substrate wafer at temperatures of 1100°C to 1250°C. Substrate wafers of monocrystalline silicon having
20 a diameter of not less than 300 mm are typically coated in an apparatus for coating individual wafers.

US 2010/0062611 A1 describes a process for thinning the backside of a semiconductor wafer which can be used in the course of the production of backside-
25 illuminated image sensors.

In order to be useful as a precursor for production of CIS components, the epitaxially coated semiconductor wafer has to meet particular demands. The demands are particularly demanding with regard to the thickness and specific electrical resistance (resistivity) of the epitaxial layer. Both the thickness and the specific electrical
30 resistance, called resistance hereinafter, must be very substantially homogeneous over the radius of the semiconductor wafer. A measure for description of the inhomogeneity is the quotient of the difference of greatest and smallest thickness

(greatest and smallest resistance) and the sum total of greatest and smallest thickness (greatest and smallest resistance) multiplied by the factor of 100%.

US 2010/0213168 A1 describes various measures for improving the homogeneity of the thickness of an epitaxial layer of monocrystalline silicon.

US 2011/0114017 A1 describes a method of producing an epitaxially coated semiconductor wafer of monocrystalline silicon, wherein an epitaxial layer is deposited, and the inhomogeneity of the resistance is 4% or less.

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Regardless of such teachings, there is still a need for an improvement in the homogeneity of layer thickness and resistance, especially because there is a lack of any satisfactory solution to date for matching the layer thickness and the resistance in a problematic edge region having a distance of up to 15 mm from the edge of the semiconductor wafer to the layer thickness and resistance of regions at greater distance from the edge. In the problematic edge region, there is a decrease in the temperature of the substrate wafer toward the edge because the substrate wafer loses heat as a result of thermal radiation close to the edge. Unless countermeasures are taken, the layer thickness of an epitaxial layer doped with a p-type dopant in this region will become less and the resistance will become greater. If the dopant is of the n-type, the resistance will become less. Known countermeasures, such as the attempt to influence the temperature field, have to date been at the expense of the homogeneity of the thickness of the epitaxial layer in regions outside the problematic edge region and/or increase the propensity of the semiconductor wafer to be subject to slips. Slips arise especially on relaxation of stresses caused by temperature differences. Such temperature differences occur particularly in the edge region as radial and axial temperature gradients, i.e. as a temperature drop directed toward the edge of the substrate wafer and as a temperature difference between the substrate wafer which is colder in that case and the susceptor which is warmer in that case.

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Stresses in the crystal lattice can be measured by means of SIRD (scanning infrared depolarization). US 2012/0007978 A1 contains a description of how SIRD stresses

can be measured and expressed in depolarization units DU, and also a reference to a suitable measuring instrument.

The inventors of the present invention have addressed the task, which is the object of
5 the present invention, of further reducing the inhomogeneity of the thickness of the epitaxial layer and the inhomogeneity of the resistance of the epitaxial layer without increasing the propensity of the semiconductor wafer to development of slips.

The object of the invention is achieved by a semiconductor wafer of monocrystalline
10 silicon having a diameter of not less than 300 mm, comprising a substrate wafer of monocrystalline silicon and a dopant-containing epitaxial layer of monocrystalline silicon atop the substrate wafer, wherein an inhomogeneity of the thickness of the epitaxial layer is not more than 0.5% and an inhomogeneity of the specific electrical resistance of the epitaxial layer is not more than 2%.

15 The thickness and resistance of the epitaxial layer of the semiconductor wafer are accordingly particularly homogeneous. The thickness of the epitaxial layer is preferably 1 to 20 μm . The substrate wafer preferably also contains a dopant and may further additionally have been doped with carbon or with nitrogen. The semiconductor
20 wafer is preferably a pp^+ wafer or an nn^- wafer.

The semiconductor wafer, in an edge region with a distance of up to 15 mm from the edge of the semiconductor wafer, with an edge exclusion of 0.5 mm, has SIRD stresses which cause a degree of depolarization of preferably not more than 30
25 depolarization units.

The object is additionally achieved by a method of producing a coated semiconductor wafer of monocrystalline silicon, comprising
the providing of a substrate wafer of monocrystalline silicon having a diameter of not
30 less than 300 mm;
the placing of the substrate wafer atop a susceptor of an apparatus for coating individual wafers, wherein the apparatus has an upper cover with an annular region

which concentrates radiation transmitted through the annular region in an edge region of the substrate wafer;

the heating of the substrate wafer to a deposition temperature by means of a radiation source arranged above the upper cover of the apparatus;

- 5 the depositing of an epitaxial layer of silicon by passing process gas over the heated substrate wafer, where the process gas comprises hydrogen, inert gas and a deposition gas, and the deposition gas comprises dopant and a silicon source.

- 10 The method includes measures which affect the depositing of the epitaxial layer in the problematic edge region such that the influence remains largely locally limited. For instance, it is ensured that the resistance rises and the temperature field is adjusted in this region, while simultaneously avoiding temperature gradients which cause slips.

- 15 In order to positively influence the deposition outcome, especially with regard to the resistance, the process gas comprises not only hydrogen but also inert gas. A useful inert gas is argon in particular. Alternatively, it is possible to use another noble gas or any mixture of two or more noble gases as inert gas. Preference is given to passing hydrogen and inert gas in a volume ratio of not less than 6 and not more than 20 over the substrate wafer. The additional use of inert gas surprisingly brings about an
- 20 increase in the resistance in the problematic edge region and a certain improvement with regard to homogenization of the thickness of the epitaxial layer. Furthermore, the thickness of the epitaxial layer in the problematic edge region of the substrate wafer is improved in a controlled manner by coating the substrate wafer in an apparatus for coating individual wafers, the upper cover of which is structured in a particular
- 25 manner. It has an annular region which, by contrast with adjacent regions, concentrates radiation passing through. The cross section through the annular region of the upper cover preferably has upward convex curvature or has the outline of a Fresnel lens. The concentrated radiation is incident in the problematic edge region of the substrate wafer, as a result of which the temperature there is selectively
- 30 increased. The local increase in temperature in the problematic edge region of the substrate wafer compensates for the loss of heat that arises there as a result of thermal radiation, and its effect is that temperature differences become smaller toward regions further inward. Ultimately, in this way, the thickness of the epitaxial layer in the edge region of the substrate wafer is matched to the thickness of the epitaxial layer in
- 35 regions of the substrate wafer further inward.

The invention is elucidated further hereinafter with reference to drawings.

5 **Brief description of the drawings**

Fig. 1a and **fig. 1b** show the effect of argon in the process gas on the homogenization of the thickness of the epitaxial layer.

10 **Fig. 2** shows the effect of argon in the process gas on the homogenization of the resistance of the epitaxial layer.

Fig. 3 shows the cross section of an apparatus suitable for coating individual wafers by means of CVD.

15 **Fig. 4** shows a schematic of the mode of action of an upper cover having an annular region that concentrates radiation passing through.

20 **Fig. 5** shows the geometric relationship between the position of the annular region of the upper cover and the edge region of the substrate wafer in which radiation is concentrated when it passes through the annular region of the cover.

25 **Fig. 6** and **fig. 7** show images of SIRD measurements on a semiconductor wafer produced in accordance with the invention (fig. 6) and on a semiconductor wafer (fig. 7) which not has been produced in an inventive manner.

30 **Fig. 8** shows, over the radius R , the profile of the deviation V_{th} in the layer thickness from a target value in the case of a semiconductor wafer produced in accordance with the invention (solid line) with layer thickness according to the invention and in the case of a semiconductor wafer (dotted line) which has not been produced in an inventive manner.

Fig. 9 shows, over the radius R , the profile of the deviation V_r in the resistance from a target value in the case of a semiconductor wafer produced in accordance with the invention (solid line) with layer thickness according to the invention and in the case of a semiconductor wafer (dotted line) which has not been produced in an inventive manner.

List of reference numerals used

- 1 upper cover
- 2 lower cover
- 10 3 side wall
- 4 substrate wafer
- 5 susceptor
- 6 radiation source
- 7 annular region of the upper cover
- 15 8 radiation passing through
- 9 epitaxial layer
- 10 material

20 Fig. 1a and fig. 1b show the effect of argon in the process gas on the homogenization of the thickness of the epitaxial layer. What is shown in each case is a typical profile of deviation of the thickness of the epitaxial layer from a target thickness Δ versus the diameter d of the substrate wafer. The profile of the thickness of the epitaxial layer in the case of fig. 1b is more homogeneous than in the case of fig. 1a. This difference is

25 attributable to the fact that the process gas in the deposition of the epitaxial layer additionally contained argon (fig. 1b), or did not contain any argon (fig. 1a). Argon was fed in with a proportion of 3 slm. The proportion of hydrogen in both cases was 50 slm. The deposition gas was the same in both cases, as was the deposition temperature, namely 1115°C.

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Fig. 2 shows the effect of argon in the process gas on the homogenization of the resistance of the epitaxial layer. Two curves are shown, which show the profile of the resistance ρ versus the diameter d of the semiconductor wafer. The more

homogeneous resistance profile (curve with square data points) is attributable to the fact that the process gas in the deposition of the epitaxial layer additionally contained argon and did not in the comparative case (curve with diamond-shaped data points). Argon was supplied with a proportion of 3 slm. The proportion of hydrogen in both
 5 cases was 60 slm.

The apparatus shown in fig. 3 comprises a reactor chamber bounded by an upper cover ("upper dome") 1, a lower cover ("lower dome") 2 and a side wall 3. The upper and lower covers 1, 2 are transparent to thermal radiation which is emitted by the
 10 radiation sources 6 arranged above and below the reactor chamber. The epitaxial layer is deposited from the gas phase on the top side of the substrate wafer 4, by passing process gas over the substrate wafer heated by thermal radiation. The process gas is fed in through a gas inlet in the side wall 3, and the offgas remaining after the reaction is removed through a gas outlet in the side wall 3. The apparatus
 15 shown represents an embodiment having a further gas inlet and a further gas outlet in order, for example, to be able to introduce a purge gas into the volume of the reactor chamber beneath the substrate wafer and discharge it therefrom. However, the further gas inlet and the further gas outlet make no contribution to the achievement of the object of the invention. During the deposition of the epitaxial layer, the substrate wafer
 20 4 lies on the contact area of a susceptor 5 and is rotated about an axis of rotation in the middle of the substrate wafer together with the susceptor.

The upper lid 1 has an annular region 7 (fig. 4) which concentrates radiation passing through. The thickness of the upper lid 1 is thicker in the annular region 7 than in the
 25 adjoining regions. The cross section through the annular region of the upper cover preferably has upward convex curvature or has the outline of a Fresnel lens. The annular region 7 acts on the radiation 8 passing through like a collecting lens that concentrates radiation. The concentrated radiation is incident in the edge region of the substrate wafer, which preferably has a distance of up to 15 mm from the edge of
 30 substrate wafer 4. The incident radiation eliminates a radial temperature drop in the edge region, such that an envisaged amount of material 10 is deposited there and the thickness of the epitaxial layer 9 attains an envisaged value.

The position of the annular region 7 of the upper cover and that of the edge region of the substrate wafer correlate according to the rules of beam optics, as shown in fig. 5. The length r_D denotes the distance of the annular region 7 of the upper cover 1 from the perpendicular through the middle of the upper cover and is calculated from the difference between the lengths r_S and x . The length r_D can be calculated as an approximation with defined heights b and h , defined length a and defined angle α , where the height b denotes the distance of the radiation source from the plane of the substrate wafer, the length r_S denotes the distance of the radiation source from the perpendicular through the middle of the upper cover, the height h denotes the distance of the upper cover 1 from the substrate wafer 4, the length x denotes the distance of the annular region 7 from the height b , the length a denotes the greatest distance of the edge region of the substrate wafer from the height b , and the angle α denotes the angle, opposite the base, of a triangle with height b and length a as the base.

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Detailed description of working examples according to the invention

20 Semiconductor wafers of monocrystalline silicon were produced by the method of the invention and, for the purpose of comparison, semiconductor wafers were also produced by a different method.

25 Substrate wafers of monocrystalline silicon having a diameter of 300 mm were coated in a single-wafer apparatus according to fig. 3 within an epitaxial layer of silicon, after they had been divided from a single crystal, ground, etched and polished.

30 On employment of the method of the invention, the apparatus had an upper cover having an annular region that concentrated the radiation that passed through in an edge region of the substrate wafer. On employment of the different method, the upper cover lacks this structure.

On employment of the method of the invention, the process gas consisted of hydrogen (70 slm), argon (5 slm) and deposition gas (trichlorosilane (6 slm), diborane

(50 ppm in hydrogen (180 sccm)) diluted in 4 l of hydrogen), and the epitaxial layer was deposited at a temperature of 1130°C.

On employment of the different method, the process gas consisted solely of hydrogen (55 slm) and deposition gas (trichlorosilane (10 slm), diborane (50 ppm in hydrogen (180 sccm)) diluted in 4 l of hydrogen), and the epitaxial layer was deposited at a temperature of 1125°C.

Fig. 6 shows the image of an SIRD measurement on a semiconductor wafer produced in accordance with the invention. The degree of depolarization remained within the preferred degree. In none of the measurement cells was the degree of depolarization greater than 30 DU. In the case of the semiconductor wafer that was produced by the different method, 0.907% of the measurement cells were noticeable owing to a degree of depolarization of more than 30 DU (fig. 7). The SIRD measurement was conducted with an SIRD-AB300 instrument from PVA TePla AG, placing a polar coordinate grid with a cell size of 1 mm (radius) and 2 mm (azimuth) over the measurement area for evaluation. For each cell of the grid, the degree of depolarization was determined. A depolarization unit DU corresponds to a degree of depolarization of 1×10^{-6} . What is shown in each case is the unrolled peripheral region of the semiconductor wafer with a distance of 4.5 mm or less from the edge of the semiconductor wafer and with the notch position (pos = 0°) in the middle. The peripheral region with a distance of 15 mm to 4.5 mm from the edge of the semiconductor wafer is not shown because the SIRD stress was unremarkable in both cases.

Fig. 8 shows, over the radius R, the profile of the deviation V_{th} in the layer thickness from a target value in the case of a semiconductor wafer produced in accordance with the invention (solid line) and in the case of a semiconductor wafer (dotted line) which has been produced by the different method. Only the semiconductor wafer produced in accordance with the invention fulfilled the criterion of the invention with regard to layer thickness.

Fig. 9 shows, over the radius R, the profile of the deviation V_r in the resistance from a target value in the case of a semiconductor wafer produced in accordance with the invention (solid line) and in the case of a semiconductor wafer (dotted line) which has been produced by the different method. Only the semiconductor wafer produced in

accordance with the invention fulfilled the criterion of the invention with regard to resistance.

The above description of illustrative embodiments should be regarded as an
5 illustration. The disclosure that has thus been made enables the person skilled in the art firstly to understand the present invention and the associated advantages, and secondly encompasses, within the understanding of the person skilled in the art, obvious alterations and modifications to the structures and methods described as well. Therefore, all such alterations and modifications and equivalents shall be covered by
10 the scope of protection of the claims.

Claims

1. A semiconductor wafer of monocrystalline silicon having a diameter of not less than 300 mm, comprising
 - 5 a substrate wafer of monocrystalline silicon and a dopant-containing epitaxial layer of monocrystalline silicon atop the substrate wafer, wherein an inhomogeneity of the thickness of the epitaxial layer is not more than 0.5% and an inhomogeneity of the specific electrical resistance of the epitaxial layer is not more than 2%.
- 10 2. The semiconductor wafer as claimed in claim 1, wherein the thickness of the epitaxial layer is not less than 1 μm and not more than 20 μm .
3. The semiconductor wafer as claimed in claim 1 or claim 2, wherein the semiconductor wafer, in an edge region with a distance of up to 15 mm from the edge
 - 15 of the semiconductor wafer, with an edge exclusion of 0.5 mm, has SIRD stresses which cause a degree of depolarization of not more than 30 depolarization units.
4. A method of producing a coated semiconductor wafer of monocrystalline silicon, comprising
 - 20 the providing of a substrate wafer of monocrystalline silicon having a diameter of not less than 300 mm;
 - the placing of the substrate wafer atop a susceptor of an apparatus for coating individual wafers, wherein the apparatus has an upper cover with an annular region which concentrates radiation transmitted through the annular region in an edge region
 - 25 of the substrate wafer;
 - the heating of the substrate wafer to a deposition temperature by means of a radiation source arranged above the upper cover of the apparatus;
 - the depositing of an epitaxial layer of silicon by passing process gas over the heated substrate wafer, where the process gas comprises hydrogen, inert gas and a
 - 30 deposition gas, and the deposition gas comprises dopant and a silicon source.
5. The method as claimed in claim 4, wherein the edge region of the substrate wafer has a distance of up to 15 mm from an edge of the substrate wafer.

6. The method as claimed in claim 4 or claim 5, comprising the passing of hydrogen and inert gas in a volume ratio of not less than 6 and not more than 20 over the heated substrate wafer.
- 5 7. The method as claimed in any of claims 4 to 6, wherein the cross section through the annular region of the upper cover has upward convex curvature or the outline of a Fresnel lens.