

Description

This invention relates to an adaptive recognising device. There are many technical fields in which electronic recognition processes are employed such as optical pattern or character recognition, voice recognition, and the like. In addition to such well known processes where values comprising labels are assigned to patterns of one form or another and output as responses by a recogniser, there are also many other processes in which patterns are recognised and values are output as responses. Two examples of such processes are for example echo cancellation and signal filtering, though hitherto such processes have not been considered as pattern recognition problems.

In all such processes though patterns are input, and a response is output and whilst the present invention is particularly suitable for use with recognition processes which also involve cancellation processes it may be adopted for other recognition processes where its properties may be used to advantage. In order to discuss the present invention more readily though particular reference will be made to the field of echo cancellation.

Echo cancellers are used in telephone circuits to suppress echoes received from a circuit by a station which emanate from signals transmitted into the circuit by the same station. Echoes result from a variety of causes for example slight mismatches in four to two wire hybrids and from acoustic feedback in the distant stations handset. Normally such echoes are not noticeable but with International calls, where the echo may be delayed by more than a few tens of milliseconds, they can be annoying. In order to maintain duplex operation an echo canceller is required which can model the response of any feedback path. Since different feedback paths and different hybrids will have different characteristics the canceller must be adaptive to be useful in any circuit.

Three main forms of filters/echo cancellers are known. In the first, known as an F.I.R. canceller (Finite Impulse Response), the input signal is convolved with the impulse response of the line to form an instantaneous echo estimate. In the UK the maximum echo delay encountered is about 32ms and with an 8kHz sampling rate a 256 tap shift register would be needed to hold the relevant history of the input signal whose echo is to be estimated. In order to estimate such an echo and update the response the canceller would need to perform 512 multiplications and 512 additions within the 125µs period between samples. To do this is expensive in terms of the high speed devices and fast memory required.

A second form of echo canceller uses the entire contents of the signal history shift register to address a large memory. Each possible previous form of the signal thus has a corresponding memory location and in each of these locations data is stored which comprises an estimate of the corresponding echo response for the particular signal history in the signal history shift register. However, if 8 bit words are used with the 256 tap shift register, which would be required as described above, the signal history shift register will have 2048 locations and thus the random access memory for storing the corresponding echo estimates will require 2²⁰⁴⁸ 8 bit word locations. Such an amount of memory is clearly impracticable to implement and the only practical cancellers of this type use a signal history shift register which is considerably smaller. The advantages of such a system are that no multiplications or additions are required and that since each input signal accesses a different memory location many non-linearity in the feedback path can be cancelled. However, the adaptation times of such cancellers is long and in any event due to the constraints on memory size such cancellers are only practicable for use in systems where the number of transmitted symbols is small and the echo path short. Such systems are therefore unsuitable for speech signals.

A third form of echo canceller uses the contents of stages of an input shift register each containing a digital word of a signal to provide the address for a plurality of random access memories, each stage and thus word providing the address for a corresponding RAM. The contents of the RAM locations addressed thus are then summed to provide an echo estimate which can be updated. However such cancellers are only able to cope with amplitude dependent instantaneous non-linearities.

An arrangement of this kind is shown in 'Patent Abstracts of Japan', Volume 8, no. 78 (E-237)(1515), 10 April 1984, page 20 E 237; and JP-A-58 223 928 (Nippon Denki K.K.) 26.12.83. A digital filter which also comprises an arrangement of this kind, but which implements ROMs in place of RAMs, is shown in UK Patent Application GB-A-2 095 067.

According to the present invention there is provided an electronic adaptive recognising device comprising, an input connected to an input store having a plurality of storage locations allowing data representative of elements of a signal pattern to be recognised to be stored at locations related to the positions of the elements in said pattern; a plurality of addressable stores each having one address line specifying one or more store locations therein, each of said addressable store locations being capable of containing a word of at least one bit, the address lines each being connected to a respective location in the input store such that the contents of said input store are capable of specifying a store location in each of the addressable stores; means for deriving a common value dependent on the contents of the store locations specified by the contents of the input store; an input for received values; calculating means for calculating a value dependent on the common value

and a corresponding one of the received values; and updating means for applying an update value dependent on said calculated value to the contents of the specified store locations; characterised in that the address lines are connected in a random manner to the locations of the input store.

The use of random connections gives the ability to model non-linearities where the non-linearity cannot be defined.

In another aspect, the invention provides an electronic adaptive recognising device comprising: an input connected to an input store having a plurality of storage locations allowing data representative of elements of a signal pattern to be recognised to be stored at locations related to the positions of the elements in said pattern; a plurality of addressable stores each having an address line specifying one or more store locations therein, each of said addressable store locations being capable of containing a word of at least one bit, said address lines each being connected to a respective location in said input store such that the contents of said input store are capable of specifying a store location in each of said addressable stores; means for deriving a common value dependent on the contents of the store locations specified by the contents of said input store; an input for received values; calculating means for calculating a value dependent on said common value and a corresponding one of said received values and updating means for applying an update value dependent on said calculated value to the contents of said specified store locations, characterised in that each of the addressable stores has only one address line and not more than two store locations.

If only one store location per store is provided the adaption time of the device is extremely quick but by using two store locations per store some of this speed may be sacrificed for an increased ability to model non-linearities.

Since there is only one address line per addressable store the memory requirements are very small and the training time of the device will also be small. However, though such a system will not completely model non linearities in the input signal pattern if only one store location per addressable store is provided and though with two store locations per addressable store the capacity to model non-linearities is still limited, use of either one or two store locations per addressable store is still useful for the speed it gives and the economy of memory.

The present invention provides an adaptive recognising device which can enable implementation of devices, such as for example adaptive memory echo cancellers, without the need for excessive amounts of random access memory. The input store is preferably a shift register through which digital data forming a pattern is fed and the addressable stores are preferably each random access memories. In effect each of the addressable stores contributes to the common value which in turn contributes directly or indirectly to an estimate of the received value which in the case of an echo canceller will be the returned echo.

The means for deriving a common value dependent on the contents of the addressable store locations specified by the input store locations can take a number of suitable forms. Preferably though the common value is the sum of the contents of specified addressable store locations. Other functions than the sum may be used to derive the common value, though for each different function used an appropriate updating means for calculating the update value must be used to ensure that the device adapts correctly. The device is remarkable for its ability to recognise input data patterns and output corresponding responses whilst using only a relatively small amount of memory and whilst also being able to very quickly adapt itself to account for changes in the received value's relationship to the input signal pattern which may be caused for example by a change in echo path in the case of an echo canceller. The device will also operate on any input of digital data which forms patterns in the input store whether the data represents data, a visual, aural, or any other pattern or mixture of them.

Preferably the corrected value is obtained by subtracting an estimate value from a corresponding one of the received values, the estimate value being derived from the average value of the contents of the store locations specified by the corresponding contents of the input store.

Alternatively the corrected value can be obtained by subtracting the sum from a corresponding one of the received values, providing the updating means comprises means for dividing the corrected value by the number of addressable stores connected to the input store in order to provide the update value. In both cases an update value is provided but in the former case both it and the partial estimates in the addressable store locations are each individual estimates whilst in the latter case they are true partial estimates requiring summing but not normalising or averaging before being supplied to the calculating means. In this latter case though, normalisation of the corrected value is required before it can be used as an update value. In both cases the update value is preferably added to each of the specified store locations in the addressable stores.

In certain circumstances with the first aspect of the invention, it is advantageous to have more than one address line per addressable store and in this case the addressable stores each have a plurality of additional address lines which together with the single address line address a plurality of locations in said input store and are connected to locations in said input store at random. This arrangement will of course increase the adap-

tion time of the device but it also enables the device to model many more different types of non-linearities and will be particularly useful if the form of the non-linearity to be modelled cannot be defined precisely.

When the addressable stores each have a plurality of additional address lines which together with the single address line address a plurality of store locations in the store then whether or not the locations of the address line connections are chosen randomly it is preferable that the number of address lines per addressable store is smaller than the number of bits each word of the input data is comprised of. This will result in a great saving of memory used by the addressable stores and can be effected with either a random distribution of the address lines or with a specific arrangement of them to suit a particular purpose.

In all the above embodiments of the present invention more than one address line may advantageously be connected to a single input store location.

Instead of using a single recognising device a plurality of them may be combined by having their input stores connected in series and having a common input, input for received values, output for corrected values, calculating means and updating means. The estimate value used in the calculating means in this case is the average of the average values of the contents of the addressable store locations specified by the contents of each of the input stores.

A device according to the present invention may also include means for selectively operating the device according to a predetermined sequence in either a recognition mode in which corrected values are output or in an update mode where the update value is applied, preferably by being added, to the contents of each of said addressable store locations by the update means.

The device according to the present invention may be made capable of recognising data forming a particular input signal pattern independently of the pattern's position in a shift register forming the input store by writing identical values in locations corresponding to a plurality of positions of said signal pattern in the input store shift register.

The device may of course be used as an echo canceller for use with a transmitter/receiver unit when the transmitter output is applied to the device input, the receiver is connected to the output for corrected values and the input for received values is supplied with a signal including an echo which is to be received by the receiver. This enables portions of the received signal which are derived from the transmitted signal to be cancelled.

The device may also be used as a self training filter or waveform recogniser by connecting the input to the input for received values and providing means for interrupting the updating of the contents of the addressable store locations. Using the device in this way enables the device to be trained to recognise a particular input signal pattern or patterns by passing the appropriate signal patterns into the input. After updating is interrupted the corrected value output will only be cancelled for those input signal patterns on which the device has been trained.

Preferred embodiments of the present invention will now be described with reference to the accompanying drawings in which:

Figure 1 shows an hypothetical adaptive memory echo canceller according to the prior art in diagrammatic form.

Figure 2 shows in diagrammatic form an adaptive recognising device according to an embodiment of the present invention.

Figure 3 shows in diagrammatic form an adaptive recognising device according to a further embodiment of the present invention using a plurality of randomly distributed address lines for each addressable store.

Figure 4 shows in diagrammatic form an adaptive recognising device according to a further embodiment of the present invention using a plurality of input stores.

Figures 5 & 6 show in diagrammatic form two arrangements of analogue to digital and digital to analogue converters for use with the device shown in Figures 2 to 4 as an echo-canceller in an analogue circuit.

Figure 7 shows in diagrammatic form an embodiment of the present invention being used as an echo canceller in a telephone circuit using A-law words showing where linearisation of the signal is required.

Figure 8 shows a partial view in diagrammatic form of a further embodiment of the present invention being used as an echo canceller in a telephone circuit using A-law or μ -law words.

Figure 9 shows a partial view in diagrammatic form of another embodiment of the present invention being used as an echo canceller in a telephone circuit using A-law or μ -law words.

In Figure 1 an adaptive memory echo canceller according to the prior art is shown. An input signal 1 which is also to be transmitted from a hybrid 2 is fed into a 256x8bit shift register 3. Once the shift register 3 contains a sequence of words it also in effect contains a pattern of binary values. Each of the cells of the shift register

thus contains either 0 or 1 and each of these cells is also connected to an address line of a block 4 of random access memory (RAM). Since the shift register 3 contains 2048 cells the RAM will have to have 2^{2048} words of memory in order to store an echo estimate for each of the possible input signal bit patterns in the shift register 3. Assuming such a memory could be constructed the addresses in the RAM 4 can be used to store echo estimates which can be read out as an estimate value 5 when the corresponding signal pattern is detected by the address lines connected to the shift register. The echo estimate value 5 corresponding to the input signal 1 is then subtracted 7 from the actual echo 6 received from the hybrid 2 to provide a residual echo signal 8. The residual echo signal 8 is used to send an update value 9 to the RAM location where the estimate value 5 came from so that when exactly the same signal appears again the corrected echo estimate will be read out.

The major disadvantage with such a system is that an impossibly large amount of memory is required. Such echo cancellers can thus only be used where the echo path is short and the number of transmitted symbols small which considerably limits their usefulness. A further disadvantage of such a large memory requirement is that the training time taken before a response for each of the types of signal likely to be encountered in normal operation has been stored is very great.

Figure 2 shows a general embodiment of the present invention in diagrammatic form. The use of the circuit is not restricted to use as an echo canceller but may be put to a number of uses. An input signal 10 is fed into an input store 12 which is preferably a shift register. The manner in which the data is fed in will depend on its source and the use to which the device is being put and is not important provided the result is an array of cells each containing bits of the input data. The input signal may, if preferred, be fed through the shift register 12 as part of a line 14 rather than being tapped from it.

Linked to individual cells of the input store 12 are a plurality of address lines 16. Each of these lines senses the contents of a particular input store cell and each forms the address line for a respective random access memory 18 (of which only a representative few are shown). Since there is only one address line per RAM each RAM only contains either one or two addresses. Thus the size of RAM required is considerably reduced compared to the prior art whilst the number input store cells remains the same. For example in Figure 2 128 input store cells are shown which using the construction of Figure 1 would require a RAM with 2^{128} addresses. Using the construction of Figure 2 RAMs with only 2^1 addresses are required and whilst more than one of these is used the total memory requirement is still considerably reduced.

The address lines 16 may be connected to the input store cells in any suitable way either according to a predetermined pattern depending on the use to which the device is put or randomly as shown in Figure 2. The connections of different lines may also be to identical cells. The number of lines 16 and thus the number of RAMs 18 may take any suitable number, typically this might be such that there are as many address lines as input store cells but a lesser or greater number may be used.

The address lines 16 each specify an address in a corresponding RAM 18 corresponding to the contents of the input store 12 and the location of the address lines 16 among the store cells. At each of the RAM store locations a word is stored indicating a partial response to the input store contents.

A common value based on these partial responses is then calculated by an appropriate device 22. The way in which the common value is derived from the partial responses may take a number of suitable forms but is preferably by addition of all the partial responses. A calculating means 23 then calculates a corrected value 28 based on the common value forming a total estimate 26 and also on a received value 24 which is related in some way to the input signal 10. An updating means (not shown) then applies an update value 30 to each of the RAMs 18 so that the next time the same data is present in the input store a substantially correct total estimate will be returned. The updating means also allows variations in the dependence of the received value on the input signal to be accounted for by amending the partial responses 20 when the received value 24 differs from that expected based on the input signal 10 and the partial responses corresponding to it which are already stored in the RAMs 18. The way in which the updating means calculates the update value 30 must be appropriate though to the way in which the device 22 derives the common value so that the device will adapt correctly.

Preferably the partial responses 20 are summed by summing means 22 and the total 26 subtracted 23 from the received value 24 of which the total estimate 26 is an estimate. The subtraction 23 yields the corrected value 28 which is also used to provide the update value 30 for the RAM address locations which provided the partial responses 20. Since the words held in the RAM addresses are summed by the summing means 22 either the total estimate 26 or the corrected value 28 must be divided by the total number of RAMs 18 used to prevent a wrongly scaled update value 30 being applied to the RAM addresses to be updated. Preferably the update value is added to the contents of each address to be updated. Other means for deriving an update value may be used as appropriate though, for example a fraction of the error may be returned or only a sign bit. In such cases adaption will be slower though.

By connecting directly or indirectly the line 14 to the received value input 24 a particularly useful set of uses of the device can be realised. The device will, when a signal 10 is input to it, learn to recognise the signal

and return a total estimate which will be the same or nearly the same as the received value 24 corresponding to the input signal 10. Subsequent variations in the relationship between the input signal and received value will be adjusted for by the device due to the adaptive nature of the device. Furthermore faults in the device for example in one of the blocks of RAM will be adjusted for by the device too since the other RAMs will compensate for the error when they are updated.

By interrupting the updating of the RAM after learning has occurred the device can be used to recognise only those signals on which it has been trained and if the total estimate value for all other signals is made zero the corrected value 28 will only be other than the received value 24 for those input signals 10 comprising signals on which the device has been trained. The device can thus be used in effect as a trainable filter or input signal pattern detector.

A further advantage of the system is that no multiplications are necessary. When used as an echo canceller this gives the device a definite advantage over F.I.R. cancellers which have to perform many such calculations.

The device also has the advantage of being able to associate a value comprising a plurality of bits with a particular response for each of the RAMs.

The use of RAMs having only one or two addresses gives a great saving in memory requirement in comparison with prior art devices.

Figure 3 shows a further embodiment of the present invention in diagrammatic form. In this embodiment each RAM is provided with additional memory locations and additional address lines the latter of which are distributed randomly over the input store. Linked to individual cells of the input store 30 are a plurality of address lines arranged in groups 32. Each of these lines senses the contents of a particular input store cell and each group of lines forms the address lines for a respective block of RAM 34. The groups of lines may be of any size from 1 upwards. Preferably though the number is kept relatively small so that the number of addresses per block of RAM which can be addressed is kept within practical limits. Since the number of lines per RAM may typically be only 8 the number of addresses per RAM will only be 2^8 . Thus the size of RAM required is also considerably reduced compared to the prior art whilst the number of input store cells remains the same. For example in Figure 3 128 input store cells are shown which using the construction of Figure 1 would require a RAM with 2^{128} addresses. Using the construction of Figure 2 RAMs with only 2^8 addresses are required and whilst more than one of these is used the total memory requirement is still considerably reduced. At the same time the random distribution of the address lines enables the modelling of many different waveforms and particularly non-linearities which prior art devices could not.

The connections of different lines may also be to identical cells. The number of such groups of lines 32 and thus the number of RAMs 34 may take any suitable number, typically this might be such that there are as many address lines as input store cells but a lesser or greater number may be used.

The groups of address lines 32 each specify an address in a corresponding RAM 34 corresponding to the contents of the input store 30 and the location of the address lines 32 among the store cells. At each of the RAM store locations a word is stored indicating a partial response to the input store contents. These partial responses are summed to produce a total estimate which in conjunction with a received value is used to produce a corrected value and an update value in the same way as is shown in Figure 2.

The use of a larger number of address lines increases the devices ability to model non-linearities but at the same time increases the memory requirement. In Figure 4 a further embodiment of the device according to the present invention is shown which comprises a plurality of input stores connected in series 42, 43, 44. These are each connected to a plurality of corresponding series of RAMs 46, 48, 50 by a plurality of address lines in a similar manner to those 16, 32 shown in either Figures 2 or 3. Each of the RAMs in the series of RAMs 46, 48, 50 output a stored partial estimate in response to the address generated by the contents of its appropriate input store. For each of the series of RAMs 46, 48, 50 the partial responses are summed by summing means 52, divided 54 by the number of RAMs in the respective series to produce an average estimate value for each of the series of RAMs. The average values are then summed in summing means 56 and divided 58 by the number of series of RAM to produce an average of the average values as an estimate value 60. The estimate value obtained in this way is then used together with a received value 62 to produce a corrected value 64 from which is derived an update value 66 for application to the RAMs 46, 48, 50 in a similar manner to the update value in Figures 2 or 3. In this manner a global error update value is applied to the RAMs used.

In Figures 5 and 6 diagrammatic views of the disposition of analogue to digital (A/D) and digital to analogue (D/A) converters are shown for use of the circuits shown in Figures 2, 3 or 4 as echo cancellers using linearly coded input signals. In Figure 5 the subtraction of the estimate signal from the echo signal is performed by an analogue subtractor 68 whereas in Figure 6 the subtraction is performed by a digital subtractor 70. In each case the corrected value forms the echo cancelled signal 72, the echo forms the received value 74, and the transmitted signal forms the input signal 76. However, the configuration shown in Figure 5 is preferred due to the delays caused to updating by the configuration shown in Figure 6 in certain circumstances.

Figure 7 shows in diagrammatic form an embodiment of the present invention being used as an echo canceller in a telephone circuit using A-law words showing where linearisation of the signal is required. The same need for linearisation arises when μ law words or any other non-linearly coded words are used. This is particularly relevant when the present invention is to be used in a telephone circuit where A-law or μ law words are being used. In Figure 7 the input signal 80 is fed to an input shift register 81. Conventional A/D and D/A converters 82, 84 connected to a hybrid 86 are provided. However since the digital words being input to the echo canceller are non-linearly coded it is necessary to surround the estimate subtractor 92 (which may form part of the device as shown in either of Figures 2, 3 or 4) with linearisers for converting coded words to linear words and vice versa so that the subtraction of the estimate value from the received value can be performed on linearly coded values. However with the present invention there is no need for the input to the input shift register to be linearised since a device according to the present invention will "recognise" the input irrespective of its coding and produce an appropriate linear estimate.

Using an arrangement as shown in Figure 7 in conjunction with the arrangements shown in Figures 2, 3 or 4 enables non-linearly coded input signals to be used without the need for a lineariser on the input to the input shift register unlike many prior art echo-cancellers which do need a preliminary linearisation step before any cancellation can occur. However it is possible to use a vertical arrangement of the RAM address lines which uses fewer address lines per RAM than there are bits in the words of the input signal and yet still achieves as good a result as if for example eight address lines per RAM were used when dealing with A law or μ law coded words. One such arrangement is shown in Figure 8.

In Figure 8 an input A or μ law coded signal is fed not only to a hybrid (not shown) but also to an input shift register 102. For the sake of clarity only four stages of the shift register are shown but any suitable number may be used as with the arrangements shown in Figures 2 or 3. Each stage 104 of the shift register 102 comprises eight cells, one for a sign bit, three for exponent bits and four for mantissa bits. The shift register thus comprises an eight bit parallel shift register. Four RAMs 106, 107, 108, 109 are connected to each of the stages 104 by only five address lines each. In the case of each RAM four of the address lines are taken from the cells containing the sign bit and the three exponent bits in each stage. The fifth address line in the case of each RAM is taken from one of the mantissa cells of the corresponding stage. The values at the locations in each RAM specified by the word in the stage are summed for each set of four RAMs corresponding to a stage in the shift register by adders 110 to form partial responses. These are in turn summed to form a total estimate. The individual adders 110 may alternatively be dispensed with and the outputs from each RAM summed together directly. In either case the total estimate is then subtracted from a received value 112 by a subtractor 114 to give a corrected value 116 and an update value 118 in the same manner as that shown in Figures 2, 3 or 4. Suitable normalising means should of course be used to ensure that the correct update value is applied to the RAM locations. One of the main advantages of this arrangement is the saving in memory it gives in comparison with using one eight address line RAM per shift register stage. For a sixteen stage shift register such an arrangement would require sixteen 2^8 address RAMs whereas using an arrangement as shown in Figure 8 would only require sixty four 2^5 address RAMs, a saving of 2048 bits of memory. Despite this reduction in memory the device is still able to function and has a greater adaption speed than one having the larger memory requirement.

In Figure 9 a further variant of the arrangement shown in Figure 8 is shown. For the sake of clarity only one of the shift register stages 120 is shown the others and their associated RAMs being identical. In this case there are five RAMs per shift register stage. Four are four address line RAMs 122, 124, 126, 128. The other is a two address RAM 130 whose single address line is supplied by the sign bit cell of the associated shift register stage. The four address lines for each of the other RAMs are taken from the three exponent bit cells and one of the four mantissa bit cells in each case. The outputs from all five RAMs are summed by an adder 132 there being one such adder per shift register stage. Alternatively the outputs from each RAM may be summed directly. A further alternative arrangement is for the two address sign bit RAM to be omitted altogether and the sign bit used to control an inverter 134 on the output of the corresponding adder 132. Both arrangements can be incorporated in the same device by use of a suitable switch 136. Once the total estimate 138 has been obtained it is subtracted from the received values to give an update value 140 and a corrected value 142 in the same way as with the arrangements shown in Figures 2, 3, 4 or 8.

Such an arrangement gives an even greater saving in memory since it only requires sixty four 2^4 address RAMs with an optional two address RAM for the sign bit.

Claims

1. An electronic adaptive recognising device comprising: an input (10) connected to an input store (12) hav-



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In Figure 8 an input A or μ law coded signal is fed not only to a hybrid (not shown) but also to an input shift register 102. For the sake of clarity only four stages of the shift register are shown but any suitable number may be used as with the arrangements shown in Figures 2 or 3. Each stage 104 of the shift register 102 comprises eight cells, one for a sign bit, three for exponent bits and four for mantissa bits. The shift register thus comprises an eight bit parallel shift register. Four RAMs 106, 107, 108, 109 are connected to each of the stages 104 by only five address lines each. In the case of each RAM four of the address lines are taken from the cells containing the sign bit and the three exponent bits in each stage. The fifth address line in the case of each RAM is taken from one of the mantissa cells of the corresponding stage. The values at the locations in each RAM specified by the word in the stage are summed for each set of four RAMs corresponding to a stage in the shift register by adders 110 to form partial responses. These are in turn summed to form a total estimate. The individual adders 110 may alternatively be dispensed with and the outputs from each RAM summed together directly. In either case the total estimate is then subtracted from a received value 112 by a subtractor 114 to give a corrected value 116 and an update value 118 in the same manner as that shown in Figures 2, 3 or 4. Suitable normalising means should of course be used to ensure that the correct update value is applied to the RAM locations. One of the main advantages of this arrangement is the saving in memory it gives in comparison with using one eight address line RAM per shift register stage. For a sixteen stage shift register such an arrangement would require sixteen 2^8 address RAMs whereas using an arrangement as shown in Figure 8 would only require sixty four 2^5 address RAMs, a saving of 2048 bits of memory. Despite this reduction in memory the device is still able to function and has a greater adaption speed than one having the larger memory requirement.

In Figure 9 a further variant of the arrangement shown in Figure 8 is shown. For the sake of clarity only one of the shift register stages 120 is shown the others and their associated RAMs being identical. In this case there are five RAMs per shift register stage. Four are four address line RAMs 122, 124, 126, 128. The other is a two address RAM 130 whose single address line is supplied by the sign bit cell of the associated shift register stage. The four address lines for each of the other RAMs are taken from the three exponent bit cells and one of the four mantissa bit cells in each case. The outputs from all five RAMs are summed by an adder 132 there being one such adder per shift register stage. Alternatively the outputs from each RAM may be summed directly. A further alternative arrangement is for the two address sign bit RAM to be omitted altogether and the sign bit used to control an inverter 134 on the output of the corresponding adder 132. Both arrangements can be incorporated in the same device by use of a suitable switch 136. Once the total estimate 138 has been obtained it is subtracted from the received values to give an update value 140 and a corrected value 142 in the same way as with the arrangements shown in Figures 2, 3, 4 or 8.

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Claims

1. An electronic adaptive recognising device comprising: an input (10) connected to an input store (12) hav-



- ing a plurality of storage locations allowing data representative of elements of a signal pattern to be recognised to be stored at locations related to the positions of the elements in the pattern; a plurality of addressable stores (18) each having a plurality of address lines (16) specifying locations therein, each of the said addressable store locations being capable of containing a word of at least one bit, the address lines (16) each being connected to a respective location in the input store (12) such that the contents of said input store (12) are capable of specifying a store location in each of the addressable stores (18); means (22) for deriving a common value (26) dependent on the contents of the store locations specified by the contents of the input store (12); an input for received values (24); calculating means (23) for calculating a value (28) dependent on the common value (26) and a corresponding one of the received values (24); and updating means for applying an update value (30) dependent on said calculated value (28) to the contents of the specified store locations; characterised in that the address lines (16) are connected in a random manner to the locations of the input store (12).
2. A recognizing device according to claim 1, wherein the number of address lines (16) per store is smaller than the number of bits each word of said input data contains.
 3. An electronic adaptive recognising device comprising: an input connected (1) to an input store (12) having a plurality of storage locations allowing data representative of elements of a signal pattern to be recognised to be stored at locations related to the positions of the elements in said pattern; a plurality of addressable stores (18) each having an address line (16) specifying one or more store locations therein, each of said addressable store locations being capable of containing a word of at least one bit, said address lines (16) each being connected to a respective location in said input store (12) such that the contents of said input store (12) are capable of specifying a store location in each of said addressable stores (18); means (22) for deriving a common value (26) dependent on the contents of the store locations specified by the contents of said input store (12); an input for received values (24); calculating means (23) for calculating a value dependent on said common value (26) and a corresponding one of said received values and updating means for applying an update value (30) dependent on said calculated value (28) to the contents of said specified store locations, characterised in that each of the addressable stores (18) has only one address line (16) and not more than two store locations.
 4. A recognizing device according to any one of the preceding claims characterised in that more than one address line (16) is connected to a single input store location.
 5. A recognising device according to any one of the preceding claims, characterised in that the common value (26) is the sum of the contents of the store locations specified by the contents of the input store (12).
 6. A recognising device according to claim 5, characterised in that the calculating means (23) is arranged to obtain the said calculated value (28) by subtracting, from a corresponding one of the received values (24), the said sum divided by the number of addressable stores.
 7. A recognising device according to claim 5 or claim 6, characterised in that the calculating means (23) are arranged to obtain the said calculated value (28) by subtracting the said sum from a corresponding one of the received values (24) and that the updating means is arranged to divide the calculated value by the number of addressable stores, to provide the update value (30).
 8. A recognising device according to any one of the preceding claims wherein the updating means are arranged to add the update value (30) to the contents of each of the specified store locations.
 9. A recognizing device according to any one of the preceding claims, characterised in that it further comprises means for selectively operating the device according to a predetermined sequence in either a recognition or an updating mode wherein in the recognition mode calculated values (28) are output and in the update mode the updating means applies the update value (30) to the contents of each of the addressable store locations.
 10. A recognising device according to any one of the preceding claims, characterised in that the input store (12) comprises a shift register into which data forming a signal pattern to be recognised may be fed and the addressable stores (18) have identical values written in locations corresponding to a plurality of positions of the signal pattern in the shift register such that the signal pattern may be subsequently recognised independently of its position in the input store (12).



11. An echo canceller comprising an adaptive recognizing device according to any one of the preceding claims for use with a transmitter/receiver unit wherein the transmitter output is also applied to the device input, the receiver is connected to receive the calculated values (28) and the input for received values (24) is supplied with a signal to be received by the receiver such that portions of the signal to be received by the receiver which are derived from signals transmitted by the transmitter are cancelled.
12. A digital filter comprising an adaptive recognising device according to any one of claims 1 to 10 wherein means are provided for disabling the updating means after supplying the signal to be filtered to the input (1), the input (1) also being connected to the input for received values (24).

Patentansprüche

1. Elektronische, adaptive Erkennungseinrichtung mit einem Eingang (10), der mit einem Eingangsspeicher (12) mit mehreren Speicherstellen verbunden ist, die es erlauben Daten zu speichern, welche für Elemente einer zu erkennenden Signalstruktur repräsentativ sind, an Stellen, die den Positionen der Elemente in der Struktur entsprechen, mehreren adressierbaren Speichern (18) mit mehreren Adreßleitungen (16), die die Stellen in den Speichern spezifizieren, wobei jede der adressierbaren Speicherstellen ein Wort von zumindest einem Bit enthalten kann und jede der Eingangsleitungen (16) mit einer entsprechenden Stelle in dem Eingangsspeicher (12) derart verbunden werden kann, daß die Inhalte des Eingangsspeichers (12) eine Speicherstelle in jedem der adressierbaren Speicher (18) spezifizieren können, Mitteln (22) zum Erhalten eines gemeinsamen Werts (26), abhängig von den Inhalten der Speicherstellen, die durch die Inhalte des Eingangsspeichers (12) spezifiziert sind, einem Eingang für die erhaltenen Werte (24), Berechnungsmitteln (23) für die Berechnung eines Werts (28), abhängig von dem gemeinsamen Wert (26) und einem entsprechenden von den erhaltenen Werten (24) und Fortschreibungsmitteln zum Anwenden eines Fortschreibungswerts (30), abhängig von dem berechneten Wert (28), auf die Inhalte der spezifizierten Speicherbereiche, **dadurch gekennzeichnet, daß** die Adreßleitungen (16) auf eine zufällige Weise mit den Bereichen des Eingangsspeichers (12) verbunden sind.
2. Erkennungseinrichtung nach Anspruch 1, in der die Anzahl der Adreßleitungen (16) pro Speicher kleiner ist, als die Anzahl der Bits von jedem Wort, welches die Eingangsdaten enthält.
3. Elektronische, adaptive Erkennungseinrichtung mit einem Eingang (1), der mit einem Eingangsspeicher (12) verbunden ist, der mehrere Speicherstellen aufweist, zum Erlauben, daß Daten, die Elementen einer zu erkennenden Signalstruktur entsprechen, an Stellen gespeichert werden, die den Positionen der Elemente in der Struktur entsprechen, mehreren adressierbaren Speichern (18), die jeder eine Adreßleitung (16) aufweisen, welche eine oder mehrere Speicherstellen in dem Speicher spezifizieren, wobei jede der adressierbaren Speicherstellen ein Wort von zumindest einem Bit enthalten kann und jede der Adreßleitungen (16) mit einer entsprechenden Stelle in dem Eingangsspeicher (12) derart verbunden ist, daß die Inhalte des Eingangsspeichers (12) eine Speicherstelle in jedem der adressierbaren Speicher (18) spezifizieren können, Mitteln (22) zum Erhalten eines gemeinsamen Werts (26), abhängig von den Inhalten der Speicherstellen, die durch die Inhalte des Eingangsspeichers (12) spezifiziert sind, einem Eingang für erhaltene Werte (24), Berechnungsmitteln (23) zum Berechnen eines von dem gemeinsamen Wert (26) abhängigen Werts und einen entsprechenden der erhaltenen Werte und Fortschreibungsmittel zum Anwenden eines fortgeschriebenen Werts (30), abhängig von dem berechneten Wert (28), auf die Inhalte der spezifizierten Speicherstellen, **dadurch gekennzeichnet, daß** jeder der adressierbaren Speicher (18) nur eine Adreßleitung (16) und nicht mehr als zwei Speicherstellen aufweist.
4. Erkennungseinrichtung nach einem der vorangehenden Ansprüche, **dadurch gekennzeichnet, daß** mehr als eine Adreßleitung (16) mit einer einzelnen Eingangsspeicherstelle verbunden ist.
5. Erkennungseinrichtung nach einem der vorangehenden Ansprüche, **dadurch gekennzeichnet, daß**



der gemeinsame Wert (26) die Summe der Inhalte der Speicherstellen ist, die durch die Inhalte des Eingangsspeichers (12) spezifiziert ist.

- 5 6. Erkennungseinrichtung nach Anspruch 5,
dadurch gekennzeichnet, daß
die Berechnungsmittel (23) zum Erhalten des berechneten Werts durch Subtraktion angeordnet sind, von
einem entsprechenden der erhaltenen Werte (24), wobei die Summe durch die Anzahl der adressierbaren
Speicher dividiert wird.
- 10 7. Erkennungseinrichtung nach Anspruch 5 oder 6,
dadurch gekennzeichnet, daß
die Berechnungsmittel (23) zum Erhalten des berechneten Werts (28) durch Subtrahieren der Summe
von einem entsprechenden der erhaltenen Werte (24) angeordnet sind und die Fortschreibungsmittel zum
Teilen des berechneten Werts durch die Anzahl der adressierbaren Speicher angeordnet sind, zum Er-
halten des fortgeschriebenen Werts (30).
- 15 8. Erkennungseinrichtung nach einem der vorangehenden Ansprüche, in der die Fortschreibungsmittel zum
Addieren des fortgeschriebenen Werts (30) zu den Inhalten jeder der spezifizierten Speicherstellen an-
geordnet sind.
- 20 9. Erkennungseinrichtung nach einem der vorangehenden Ansprüche,
dadurch gekennzeichnet, daß
sie ferner Mittel zum selektiven Betreiben der Einheit entsprechend einer vorbestimmten Sequenz ent-
weder in einem Erkennungs- oder in einem Fortschreibungsmodus enthält, wobei in dem Erkennungs-
modus berechnete Werte (28) ausgegeben werden und in dem Fortschreibungsmodus die Fortschrei-
bungsmittel den fortgeschriebenen Wert (30) auf die Inhalte jeder der adressierbaren Speicherstellen an-
wenden.
- 25 10. Erkennungseinrichtung nach einem der vorangehenden Ansprüche,
dadurch gekennzeichnet, daß
der Eingangsspeicher (12) ein Verschieberegister enthält, dem Daten zugeführt werden können, welche
eine zu erkennende Signalstruktur bilden, wobei die adressierbaren Speicher (18) identische Werte auf-
weisen, welche in Stellen geschrieben sind, die mehreren Positionen der Signalstruktur in dem Verschie-
beregister derart entsprechen, daß die Signalstruktur nachfolgend unabhängig von deren Position in dem
Eingangsspeicher (12) erkannt werden kann.
- 30 11. Echokompensator mit einer adaptiven Erkennungseinheit nach einem der vorangehenden Ansprüche zur
Verwendung mit einer Sende-/Empfangeinheit, wobei der Senderausgang dem Einrichtungseingang auf-
gegeben wird und der Empfänger ist zum Empfangen der berechneten Werte (28) verbunden, weiterhin
wird dem Eingang für erhaltene Werte (24) ein durch den Empfänger zu empfangendes Signal derart zu-
geführt, daß Teile des von dem Empfänger zu empfangenden Signals, welches von durch den Sender
übertragene Signale abgeleitet ist, gelöscht werden.
- 35 12. Digitalfilter mit einer adaptiven Erkennungseinheit gemäß einem der Ansprüche 1 bis 10, in dem Mittel
zum Sperren der Fortschreibungsmittel nach dem Zuführen des durch den Eingang (1) zu filternden Si-
gnals vorgesehen sind, wobei der Eingang (1) auch mit dem Eingang für empfangene Werte (24) verbun-
den ist.
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Revendications

- 50 1. Dispositif de reconnaissance adaptatif électronique comprenant : une entrée (10) reliée à un dispositif
de mémorisation d'entrée (12) comportant une pluralité d'emplacements de mémorisation permettant à
des données représentatives d'éléments d'une configuration de signal à reconnaître d'être mémorisées
à des emplacements se rapportant aux positions des éléments dans la configuration, une pluralité de dis-
positifs de mémorisation adressables (18) comportant chacun une pluralité de lignes d'adresse (16) spé-
cifiant les emplacements dans ceux-ci, chacun desdits emplacements de mémorisation adressables
55 étant capable de contenir un mot d'au moins un bit, les lignes d'adresse (16) chacune étant reliée à un
emplacement respectif dans le dispositif de mémorisation d'entrée (12) de sorte que le contenu dudit dis-



- positif de mémorisation d'entrée (12) soit capable de spécifier un emplacement de mémorisation dans chacun des dispositifs de mémorisation adressables (18), un moyen (22) pour obtenir une valeur commune (26) fonction du contenu des emplacements de mémorisation spécifiés par le contenu du dispositif de mémorisation d'entrée (12), une entrée pour les valeurs reçues (24), un moyen de calcul (23) pour calculer la valeur (28) fonction de la valeur commune (26) et d'une valeur correspondante parmi les valeurs reçues (24) et un moyen de mise à jour pour appliquer une valeur de mise à jour (30) fonction de ladite valeur calculée (28) au contenu des emplacements de mémorisation spécifiés caractérisé en ce que les lignes d'adresses (16) sont reliées de manière aléatoire aux emplacements du dispositif de mémorisation d'entrée (12).
2. Dispositif de reconnaissance selon la revendication 1, dans lequel le nombre de lignes d'adresse (16) par dispositif de mémorisation est inférieur au nombre de bits que chaque mot desdites données d'entrée contient.
3. Dispositif de reconnaissance adaptatif électronique comprenant : une entrée (1) reliée à un dispositif de mémorisation d'entrée (12) comportant une pluralité d'emplacements de mémorisation permettant à des données représentatives d'éléments d'une configuration de signal à reconnaître d'être mémorisées à des emplacements se rapportant aux positions des éléments dans ladite configuration, une pluralité de dispositifs de mémorisation adressables (18) comportant chacun une ligne d'adresse (16) spécifiant un ou plusieurs emplacements de mémorisation dans ceux-ci, chacun desdits emplacements de mémorisation adressables étant capable de contenir un mot d'au moins un bit, lesdites ligne d'adresse (16) étant chacune reliée à un emplacement respectif dans ledit dispositif de mémorisation d'entrée (12), de sorte que le contenu dudit dispositif de mémorisation d'entrée (12) soit capable de spécifier un emplacement de mémorisation dans chacun desdits dispositifs de mémorisation adressables (18), un moyen (22) pour obtenir une valeur commune (26) fonction du contenu des emplacements de mémorisation spécifiés par le contenu dudit dispositif de mémorisation d'entrée (12), une entrée pour les valeurs reçues (24), un moyen de calcul (23) pour calculer une valeur fonction de ladite valeur commune (26) et une valeur correspondante parmi lesdites valeurs reçues et un moyen de mise à jour pour appliquer une valeur de mise à jour (30) fonction de ladite valeur calculée (28) au contenu desdits emplacements de mémorisation spécifiés, caractérisé en ce que chacun des dispositifs de mémorisation adressables (18) comprend seulement une ligne d'adresse (16) et pas plus de deux emplacements de mémorisation.
4. Dispositif de reconnaissance selon l'une quelconque des revendications précédentes, caractérisé en ce que plus d'une ligne d'adresse (16) est reliée à un emplacement de mémorisation d'entrée unique.
5. Dispositif de reconnaissance selon l'une quelconque des revendications précédentes, caractérisé en ce que la valeur commune (26) est la somme du contenu des emplacements de mémorisation spécifiés par le contenu du dispositif de mémorisation d'entrée (12).
6. Dispositif de reconnaissance selon la revendication 5, caractérisé en ce que le moyen de calcul (23) est disposé afin d'obtenir ladite valeur calculée (28) en soustrayant, à partir d'une valeur correspondante parmi les valeurs reçues (24), ladite somme divisée par le nombre de dispositifs de mémorisation adressables.
7. Dispositif de reconnaissance selon la revendication 5 ou la revendication 6, caractérisé en ce que les moyens de calcul (23) sont disposés afin d'obtenir ladite valeur calculée (28) en soustrayant ladite somme à partir d'une valeur correspondante des valeurs reçues (24) et en ce que le moyen de mise à jour est disposé afin de diviser la valeur calculée par le nombre de dispositifs de mémorisation adressables, afin de procurer la valeur de mise à jour (30).
8. Dispositif de reconnaissance selon l'une quelconque des revendications précédentes, dans lequel les moyens de mise à jour sont disposés pour ajouter la valeur de mise à jour (30) au contenu de chacun des emplacements de mémorisation spécifiés.
9. Dispositif de reconnaissance selon l'une quelconque des revendications précédentes, caractérisé en ce qu'il comprend de plus un moyen pour faire fonctionner le dispositif de manière sélective conformément à une séquence prédéterminée soit en mode de reconnaissance, soit en mode de mise à jour dans lequel dans le mode de reconnaissance les valeurs calculées (28) sont sorties et dans le mode de mise à jour, le moyen de mise à jour applique la valeur de mise à jour (30) au contenu de chacun des emplacements



de mémorisation adressables.

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10. Dispositif de reconnaissance selon l'une quelconque des revendications précédentes caractérisé en ce que le dispositif de mémorisation d'entrée (12) comprend un registre à décalage dans lequel les données formant une configuration de signal qui doit être reconnu peuvent être délivrées et les dispositifs de mémorisation adressables (18) comportent des valeurs identiques écrites dans les emplacements correspondants à une pluralité de positions de la configuration de signal dans le registre à décalage, de sorte que la configuration de signal puisse être reconnue par la suite indépendamment de sa position dans le dispositif de mémorisation d'entrée (12).
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11. Dispositif d'annulation d'écho comprenant un dispositif de reconnaissance adaptatif conformément à l'une quelconque des revendications précédentes pour utilisation avec une unité d'émetteur/récepteur dans laquelle la sortie d'émetteur est également appliquée à l'entrée du dispositif, le récepteur est relié afin de recevoir les valeurs calculées (28) et l'entrée pour les valeurs reçues (24) reçoit un signal qui doit être reçu par le récepteur, tel que des parties du signal qui doit être reçu par le récepteur qui sont obtenues à partir de signaux émis par l'émetteur soient annulées.
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12. Filtre numérique comprenant un dispositif de reconnaissance adaptatif selon l'une quelconque des revendications 1 à 10, dans lequel des moyens sont prévus pour désactiver le moyen de mise à jour après délivrance du signal filtré à l'entrée (1), l'entrée (1) étant également reliée à l'entrée pour les valeurs reçues (24).
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