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1 Image Processing Apparatus

BACKGROUND OF THE INVENTIONField of the Invention

5 The present invention relates to an image processing apparatus, and more particularly to an image processing apparatus equipped with image decoding means which has a function of expanding compressed image data, for example.

10 Related Background Art

 Conventionally, there is known a technique for transmitting image data after performing a frequency transform (transformation) of image data for each block to make data compression. In
15 particular, by separating frequency components into a high-frequency component and a low-frequency component and encoding those components separately from each other, compression efficiency of images is increased.

20 However, the above prior art has had a disadvantage that if an error occurs during transmission of encoded data, an image signal including false image data is reproduced and image quality deteriorates remarkably. In the case of using a
25 variable-length code in encoding the above high-frequency component, it may sometimes happen that even the number of data is not reproduced accurately

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1 and a quite gross deterioration of image quality
such as missing of image data occurs.

Meanwhile, in the field of transmitting images
in the digital form, there have also conventionally
5 been proposed a variety of encoding methods for
cutting down the quantity of information before
transmitting images because the quantity of
information is very large.

Among them, there is known a method of carrying
10 out an orthogonal transform, quantizing a coefficient
after the transform, and forming a variable-length
code.

With the above-mentioned prior art including
no error detecting means, however, if an error
15 occurs in a transmission path, such an error cannot be
corrected, leading to a gross deterioration of image
quality.

Especially, in the event of exceeding a
dynamic range capable of decoding and reproducing
20 when encoded data after transmission is decoded, for
example, image quality deteriorates.

Moreover, in an image transmission system of
the type that a moving image signal is digitized and
image data is transmitted via transmission paths such
25 as optical fibers or communication satellites and
recording media such as magnetic tapes, an error
correcting code (ECC) for detecting and correcting a

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1 transmission error is utilized to correct the
transmission error in the reception side (or the
reproduction side) based on the error correcting
code. That error which cannot be corrected by using
5 the error correcting code is subjected to interpolation
processing to form an approximate value from surround-
ing pixels.

In order to avoid a deterioration of image
quality caused by the interpolation processing, it
10 is required that the surrounding pixels utilized for
the interpolation are free from errors. When adopting
highly efficient encoding (image compression) which
has been widely used in recent years, the surrounding
pixels capable of being utilized for the interpolation
15 are restricted. In a DPCM (difference pulse code
modulation) method that reset is made for each line,
for example, if a correction impossible error occurs,
the original data cannot be reproduced by using the
line inclusive of the error. Accordingly, only those
20 pixels which are included in the upper and lower
lines can be utilized for interpolation in this case.
Further, in an encoding method that uses an orthogonal
transform such as a discrete cosine transform (DCT),
if a correction impossible error occurs, all the
25 pixels included in a transmission block (e.g., 8
pixels vertical x 8 pixels horizontal) cannot be
used to reproduce the original signal. As a result,

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1 a deterioration of image quality cannot be prevented
even by the interpolation using the upper and lower
lines.

Thus, even in an attempt of performing the
5 interpolation in the same frame, no effect may be
expected depending on the coding methods.

Additionally, in the field of transmitting
information such as images and voices in the digital
form, there have been proposed various encoding
10 methods for cutting down the amount of data trans-
mitted. One known run-length coding method is to
encode data by combining the number of successive 0s
and a value other than 0 into a set. On the other
hand, a forecast difference encoding method or a
15 difference pulse code modulation (hereinafter referred
to as DPCM) encoding method is also known which
compresses information by utilizing correlation
between sample values close to each other. There is
further known an encoding method that the above two
20 methods are combined with each other. Fig. 14 is
a block diagram showing the encoding method in a
combination of the two methods. Image data of 8
bits inputted through an input terminal 611 is applied
to a DPCM encoder 613 for DPCM encoding into 4 bits.
Specifically, the DPCM encoder 613 assigns DPCM codes
25 of 4 bits to respective difference values as shown
in Table 1 below.

1

Table 1

	Range of Difference Values	DPCM Code	Representative Value of Difference
	-255 ~ -94	15	-140
	-93 ~ -70	13	-80
5	-69 ~ -50	11	-58
	-49 ~ -34	9	-40
	-33 ~ -22	7	-27
	-21 ~ -13	5	-17
	-12 ~ -6	3	-8
	-5 ~ -2	1	-3
10	-1 ~ 1	0	0
	2 ~ 5	2	3
	6 ~ 11	4	8
	12 ~ 20	6	15
	21 ~ 35	8	27
	36 ~ 53	10	44
15	54 ~ 93	12	70
	94 ~ 255	14	150

An image generally has correlation between sample values close to each other such that many difference signals occur as 0 and many DPCM codes occur as 0. The DPCM codes encoded into 4 bits are outputted to a run-length encoder 615. As shown in Fig. 15A, the run-length encoder 615 combines the DPCM code other than 0 and the number of successive 0s (hereinafter referred to as a 0 run-length) before the DPCM code into a set for each DPCM code of 4 bits.

At this time, by limiting the 0 run-length

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1 to 16 at maximum, the run-length codes can be each
expressed in 8 bits. The 8-bit run-length codes
thus encoded by the run-length encoder 615 are
added with a reset synch bit in a transmission format
5 unit 617 as shown in Fig. 15B and then delivered to
an output terminal. The reset synch bit is added,
for example, after processing of each line.

Fig. 13 is a block diagram showing a
configuration of a decoder device in cooperation with
10 the encoding section of Fig. 14. The run-length code
and the reset synch bit both transmitted through a
transmission path are applied to an input terminal
621, and a run-length decoder 623 decodes the DPCM
code by inserting 0s in the number corresponding to
15 the 0 run-length before each DPCM code until arrival
of the reset synch bit. The data decoded to the
DPCM code is outputted to a DPCM decoder 625 for
decoding to image data of 8 bits, which are then
delivered to an output terminal 627.

20 With the above conventional method, however,
if an error occurs in a transmission path, such an
error cannot be corrected and image quality deterio-
rates remarkably because of including no error
detecting means.

25 As mentioned before, in the field of trans-
mitting information such as images and voices in the
digital form, there have been proposed various encoding

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1 methods for cutting down the amount of data
transmitted. One known run-length coding method is
to encode data by combining the number of successive
0s and a value other than 0 into a set. On the other
5 hand, a transform encoding method is also known
which performs an orthogonal transform of pixels to
be transmitted and quantizes transmitted data. There
is further known an encoding method that the above
two methods are combined with each other.

10 With the above conventional methods, however,
if an error occurs in a transmission path, such an
error cannot be corrected and image quality deterio-
rates remarkably because of including no error
detecting means.

15 Meanwhile, U.S. Patent No. 5,023,919 has been
proposed with an intention to correct or avoid a
deterioration on the side decoding compressed data,
but has not yet succeeded in sufficiently solving the
problem.

20

SUMMARY OF THE INVENTION

The present invention has been made in view
of the situations in the prior art as set forth
above, and its object is to provide an image process-
25 ing apparatus which can satisfactorily control the
amount of compressed data.

To achieve the above object, in accordance

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1 with the present invention, there is disclosed an
image processing apparatus comprising, receiving
means for receiving encoded image data which is
encoded by using orthogonal transform in a
5 predetermined block unit, error detecting means for
detecting a transmission error of the encoded image
data, correcting means for correcting the trans-
mission error in the predetermined block unit, and
decoding means for decoding the encoded image data
10 and outputting image data for reproducing an image.

Another object of the present invention is
to output a moving picture of high quality.

To achieve the above object, in accordance
with the present invention, there is disclosed a
15 moving picture processing apparatus comprising
receiving means for receiving a plurality of pictures
of encoded image data sequentially which is encoded
by using orthogonal transform in a predetermined
block unit, error detecting means for detecting a
20 transmission error of one of the plurality of pictures,
correcting means for correcting the transmission
error by using encoded image data of another picture,
and decoding means for decoding the encoded image
data and outputting a plurality of pictures of image
25 data sequentially for reproducing an image.

Still another object of the present invention
is to improve a decoding method of encoded data which

1 in encoded by run-length encoding. To achieve the
above object, in accordance with the present invention,
there is disclosed an image processing apparatus
comprising receiving means for receiving an encoded
5 orthogonal transform coefficient which is encoded
by using run-length encoding method, decoding means
for decoding the encoded orthogonal transform co-
efficient, error detecting means for detecting a
transmission error of the encoded orthogonal transform
10 coefficient based on the orthogonal transform
coefficient, and correcting means for correcting the
transmission error of the decoded orthogonal transform
coefficient.

Still another object of the present invention
15 is to improve an encoding method. To achieve the
above object, in accordance with the present invention,
there is disclosed an image processing apparatus
comprising input means for inputting image data,
transforming means for performing an orthogonal
20 transform on the input image data, extracting means
for extracting DC component and AC component from the
transformed image data, adding means for adding data
for error detection to at least one of the DC component
and the AC component, and encoding means for encoding
25 the DC component and the AC component.

Other objects and forms of the present
invention will be apparent from the following

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1 explanation with reference to the drawings and the
description in the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

5 Fig. 1 is a block diagram showing a configuration of a first embodiment of the present invention.

Fig. 2 is a diagram showing one example of a data transmission format.

10 Fig. 3 is a block diagram showing a configuration of a second embodiment of the present invention.

Fig. 4 is a block diagram showing a configuration of a third embodiment of the present invention.

15 Fig. 5 is a block diagram showing a configuration of a decoding device in a fourth embodiment of the present invention.

Fig. 6 is a block diagram showing an encoding device in the fourth embodiment.

20 Fig. 7 is a diagram for explaining a zig-zag scanner 57 in Fig. 5.

Fig. 8 is a diagram for explaining a scan recovery unit 21 in Fig. 5.

25 Fig. 9 is a block diagram showing a configuration of a fifth embodiment of the present invention.

Fig. 10 is a circuit diagram of each of correlation detecting circuits 230, 232.

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1 Fig. 11 is a block diagram showing a
configuration of a sixth embodiment of the present
invention.

 Fig. 12 is a block diagram showing a
5 configuration of a seventh embodiment of the present
invention.

 Fig. 13 is a block diagram of a conventional
decoding device.

 Fig. 14 is a block diagram of a conventional
10 encoding device.

 Figs. 15A and 15B are diagrams for explaining
operation of Fig. 14.

 Fig. 16 is a block diagram showing a
configuration of an eighth embodiment of the present
15 invention.

 Fig. 17 is a block diagram of an encoding
device.

 Figs. 18A and 18B are diagrams for explaining
operation of Fig. 17.

20 Figs. 19, 20 and 21 are diagrams for explaining
operation of Fig. 17.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

(First Embodiment)

25 An image decoding device according to a first
embodiment of the present invention, described below,
is featured in comprising means for detecting and

1 correcting an error caused during transmission or in
reproduction from a recording medium, and means for
replacing decoded data in the relevant block by a
predetermined setting value based on error information
5 produced from the detecting and correcting means.

After detecting an error caused on a transmission path
and carrying out correction processing, if it is
found that the relevant block has a DC component
free from an error and an AC component still including
10 a correction impossible error, all the data in the
relevant block are replaced by a value of the DC
component based on such information, so that each
pixel value in the relevant block can be replaced by
a value close to a true value.

15 Fig. 1 illustrates a block diagram showing
a configuration of an image decoding device and a
corresponding image encoding device of this embodiment.

Denoted at reference numeral 401 is an
encoding device and 402 is a decoding device, both
20 the devices being connected to each other via a
transmission path 403. The transmission path 403
is in the form of a transmission medium for aboveground
electric-wave or light spaces, such as an optical
fiber, satellite or microwave guide, in the case of
25 instantaneous transmission, and in the form of a
storage medium including a tape-like medium such as a
digital VTR or DAT, a disk-like medium such as a

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1 floppy disk or optical disk, and a solid state medium
such as a semiconductor memory.

First, a video signal inputted from an image
reader comprising CCD sensors, TV camera, video
5 recorder, hostcomputer or the like is applied to an
input terminal 404 of the encoding device 401 and
divided in a block formation circuit 406 into blocks
each of which comprises a plurality of data, e.g.,
blocks each consisted of 8 x 8 pixels. The data thus
10 divided in units of block is transformed in an
orthogonal transform circuit 407 into frequency
components for each block through, for example, a
DCT (discrete cosine transform). The transformed
data is outputted as a low-frequency component and a
15 high-frequency component, for example, a DC (direct
current) component and an AC (alternating current)
component other than the former, in separate fashion.
These components are separately encoded by encoding
circuits 408, 409 for compressing the amount of
20 information. As examples of the encoding, the DC
component may be encoded by a PCM (pulse code
modulation) encoding method and the AC component may
be encoded by a run-length Huffman encoding method.
Respective encoded data outputted from the encoding
25 circuits 408, 409 are further encoded by ECC encoding
circuits 410, 411 to have error detecting and
correcting codes as a measure for coping with an

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1 error possibly caused during transmission, and then
synthesized by a synthesis circuit 412 together in a
time-serial manner. After that, the synthesized
data is added in a synch signal addition circuit 413
5 with a synch signal for each predetermined number of
blocks for the purpose of transmission or recording,
followed by delivery into the transmission path 403.

Meanwhile, as for the data transmitted and
received by the image decoding device 402, the
10 synch signal is detected by a synch signal detecting
circuit 101 and the following signal processing is
carried out on the basis of the detected synch signal.

The transmitted data is first separated by a
separation circuit 102 into encoded data corresponding
15 to the DC component and encoded data corresponding
to the AC component. At this time, the format of
the encoded data is selected such that the DC
components and the AC components are positively
separated from each other in one synch block, for
20 example, as shown in Fig. 2.

The respective separated data are then
inputted to ECC decoding circuits 103, 104 for
detection and correction of the error caused during
transmission. The ECC decoding circuits 103, 104
25 deliver the corrected data to decoding circuits 105,
106 and, simultaneously, deliver error information
to a DC replacement circuit 108 depending on the

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1 respective correction results.

 The respective encoded data corresponding to the DC component and the AC component after the correction processing are inputted to the decoding
5 circuits 105, 106 and then subjected to decoding processing for restoration into information of the DC component and the AC component. If any error still remains in the encoded data, the correct information cannot be of course restored.

10 In the case of using variable-length encoding, for example, as an encoding method for the AC component, it may happen that the decoded value of the AC component does not become a true value and, besides, even the number of data is not restored.

15 The respective decoded data outputted from the decoding circuits 105, 106 are transformed by an inverse orthogonal transform circuit 107 from values indicating the frequency components into data indicating a pixel value in the block. However, if
20 the error cannot be completely corrected by the ECC decoding circuits 103, 104 as mentioned before, the input value to the inverse orthogonal transform circuit 107 is not in itself correct information and thus an output value of the inverse orthogonal
25 transform circuit 107 will be data quite different from the correct pixel data.

 Therefore, when the error information produced

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1 from the ECC decoding circuit 103 indicates that no
error is present in the DC components for the relevant
block, and the error information produced from the
ECC decoding circuit 104 indicates that the
5 correction impossible error is present in the AC
components for the relevant block, a DC replacement
circuit 108 replaces all the pixel values in the
relevant block by the respective values given by the
DC components.

10 With the above replacing operation, even if
the correction impossible error still remains as
mentioned above, each pixel value in the block is
given by the value of the DC component which is
representative of an average value, meaning that the
15 data can be restored to a value, though not exactly
the same as the true value, relatively close to the
true value.

The respective data are rearranged by a time
base transform circuit 109 to line up on the same
20 time base as for the video signal inputted to the
encoding device, followed by delivery from an output
terminal 110. The output terminal 110 is connected
to a monitor, printer or the like for forming an image.

According to the image decoding device thus
25 arranged, even if the correction impossible error
occurs on the transmission path, a deterioration of
image quality is minimized.

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1 (Second Embodiment)

Fig. 3 shows a second embodiment of the present invention.

In the second embodiment of Fig. 3, the
5 function effected by the DC replacement circuit 108 in Fig. 1 is realized by a 0 replacement circuit 308. The other circuit blocks are the same as those in Fig. 1 and, therefore, are denoted at the same reference numerals.

10 When the respective error information outputted from the ECC decoding circuits 103, 104 indicate that no error is present in the DC components for the relevant block and the correction impossible error is present in the AC components for the relevant
15 block, as with the above first embodiment, the 0 replacement circuit 308 replaces all the values of the AC components. With that replacing operation, the respective data inputted to the inverse orthogonal transform circuit 107 have their AC components set
20 equal to 0. Consequently, the inverse orthogonal transform circuit 107 outputs the transformed data such that all the pixel values in the relevant block are given by the respective values of the DC component, with the result of the similar advantage to
25 the foregoing first embodiment.

(Third Embodiment)

Fig. 4 shows an example indicating the fact

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1 that the present invention is also applicable to a
different method of arranging the error detecting and
correcting codes.

In this embodiment, the ECC decoding circuit
5 104 in the decoding device of Fig. 1 and the ECC
encoding circuit 411 in the encoding device of Fig. 1
are located upstream of the separation circuit 102
and downstream of the synthesis circuit 412,
respectively, as an ECC decoding circuit 304 and an
10 ECC encoding circuit 311. The error detecting and
correcting codes are formed for the data resulted
from synthesizing the DC component and the AC
component.

In this case, the error information outputted
15 from the ECC decoding circuit 304 indicates that an
error is present in the transmitted data, and the
error information outputted from the ECC decoding
circuit 103 indicates that no error is present in the
DC components, this means that replacement of the AC
20 component by the DC component is effective. Thus,
the replacement can be performed by the same DC
replacement circuit 108 as that in Fig. 1.

According to the above first to third
embodiment of the present invention, as described
25 above, by using means for detecting and correcting
an error caused during transmission or in reproduction
from a recording medium, and means for replacing all

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1 the decoded data in the relevant block by respective
values given by DC components based on error informa-
tion produced from the detecting and correcting
means, or other means identical to the latter means,
5 it is possible to minimize a deterioration of image
quality even if a correction impossible error occurs,
and also realize an image decoding device which
requires the small amount of hardware to be added.

Especially, in the above embodiments, a
10 frequency transform coefficient due to the orthogonal
transform is encoded using the DC component and the
AC component in separate fashion. Therefore, when an
error in the AC component cannot be corrected, the
DC component can be used for error correction.

15 According to the above embodiment of the
present invention, deterioration of an image quality
of the image decoding device can be reduced.

(Fourth Embodiment)

An image processing apparatus according to a
20 fourth embodiment of the present invention, described
below, includes means for generating error detected
information when a predetermined dynamic range of
conversion coefficients is exceeded, and means for
correcting the data falsely decoded, thereby solving
25 the problem as set forth above.

Fig. 6 is a block diagram showing this
embodiment.

- 20 -

1 In Fig. 6, image data applied to an input
terminal 41 is delivered to a discrete cosine transform
(referred to as a DCT) unit 43 and subjected to a
two-dimensional DCT for each block of 8 x 8 pixels.
5 In this case, for example, it is supposed that a
transform coefficient of 12 bits is obtained for
image data of 8 bits.

 After performing the two-dimensional DCT, the
transform coefficient is linearly quantized by a
10 quantizer 45. The quantization step size is different
for each transform coefficient. The quantization
step sizes for the respective transform coefficients
are given as values resulted by multiplying quantiza-
tion coefficients generated from a quantization
15 matrix unit 49 and shown in Table 2 below, for example,
by 2^S . Here, S is called a scaling factor and out-
putted to not only a multiplier 47 but also a
multiplexer 61. The multiplier 47 multiplies an
output of the quantization matrix unit 49 by 2^S and
20 delivers the resulting coefficient to the quantizer
45. Thus, image quality and the number of data
generated are controlled depending on a value of S.
Specifically, with the scaling factor S increasing,
the amount of data is reduced but image quality
25 deteriorates. With the scaling factor S decreasing,
the amount of data is enlarged but image quality
ameliorates.

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Table 2

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10

16	11	10	16	24	40	51	61
12	12	14	19	26	58	60	55
14	13	16	24	40	57	69	56
14	17	22	29	51	87	80	62
18	22	37	56	68	109	103	77
24	35	55	64	81	104	113	92
49	64	78	87	103	121	120	101
72	92	95	98	112	100	103	99

As regards to a DC component of the orthogonal transform coefficient quantized by the quantizer 45, a one-dimensional forecaster 53 makes forecast and a resulting forecast error is Huffman-encoded by a Huffman encoder 55 and then outputted to the multiplexer 61. The Huffman encoder 55 divides outputs of the forecast errors into 16 groups as shown in Table 3 below, for example. The identification (ID) number SSSS of the group to which the forecast error belongs is first Huffman-encoded and then expressed by an equi-length code indicating any value in the relevant group. In the case of Table 3, the code length of the equi-length code is equal to the value of the group ID number SSSS.

Table 3

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Forecast Error of DC Transform after Quantiza- tion	Group ID Number SSSS
0	0
-1,1	1
-3,-2,2,3	2
-7 ~ -4,4 ~ 7	3
-15 ~ -8,8 ~ 15	4
-31 ~ -16,16 ~ 31	5
-65 ~ -32,32 ~ 65	6
-127 ~ -64,64 ~ 127	7
-255 ~ -128,128 ~ 255	8
-511 ~ -256,256 ~ 511	9
-1023 ~ -512,512 ~ 1023	10
-2047 ~ -1024,1024 ~ 2047	11
-4095 ~ -2048,2048 ~ 4095	12
-8191 ~ -4096,4096 ~ 8191	13
-16383 ~ -8192,8192 ~ 16383	14
-32767 ~ -16384,16384 ~ 32767	15

20

As for an AC component of the orthogonal transform coefficient except for the DC component, the output of the quantizer 45 is outputted to a zig-zag scanner 57. The zig-zag scanner 57 performs zig-zag scan from a low-frequency component to a high-frequency component as shown in Fig. 7. Thereafter, an output of the zig-zag scanner 57 is delivered to a Huffman encoder 59.

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1 The Huffman encoder 59 divides the transform
coefficients, which have the quantization results
other than 0 (hereinafter referred to as significant
coefficients), into 15 groups depending on their
5 values and sets the group ID number as SSSS, as shown
in Table 4 below. The number of the transform
coefficients, which are sandwiched between the
preceding and succeeding significant coefficients
and have the quantization results equal to 0 (herein-
10 after referred to as insignificant coefficients),
is set as a run length NNNN. Then, the group ID
number SSSS and the run length NNNN are combined
into a set, as shown in Table 5, followed by the
Huffman encoding. Subsequently, the ID number SSSS
15 is expressed by an equi-length code indicating any
value in the relevant group shown in Table 4.

20

25

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Table 4

	Quantization Output Level of AC Orthogonal Transform Coeff.	Group ID Number SSSS
	- 1,1	1
5	- 3, - 2,2,3	2
	- 7 ~ - 4,4 ~ 7	3
	- 15 ~ - 8,8 ~ 15	4
	- 31 ~ - 16,16 ~ 31	5
	- 65 ~ - 32,32 ~ 65	6
10	- 127 ~ - 64,64 ~ 127	7
	- 255 ~ - 128,128 ~ 255	8
	- 511 ~ - 256,256 ~ 511	9
	- 1023 ~ - 512,512 ~ 1023	10
	- 2047 ~ - 1024,1024 ~ 2047	11
15	- 4095 ~ - 2048,2048 ~ 4095	12
	- 8191 ~ - 4096,4096 ~ 8191	13
	- 16383 ~ - 8192,8192 ~ 16383	14
	- 32767 ~ - 16384,16384 ~ 32767	15

20

In the case of Table 4, the code length of the equi-length code is equal to the value of the group ID number SSSS. The case that the value of the run length NNNN exceeds 16 is dealt with by sending a code of R16 shown in Table 5 and repeatedly

25 subtracting 15 from the run length NNNN until the remainder becomes equal to or less than 15. When all the significant coefficients in the block are

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1 completely encoded, a code of EOB (End of Block)
in Table 5 is finally sent.

Table 5

5			Group ID Number SSSS						
			0	1	2		14	15	
10	Run Length NNNN	0	EOB	Huffman code for combination of NNNN and SSSS					
		1	no use						
		2							
		.							
		.							
.	14								
		15	R16						

The multiplexer 61 multiplexes the Huffman-
15 encoded data of the DC component and the Huffman-
encoded data of the AC component, followed by delivery
to an output terminal 63 after adding the scaling
factor S thereto.

Fig. 5 shows a block diagram a decoding device
20 in cooperation with the encoding device of Fig. 4.

The transmitted data is inputted to an XO
terminal 11 and delivered to a divider 13. The
divider 13 outputs the scaling factor S to a
multiplier 29, the DC component data to a Huffman
25 decoder 15, and the AC component data to a Huffman
decoder 19. The Huffman decoder 15 decodes a
series of Huffman codes to difference values and then

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1 outputs them to a difference decoder 17. The
difference decoder 17 restores each difference value
to the transform coefficient of the DC component and
then outputs it to a terminal a of a switch 23.

5 On the other hand, the Huffman-encoded data
of the AC component is restored by the Huffman decoder
19 to the transform coefficient of the AC component.
After that, the restored transform coefficient is
reverted by a scan recovery unit 21 from the zig-zag
10 scan series to a data series as shown in Fig. 8,
followed by delivery to a terminal b of the switch
23. Thus, both the transform coefficients of the
DC component and the AC component are multiplexed as
shown in Fig. 8 through the switch 23.

15 The multiplexer 29 multiplies the matrix
produced from a quantization matrix unit 27 by 2^{-S}
and outputs the resulting products to an inverse
quantizer 25. The transform coefficients of 8×8
are inversely quantized by the inverse quantizer 25
20 and outputted to an inverse discrete cosine transform
unit 31 for restoring to the image data of 8 bits.

While the transform coefficient inversely
quantized by the inverse quantizer 25 is outputted to
the inverse discrete cosine transform unit 31, it is
25 also outputted to a judgment unit 37. The image data
restored by the inverse discrete cosine transform unit
31 is outputted to not only a terminal a of a switch

1 39 but also a frame memory 35. The frame memory 35
delays the image data by a time period of one frame
and then outputs the delayed data to a terminal b
of the switch 39 for the purpose of using it as
5 correction data when an error is detected.

The judgment unit 37 compares the transform
coefficient with a predetermined dynamic range and
outputs the judgment result to the switch 39.

Assuming now that the dynamic range of
10 transform coefficients is 12-bit, for example, if the
transform coefficient exceeds 12 bits, this leads
to a judgment that an error has occurred in the
transmission path. When the result of the judgment
unit 37 judges the occurrence of an error, the
15 switch 39 is changed over for connection to the
terminal b so that the current image data is replaced
by the image data at the same location of preceding
one frame. When the judgment reveals the presence
of no error, the switch 39 is changed over for
20 connection to the terminal a. The image data whose
error has been corrected through the switch 39 is
delivered to an output terminal 33.

It is needless to say that although this
embodiment makes a correction using a group of pixels
25 of preceding one frame, the correction may performed
by using other group of surrounding pixels which has
high correlation. In this case, the frame memory 35

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1 for storing the image data of preceding one frame can
be dispensed with and, as a result, the circuit
configuration is simplified.

Further, although the above judgment has been
5 made by using the frequency component before transform
into the actual space, the image data after being
restored to the real space through the inverse DCT
may be instead used.

The above judgment is performed for each
10 pixel and, if an error is found in at least one
component in the block, the entire block is replaced
by the image data of the preceding frame. Alternative-
ly plural blocks or an entirety of one picture may
be replaced.

15 In addition, the orthogonal transform is not
limited to the DCT and may be any other suitable one
such as an Adamar transform.

In place of Huffman encoding, other multi-
value data encoding, arithmetic encoding or the like
20 may also be used.

With this embodiment thus arranged, since
there are provided error detecting means specific
to the decoding process and error correcting means,
image quality can be simply prevented from deteriorat-
25 ing when an error occurs.

As explained above, according to the fourth
embodiment of the present invention, it is possible to

1 prevent a deterioration of image quality otherwise
caused by the occurrence of an error, and reproduce
good image quality.

(Fifth Embodiment)

5 Fig. 9 illustrates a block diagram showing a
configuration of a fifth embodiment of the present
invention. Denoted at 210 is an input terminal for
an analog image signal, 212 is an A/D converter for
converting the analog image signal into a digital
10 image signal, 214 is an encoder for encoding the
digital image signal with high efficiency, and 216
is an ECC (error detecting and correcting code)
addition circuit for adding an ECC so as to detect
and correct a transmission error which may be caused
15 in a recording/reproducing system such as a magnetic
tape or optical disk, a communication/transmission
system such as an optical fiber or communication
satellite, etc. 218 is a transmission path which is
practically in the form of a recording/reproducing
20 system such as a magnetic tape or optical disk, or
a communication/transmission system such as an
optical fiber or communication satellite.

Denoted at 220 is an ECC decoding circuit
corresponding to the ECC addition circuit 216, and
25 222 is a decoder corresponding to the encoder 214.
The ECC decoding circuit 220 outputs the error
corrected data to the decoder 222 and outputs an

1 error correction impossible signal (flag) for the
data including an error which cannot be corrected.
The error correction impossible signal (flag) is
delayed through frame memories 233, 235 by a time
5 period of two frames and then supplied to a switch
control circuit 236 described later. 224, 226, 228
are frame memories serially interconnected and each
comprising an FIFO (first-in first-out) memory.
230 is a correlation detecting circuit for detecting
10 correlation between an output of the decoder 222
and an output of the frame memory 224, i.e., inter-
frame correlation, whereas 230 is a correlation
detecting circuit for detecting interframe correlation
between outputs of the frame memories 224 and 226.
15 234 is a switch for selecting any one of the outputs
of the frame memories 224, 226, 228. Depending on
the error correction impossible flag from the ECC
decoding circuit 220 and the detection results of
the correlation detecting circuits 230, 232, the switch
20 control circuit 236 changes over the switch 234.
238 is a D/A converter for converting the data
selected by the switch 234 into an analog signal,
and 240 is an output terminal for the reproduced
analog image signal.
25 Fig. 10 shows an exemplified circuit
configuration of each of the correlation detecting
circuit 230, 232. 242, 244 are input terminals for

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1 respective image data, and 246 is a subtracter for
calculating the difference between the two image data
applied from the input terminals 242, 244. 248 is
an adder and 250 is a D flip-flop for feeding an
5 output of the adder 248 back to the adder 248 while
delaying it by a time period of one sample. The
adder 248 and the D flip-flop 250 cooperate to
constitute an accumulator. An output of the adder
248 resulted from adding the current output of the
10 subtracter 246 and the preceding one-frame output
thereof is delivered from an output terminal 252.

Operation of this embodiment shown in Fig. 9
will now be described. The A/D converter 212 samples
the analog image signal, applied to the input terminal
15 210, at a predetermined sampling rate for converting
it into a digital signal of 8 bits or 16 bits. The
encoder 214 compresses the digital image signal
outputted from the A/D converter 212, namely, encodes
the digital image signal with high efficiency through
20 DPCM encoding or ADCT encoding. This embodiment is
not restricted by the type of high-efficient encoding
itself. The ECC addition circuit 216 adds the error
detecting and correcting code in accordance with a
predetermined method.

25 The output of the ECC addition circuit 216
is inputted to the ECC decoding circuit 220 via the
transmission path 218 in the form of a recording/

1 reproducing system or communication/transmission
system. During transmission through the transmission
path 218, there occurs a transmission error at certain
probability. The ECC decoding circuit 220 checks
5 the data inputted from the transmission path 218 for
detecting the presence or absence of an error, the
position of the error, and whether the error can be
corrected or not, followed by delivery to the decoder
222 after correcting the correction possible error.
10 When the correction impossible error is found, the
error correction impossible flag is outputted to the
switch control circuit 236.

The decoder 222 decodes (expands) the data
compressed by the encoder 214 and outputs the original
15 image data to both the frame memory 224 and the
correlation detecting circuit 230. Since the frame
memories 224, 226, 228 are operated in an FIFO manner and
cascaded to each other, the image data of successive
three frames are sequentially stored in the frame
20 memories 224, 226, 228. The correlation detecting
circuit 230 detects correlation between the current
frame (the output of the decoder 222) and the frame
preceding one (the output of the frame memory 224),
whereas the correlation detecting circuit 232 detects
25 correlation between the frame preceding one (the
output of the frame memory 224) and the frame preceding
twos (the output of the frame memory 226) with

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1 respect to the current frame (the output of the
decoder 222). The correlation detecting circuits 230,
232 each store one frame of differences between the
corresponding image signals of two frames inputted
5 thereto, and determines a degree of correlation
between the two frames.

 The switch 234 can select any one of the
outputs from the frame memories 224, 226, 228 and
normally selects the output of the frame memory 226.
10 The switch control circuit 236 can find the position
of the correction impossible error over the picture
based on the error correction impossible flag from
the ECC decoding circuit 220, and also find which
one of the preceding picture and the succeeding
15 picture has a higher degree of correlation with
respect to the output picture of the frame memory
226, based on the outputs from the correlation
detecting circuits 230, 232. Stated otherwise, in
response to the error correction impossible flag
20 from the ECC decoding circuit 220, the switch control
circuit 236 changes over the switch 234 to thereby
select the image data at the same position on the
picture which has a higher degree of correlation.

 The D/A converter 238 converts the image data
25 outputted from the switch 234 into an analog signal,
following which the reproduced analog image signal
is outputted from the output terminal 240.

1 (Sixth Embodiment)

Fig. 11 illustrates a block diagram showing
a configuration of a sixth embodiment of the present
invention. This embodiment adopts an ADCT method
5 as a high-efficient encoding method.

Denoted at 1110 is an input terminal for an
analog image signal, 1112 is an A/D converter, and
1114 is an encoder of ADCT type. The encoder 1114
separates the input data into a DC component and an
10 AC component through a DCT transform made for each DCT
block, e.g., 8 x 8 pixels, performs DPCM encoding on
the DC component between the current DCT block and
the preceding DCT block, and simultaneously performs
run-length processing and Huffman encoding on the AC
15 component. 1116 is an ECC (error detecting and
correcting code) addition circuit for adding an ECC to
the respective encoded outputs of the AC component
and the DC component from the ADCT encoder 1114.

1118 is a transmission path or system, 1120
20 is an ECC decoding circuit corresponding to the ECC
addition circuit 1116, and 1122 is an ADCT decoder
corresponding to the ADCT encoder 1114. 1124, 1126,
1128 are frame memories serially interconnected and
each comprising an FIFO (first-in first-out) memory.
25 1129, 1130 are frame memories of FIFO type for
delaying the DC component outputted from the ADCT
decoder 1122 by a time period of one frame, and are

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1 cascaded for detecting correlation. 1131 is a
correlation detecting circuit for detecting interframe
correlation between an output of the decoder 1122
and an output of a frame memory 1129, whereas 1132
5 is a correlation detecting circuit for detecting
interframe correlation between outputs of the frame
memories 1129 and 1130. 1134 is a switch for selecting
any one of the outputs of the frame memories 1124,
1126, 1128. Depending on the error correction
10 impossible flag from the ECC decoding circuit 1120
and the detection results of the correlation detecting
circuits 1131, 1132, a switch control circuit 1136
changes over the switch 1134. 1138 is a D/A converter
for converting the data selected by the switch 1134
15 into an analog signal, and 1140 is an output terminal
for the reproduced analog image signal.

Specific operation of this embodiment shown
in Fig. 11 will now be described. The A/D converter
1112 converts the analog image signal, applied to the
20 input terminal 1110, into a digital signal. The
ADCT encoder 1114 carries out a DCT transform on the
digital image signal outputted from the A/D converter
1112 for each DCT block such that the DC component is
subjected to DPCM encoding between the current DCT
25 block and the preceding DCT block, and the AC
component is subjected to run-length processing and
Huffman encoding. The ECC addition circuit 1116

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1 adds an ECC to the AC component output and the DC
component output from the ADCT encoder 1114.

The output of the ECC addition circuit 1116
is inputted to the ECC decoding circuit 1120 via
5 the transmission path 1118. The ECC decoding circuit
1120 checks the respective AC and DC component data
inputted from the transmission path 1118 for detecting
the presence or absence of an error, the position of
the error, and whether the error can be corrected or
10 not, followed by delivery to the ADCT decoder 1122
after correcting the correction possible error. When
the correction impossible error is found, an error
correction impossible flag is delayed through frame
memories 1133, 1135 by a time period of two frames
15 and then supplied to the switch control circuit 1136.

The ADCT decoder 1122 performs DPCM decoding
on the DC component and both Huffman decoding and
run-length decoding on the AC component, followed
by an inverse DCT transform for restoring to the
20 original image data. The image data restored by the
ADCT decoder 1122 is applied to the frame memory
1124, whereas the DC component before the inverse DCT
transform is applied to both the frame memory 1129
and the correlation detecting circuit 1131 for the
25 DC component. As with the frame memories 224, 226,
228 in Fig. 10, the frame memories 1124, 1126, 1128
respectively store the image data of successive

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1 three frames in a sequential manner. The frame
memories 1129, 1130 are also cascaded to store the
DC components of adjacent two frames on a frame-
by-frame basis. As for the DC component, the
5 correlation detecting circuit 1131 detects correlation
between the current frame (the output of the decoder
1122) and the frame preceding one (the output of the
frame memory 1129), whereas the correlation detecting
circuit 1132 detects correlation between the frame
10 preceding one (the output of the frame memory 1129)
and the frame preceding twos (the output of the frame
memory 1130) with respect to the current frame.
The correlation detecting circuits 1131, 1132 may
be the same circuit configuration as that shown in
15 Fig. 10, and each store one frame of differences in
the DC component between the corresponding image
signals of two frames inputted thereto. Thus, a
degree of correlation between the two frames can be
determined.

20 The switch 1134 can select any one of the
outputs from the frame memories 1124, 1126, 1128
and normally selects the output of the frame memory
1126. The switch control circuit 1136 controls the
switch 1134 in a like manner to the switch control
25 circuit 236 shown in Fig. 9. Specifically, for the
error correction impossible data, the switch control
circuit 1136 enables to select the image data at the

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1 same position on the picture which has a higher
degree of correlation. The D/A converter 1138 converts
the image data outputted from the switch 1134 into
an analog signal, following which the reproduced
5 analog image signal is outputted from the output
terminal 1140.

With this embodiment shown in Fig. 11, since
correlation is detected by using the DC component,
correlation detection can be performed more correctly
10 and, therefore, interpolation can be performed in a
more natural manner.

While the illustrated embodiment include the
correlation detecting circuits disposed on the
decoder side (or the reception side), those circuits
15 may be disposed on the encoder side (or the trans-
mission side) so as to transmit information of
interframe correlation frame by frame. This remarkably
cut down the equipment burden to be borne on the
reception side. Accordingly, this modification is
20 fit for such a transmission system that is directed
to a large number of receivers like TV broadcasting
and requires the small size and reduced cost of
receiver units.

According to the fifth and sixth embodiments,
25 as will be easily understood from the above descrip-
tion, since information of interframe correlation is
used to interpolate the error correction impossible

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1 data, it is possible to make the perforation in a
more natural manner and provide a reproduced image
(received image) with less unnaturalness.

(Seventh Embodiment)

5 Fig. 12 is a block diagram showing a seventh
embodiment of the present invention. Transmitted
data applied to an input terminal 631 is decoded by
a run-length decoder 633 to a DPCM code, and the 0 run-
length of the data is outputted from the run-length
10 decoder 633 to a counter 632. The counter 632
continues counting both the 0 run-length and the
number of DPCM codes until arrival of a reset synch
bit. In other words, the counter 632 counts the
predetermined number of pixels in a processing unit.
15 The number of pixels counted by the counter 632 is
outputted to a comparator 636. The comparator 632
compares the predetermined number of pixels set by
a processing unit setter 634 and the number of
pixels outputted from the counter 632, thereby
20 outputting an error flag of 1 bit to a switch 640.
Stated otherwise, if both the numbers of pixels are
not in match with each other, then a flat is set
based on judging the presence of an error.

Meanwhile, the DPCM code decoded by the run-
25 length decoder 633 is outputted to the DPCM decoder
635 and further decoded to image data. The image
data outputted from the DPCM decoder 635 is delivered

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1 to a delay unit 638. The delay unit 638 delays the
image data by a predetermined amount of delay caused
in the comparator 636, to thereby match the timing
between the error flag and the image data. The image
5 data outputted from the delay unit 638 is delivered
to a contact a of the switch 640 and, simultaneously,
to a one-line delay unit 639 so that the same image
data is delivered to a contact b of the switch 640
after being delayed by a time period of one line.
10 When the error flag outputted from the comparator
636 indicates that no error has occurred, the switch
640 is changed over for connection to the contact a.
When an error has occurred, the switch 640 is changed
over for connection to the contact b so that the
15 current image data is replaced by the image data of
preceding one line for correction. In either case,
the correct or corrected image data is delivered to
an output terminal 637.

It is needless to say that while the above
20 embodiment is explained as using the encoding method
in combination of DPCM encoding and run-length
encoding, this embodiment is applicable to all the
methods that use run-length encoding, such as one in
which run-length encoding is performed after orthogonal
25 transform encoding. Also, the principles of this
embodiment can be employed in any of the foregoing
embodiments as well.

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1 As described above, according to the seventh
embodiment of the present invention, it is possible
to prevent a deterioration of image quality otherwise
caused by the occurrence of an error, by providing
5 error detecting means specifically adapted for the
process of decoding run-length codes.

(Eighth Embodiment)

Fig. 17 is a block diagram showing an encoding
method which combines twos, i.e., the orthogonal
10 transform encoding method and the run-length encoding
method, with each other. Image data applied to an
input terminal 711 is divided into blocks by a block
formation unit 713 such that a raster series of Fig.
18A is turned into a plurality of blocks as shown in
15 Fig. 18B. In this case, each block comprises 8
pixels horizontal and 8 pixels vertical. The pixel
data in each block are transformed by a transform
decoder 715. The transform decoder 715 employs a
transform encoding method called a discrete cosine
20 transform (DCT) encoding.

Generally, as shown in Fig. 19, the
coefficients obtained through the DCT transform of
the image data exhibit low resolution in the oblique
direction and has the smaller magnitude at the
25 higher frequency component. Those coefficients
obtained through the DCT transform are quantized by
a quantizer 717. The quantized transform coefficients

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1 are scanned by a zig-zag scanner 717 in zig-zag
fashion as shown in Fig. 20 for the reason that the
probability of the occurrence of 0 is increased at
the higher frequency component. Such zig-zag scan
5 results in successive appearance of 0s. The zig-zag
scanned data is applied to a run-length encoder 721
to form a set of the number of 0s and the coefficients
other than 0. Upon the completion of processing of
one block, an EOB code is outputted. An entropy
10 encoder 723 assigns a short code to those codes
having high occurrence probability and a long code to
those codes having low occurrence probability,
followed by delivery to a transmission format unit 725.
The transmission format unit 725 delivers the data
15 from an output terminal 727 after adding a synch bit
for every several blocks as shown in Fig. 21.

Fig. 16 is a block diagram showing a configura-
tion of a decoding device in cooperation with the
encoding device of Fig. 17. The data transmitted
20 through a transmission path is applied to an input
terminal 731 and decoded by an entropy decoder 733
to a run-length code.

The run-length decoder 751 performs run-
length decoding and outputs the decoded data to an
25 inverse zig-zag scanner 737 and, simultaneously,
outputs the sum of the number of 0s in a run and the
number of 1s other than 0, i.e., the number of

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1 transform coefficients, to a counter 753. The
counter 753 counts the number of transform coef-
ficients for each predetermined period of time.
Assuming now that the predetermined period of time
5 is one block, a processing unit setter 755 sets 64
equal to the number of transform coefficients. A
comparator 757 compares a value inputted from the
processing unit setter 755 with a value inputted from
the counter 753. If both the values are in match
10 with each other, then it is judged that the data
has been transmitted without errors. If both the
values are not in match with each other, then it is
judged that an error has occurred. Either judgment
result is outputted to a delay unit 759. The delay
15 unit 759 delays the judgment result by the amount
to be paid off by proceeding through an inverse zig-
zag scanner 737, an inverse quantizer 739 and an
inverse transform encoder 741.

On the other hand, the inverse transform
20 encoder 741 outputs the inversely transformed pixel
data to one terminal a of a switch 763 and also to a
frame memory 761. The frame memory 761 the pixel data,
which are delayed by a time period of one frame
therethrough, to the other terminal b of the switch
25 763. Depending on the judgment result outputted
from the delay unit 759, the switch 763 selects the
terminal a for a predetermined period of time when

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1 no error is found, and the terminal b for a predeter-
mined period of time when an error is found. In
other words, upon the occurrence of an error, the
current image data is replaced by the image data of
5 preceding frame for correction.

A raster formation unit 743 converts the
block series back into the raster series, followed
by delivery to an output terminal 743.

As described above, according to the eighth
10 embodiment of the present invention, a deterioration
of image quality otherwise caused by the occurrence
of an error can be prevented with a simple hardware
construction, by providing error detecting means
specifically adapted for the process of run-length
15 decoding.

It should be understood that the error
correction in the foregoing embodiments may be
performed by using any of the image data of preceding
frame and the image data of preceding field.

20 Furthermore, the present invention is not
limited to the foregoing embodiments and can be
variously modified and applied within a scope defined
by the attached claims.

Additionally, any combinations of the foregoing
25 embodiments are covered by the principles of the
present invention.

CLAIMS:

1. An image processing apparatus comprising:
receiving means for receiving encoded image data which are encoded into orthogonal transform coefficients by using orthogonal transform in a predetermined block unit;
error detecting means for detecting a transmission error of the encoded image data;
replacing means for replacing only a part of the orthogonal transform coefficients of an error block including the error detected by said error detecting means with a predetermined orthogonal transform coefficient; and
decoding means for decoding the encoded image data output from said replacing means.
2. An apparatus according to claim 1, wherein said replacing means replaces the part of the orthogonal transform coefficient of the error block with a DC component of the error block.
3. An apparatus according to claim 1, wherein said replacing means replaces the part of the orthogonal transform coefficient of the error block with a zero data.
4. An apparatus according to claim 1, wherein the part of the orthogonal transform coefficient is an AC component of the error block.
5. An image processing apparatus according to claim 1, wherein the orthogonal transform is a discrete cosine transform.
6. An image processing apparatus according to claim 1, wherein the predetermined block is a pixel block of $N \times N$.

7. An image processing apparatus according to claim 1, wherein said error detecting means detects the transmission error based on an ECC.

8. An image processing apparatus comprising:
receiving means for receiving an encoded orthogonal transform coefficients which are encoded by using run-length encoding method in units of blocks;

decoding means for decoding the encoded orthogonal transform coefficients and for outputting a decoded orthogonal transform coefficient;

error detecting means for detecting a transmission error of the encoded orthogonal transform coefficients in the block based on the encoded orthogonal transform coefficients in the block; and

correcting means for correcting the transmission error of the encoded orthogonal transform coefficients.

9. An apparatus according to claim 8, wherein said error detecting means detects the transmission error depending on a dynamic range of an orthogonal transform coefficient in the block which is obtained by decoding the encoded orthogonal transform coefficient.

10. An apparatus according to claim 8, wherein said error detecting means includes counting means for counting the decoded orthogonal transform coefficient, said error detecting means detecting the transmission error according to a counted value of said counting means.

11. An apparatus according to claim 10, wherein said error detecting means detecting the transmission error of the block by comparing a predetermined value with the counted value of the orthogonal transform coefficient of the block.

12. An image processing apparatus according to claim 8, wherein the orthogonal transform is a discrete cosine transform.

13. An image processing apparatus comprising:
transforming means for generating orthogonal transform coefficients corresponding to an image data by performing an orthogonal transform on an input image data, the orthogonal transform coefficients including a DC component and an AC component;

adding means for adding data for detecting transmission error in the orthogonal transform coefficients to the orthogonal transform coefficients so that a decoder is able to detect a DC component transmission error and an AC component transmission error independently; and

encoding means for encoding the DC component and the AC component.

14. An apparatus according to claim 13, wherein said data for detecting transmission error is an ECC.

15. An apparatus according to claim 13, wherein said encoding means wherein said encoding means encodes the DC component by a DPCM method.

16. An apparatus according to claim 13, wherein said encoding means performs zig-zag scan of the AC component in a predetermined block and encodes the AC component by Huffman encoding.

17. An image processing apparatus according to claim 13, wherein the orthogonal transform is a discrete cosine transform.

18. An image processing apparatus according to claim 8,

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wherein said error detecting means detects the transmission error by counting the decoded orthogonal transform coefficient.

19. An image processing apparatus according to claim 13, wherein said adding data is an ECC.

20. An image processing apparatus according to claim 13, wherein said encoding means encodes the DC component by a DPCM (difference pulse code modulation) method.

21. An image processing apparatus according to claim 13, wherein said encoding means performs zig-zag scan of the AC component in a predetermined block and encodes the AC component by Huffman encoding.

22. An image processing method comprising:
a receiving step of receiving encoded image data which are encoded into orthogonal transform coefficients by using orthogonal transform in a predetermined block unit;
an error detecting step of detecting a transmission error of the encoded image data;
a replacing step of replacing only a part of the orthogonal transform coefficient of an error block including the error detected in said error detecting step with a predetermined orthogonal transform coefficient; and
a decoding step of decoding the encoded image data output in said replacing step.

23. An image processing method comprising:
a receiving step of receiving an encoded orthogonal transform coefficients which are encoded by using run-length encoding method in units of blocks;
a decoding step of decoding the encoded orthogonal transform coefficients and for outputting a decoded orthogonal transform coefficient;

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an error detecting step of detecting a transmission error of the encoded orthogonal transform coefficients in the block based on the encoded orthogonal transform coefficients in the block; and

a correcting step of correcting the transmission error of the encoded orthogonal transform coefficients.

24. An image processing method comprising:

a transforming step of generating orthogonal transform coefficients corresponding to an image data by performing an orthogonal transform on an input image data, the orthogonal transform coefficients including a DC component and an AC component;

an adding step of adding data for detecting transmission error in the orthogonal transform coefficients to the orthogonal transform coefficients so that a decoder is able to detect a DC component transmission error and an AC component transmission error independently; and

an encoding step of encoding the DC component and the AC component.