THIN INTEGRAL RESISTOR/CAPACITOR/INDUCTOR PACKAGE, METHOD OF MANUFACTURE

The present invention is directed to thin electronic circuitry which provides resistors, capacitors, interconnecting circuitry and optional inductors and to a method of manufacture of such structures.

Background of the Invention:

There is a continuing interest in printed circuitry miniaturization. In most printed circuit boards in use, circuitry traces are printed by conventional methods, particularly photoresist techniques. Accessory components such as capacitors and resistors are frequently provided as discrete components and soldered onto the printed circuitry, either manually or robotically. These components occupy "real estate" on the printed circuit board and may be difficult or expensive to apply to the board.

Accordingly, structures have been proposed in which components such as capacitors and/or resistors are provided along with circuitry traces by circuitization procedures. Examples of such structures are found in U.S. Patents Nos. 5,079,069, 5,155,655, 5,161,086, 5,261,153, 5,347,258, and 5,466,892, the teachings of each of which are incorporated herein by reference. Typically, a plurality of such structures are laminated together with dielectric material to form multi-layer printed circuit boards.

The present invention is directed to a method of forming a thin, circuitized laminate structure that provides capacitors, resistors, and conductive elements that include circuitry traces and optional inductors and to the thin circuitized laminate structure formed therefrom.

Summary of the Invention:

In accordance with the method of the invention, there is provided a first conductive metal foil to which is laminated an embeddable dielectric material layer and a second conductive metal foil which is coated on one side with a resistive material layer, the resistive material layer on the second foil having a thickness less than that of the embeddable dielectric

material layer on the first foil. The resistive material layer is circuitized to form discrete patches of resistive material. Then the two structures are laminated together with the resistive material layers being embedded into the embeddable dielectric material layer without the resistive material patches contacting the first foil. At this point, either the first or the second foil is circuitized, providing interconnecting circuitry traces and optional electrical components such as inductors. To support the structure, the circuitized foil is embedded in dielectric material such as glass-filled epoxy known as "prepreg", this material supporting the structure during subsequent processing. With the structure so supported, the other foil is then circuitized and this side too may be embedded in dielectric material. Several such structures may be laminated together to form a multi-layer printed circuit board, the several layers being electrically interconnected by via holes in conventional manner.

Brief Description of the Drawings:

Figure 1 illustrates a cross-sectional view of a first foil with a thin layer of embeddable dielectric material laminated thereto.

Figure 2 illustrates a cross-sectional view of a second foil with a thin layer of resistive material deposited thereon.

Figure 3 illustrates a cross-sectional view of the structure of Figure 2 in which the resistive material on the second foil has been circuitized to form discrete resistive patches.

Figure 4 illustrates a cross-sectional view of the structure of Figure 1 laminated to the structure of Figure 3 with the resistive material patches embedded into the embeddable dielectric material layer.

Figure 5 illustrates a cross-sectional view of the structure of Figure 4 in which the second foil layer has been circuitized.

Figure 6 illustrates a cross-sectional view of a structure in which the circuitized second foil layer has been embedded into a dielectric material and the first foil layer has subsequently been circuitized.

Detailed Description of Certain Preferred Embodiments:

Illustrated in Figure 1 is a structure 10 comprising a foil layer 11 to which is laminated a thin layer of dielectric material 12. Illustrated in Figure 2 is a structure 13 comprising a foil layer 14 on which a thin layer of resistive material is deposited. The foil layers 11,14 may be selected from a variety of metals and metal alloys, although copper foil is the most commonly used. Typically the foils 11, 14 are between about 3 and about 50 microns thick. The dielectric material layer 12 is between about 3 and about 50 microns thick. The resistive material layer 15 is between about 0.1 and about 0.5 microns thick, but in any case thinner, typically between about 2.9 and about 49.5 microns less thick than the dielectric material layer 12.

A currently preferred material used as the dielectric material layer 12 is on epoxy resin such as that sold under the trademark Dynavin.

As a first step, the resistive material layer 15 is circuitized so as to form discrete resistive layer patches 15a on the second foil 14 to form structure 13a of Figure 3. (For simplification of illustration, only one such resistive patch 15a is shown.) Circuitization of the resistive layer 15 is closely analogous to conventional circuitization of conductive to form printed circuitry traces. The resistive layer 15 is covered with a photoresist (described herein terms of a negative-acting photoresist); the photoresist is exposed through artwork to actinic radiation; unexposed portions of the photoresist are developed away, and exposed portions of the underlying resistive material layer 15 are etched away.

U.S. Patent Application No. 09/198,954, the teachings of which are incorporated herein by reference, teaches a preferred resistive material for forming layer 15. This patent application teaches that platinum containing relatively small amounts of a dielectric, such as silica, has substantial electrical resistivity, depending upon the amount of the dielectric, typically ranging from about 0.5 wt% to about 5.0 wt%. A thin layer of silica-doped platinum is conveniently deposited by combustion chemical vapor deposition (CCVD) a process described in U.S. Patent No. 5,652,021, the teachings of which are incorporated herein by

reference. CCVD-deposited Pt/SiO_2 has substantial porosity, making it possible to remove selected portions of a Pt/SiO_2 from copper foil in a process described in above referenced U.S. Patent Application No. 09/198,954 as ablative etching. The exposed portions of the Pt/SiO_2 layer are exposed to a copper etchant, such as ferric chloride. The etchant seeps through the Pt/SiO_2 layer, attacking the copper at the interface between the two layers. It is found that the Pt/SiO_2 layer ablates away when adhesion is lost before the underlying copper layer is significantly degraded. In this manner a Pt/SiO_2 layer on copper (or other foils) may be circuitized. As a refinement on this process, a very thin etchant-sensitive layer, e.g., nickel, (not shown) may be deposited either by CCVD or by electroplating on the copper foil before the Pt/SiO_2 layer is deposited. When an etchant seeps through the Pt/SiO_2 layer, it rapidly erodes the etchant-sensitive layer to facilitate the ablative etching process.

At this time, structure 10 having the dielectric material layer 12 on the first foil 11 is laminated to structure 13a by pressing the resistive material patches 15a side into the dielectric material 12, embedding the patches 15a into the dielectric material to form structure 16 of Figure 4. Because the dielectric material layer 12 is somewhat thicker than the resistive patches 15a, the patches 15a remain electrically isolated from the first foil 11 by a thinned portion of the dielectric material layer 12.

Next, the second foil layer 14 is circuitized by conventional photoresist circuitization techniques to form structure 19 having circuitry elements 20, 21 and 22 shown in Figure 5. (The process could be similarly practiced by first circuitizing the first foil layer 11 and later circuitizing the second foil layer 14.) Elements 20 represent conductive connecting traces at opposite ends of resistive patch 15a. A resistive electrical pathway is thereby formed between the connecting traces 20 through resistive patch 15a; 15a/20 as a unit thereby acting as a resistor. Element 21 represents one conductive plate of a capacitor, capacitance to be built up between element 21 and a similar plate to be later formed by circuitization of the first foil layer 11. Elements 22 represent printed electrical coils which serve as electrical inductors.

The thin dielectric material layer 12 has substantially no mechanical strength.

Accordingly, before structure 19 can be further processed, the circuitized side of structure 19 is embedded in a layer of laminate dielectric 26 which mechanically supports the structure as seen in Figure 6. Then the first foil layer is circuitized to form circuitry traces, capacitor plates 21 and inductor coils 22. This circuitized side is subsequently embedded in a further layer of laminate dielectric (not shown). A plurality of such structures may be laminated together to form a multi-layer printed circuit board in which via holes are formed and plated in conventional manner to form electrical connections between the multi-layers.

The invention will now be described in greater detail by way of specific examples.

Example 1

Formation of structure 10 as per Figure 1.

A 50 micron thick copper foil is laminated to a 50 micron sheet of Dynavin which acts as an embeddable dielectric material layer 12.

Example 2

Formation of structure 13 as per Figure 2

To a 50 micron thick copper foil there is deposited by electroplating a 3.5 micron layer of nickel. A 0-15 micron thick Pt/SiO_2 (97.5:2.5 by wt.) layer was deposited by CCVD under the following deposition conditions:

Solution Preparation	1.23 g. Pt(COD)*	
	250 ml. toluene	
	0.43 g TEOS** (1.5 wt% Si in toluene)	
	150 g propane	
Deposition conditions	Solution flow	3 ml/min
	Deposition time:	1 hour
	Deposition temp	500°C
	Variac	3.0 A
	Tip oxygen flow	2900 ml/min

*diphenyl-(1,5-cyclooctadiene) platinum II
**tetraethoxysilane

Example 3

Formation of the printed circuitry

The structure produce in Example 2 is covered on both sides with Laminar® 5000 photoresist. The Pt/SiO_2 side is exposed to patterned actinic radiation and the foil side fully exposed to actinic radiation. The structure is then developed in 2% sodium carbonate at 80°C to remove unexposed resist areas from the resistive material side. With exposed resist protecting the copper foil, the structure is exposed to a cupric chloride solution for a time sufficient for the solution to penetrate the Pt/SiO_2 and degrade the nickel layer sufficiently for the exposed portions of the Pt/SiO_2 to ablate away. Then the resist is stripped with NaOH solution. This etched structure is then laminated to the structure of Fig 1, embedding the remaining Pt/SiO_2 portions into the dielectric material.

Both foil layers are then coated with photoresist. The foil layer with the Pt/SiO_2 is exposed to patterned actinic radiation; the other foil layer fully exposed to protect the same during processing. The structure is developed in sodium carbonate as above, and the exposed portions of the one foil layer are etched with a ferric chloride solution to form circuitry traces, capacitor plates, resistor connections, and inductor coils. Then the resist is stripped from both sides of the structure.

The circuitized foil layer is embedded in laminate dielectric.

The other foil layer is then circuitized as before, forming circuitry traces, capacitor plates, and inductor coils.



What is Claimed is:

1. A method for forming electronic circuitry containing circuitry traces, integral resistors, and integral capacitors, the method comprising:

providing a first laminate structure comprising a first conductive metal foil and a layer of embeddable dielectric material laminated thereto,

providing a second laminate structure comprising a second conductive metal foil having a layer resistive material on one side thereof, said resistive material layer having a thickness less than that of said layer of embeddable dielectric material,

circuitizing said layer of resistive material to produce discrete resistive material patches on said second foil,

laminating said first and second structures so as to embed said resistive material patches in said layer of embeddable dielectric material,

circuitizing one or the other of said foils to form capacitor plates, circuitry traces, optionally inductor coils, and in case of the second foil resistor connections,

embedding the circuitized foil into laminate dielectric so as to support the structure for further processing, and

circuitizing the other of said foils to form capacitor plates, circuitry traces, optionally inductor coils, and in case of the second foil resistor connections.

2. The method of Claim 1 further embedding the other of said circuitized foils in laminate dielectric.

3. Laminating a plurality of the electronic circuitry produced by the method of Claim 1 together to form a multi-layer printed circuit board.

4. The method of Claim 1 wherein each of said foil layers is between about 3 and about 50 microns thick.

5. The method of Claim 1 wherein said resistive layer is between about 0.1 and about 0.5 microns thick; said embeddable material layer is between about 3 and about 50 microns thick, and said embeddable material layer is between about 2.9 and about 49.5 microns thicker

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than said electrically resistive material layer.

6. The method according to Claim 1 wherein said foils are copper.

7. The method according to Claim 1 wherein said embeddable dielectric material is epoxy.

8. The method according to Claim 1 wherein said resistive material layer is platinum doped with a dielectric material.

9. An embedded electrical circuitry structure comprising in order,

an embedding layer of epoxy layer,

a first circuitized layer of electrically conductive material,

a patterned layer of electrically resistive material having patches of resistive material in contact with said first circuitized conductive layer such that resistor electrical pathways are formed through said patches of said resistive material,

a dielectric material layer, said patches of resistive material embedding said patches of said resistive material, and,

a second circuitized layer of electrically conductive material, said dielectric material layer spacing said patches of resistive material from said second circuitized layer, capacitor electrical pathways being defined between said first and second circuitized layers through said dielectric material layer.

10. The structure according to Claim 9 wherein said second circuitized layer is embedded in an epoxy layer.

11. The structure according to Claim 9 wherein said dielectric material layer is an epoxy resin.

12. The structure according to Claim 9 wherein said resistive material layer is platinum doped with a dielectric material.

13. The structure of Claim 9 wherein each of said foil layers is between about 3 and about 50 microns thick.

14. The structure of Claim 9 wherein said resistive layer is between about 0.1 and about 0.5 microns thick; said embeddable material layer is between about 3 and about 50 microns thick, and said embeddable material layer is between about 2.9 and about 49.5 microns thicker