

**MEMORY DEVICE PERFORMING CACHE LATCH INITIALIZATION
OPERATION, MEMORY CONTROLLER FOR CONTROLLING THE SAME,
AND CACHE LATCH INITIALIZATION METHOD THEREOF**

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This patent application claims priority to Korean Patent Application No. 10-2024-0136083 filed on 7 October 2024, in the Korean Intellectual Property Office, the disclosures of which are incorporated by reference herein in its entirety.

TECHNICAL FIELD

[0002] The present disclosure relates to memory devices, a memory controller for the memory device, and a cache latch initialization method of a memory device.

BACKGROUND

[0003] Semiconductor memories may be classified as a volatile memory or a non-volatile memory, for example. Typically, the volatile memories (e.g., a dynamic random access memory (DRAM) or a static random access memory (SRAM)) may exhibit faster read and/or write speeds when compared to the non-volatile memory. However, data stored in the volatile memory may disappear when a power applied to the volatile memory is turned off. In contrast, the non-volatile memory may retain the data even when the power is turned off.

[0004] A representative example of the non-volatile memory may be a flash memory. The flash memory may store multi-bit data of two or more bits in one memory cell. The flash memory may have at least one erase state and a plurality of program (e.g., writing) states depending on threshold voltage distributions.

[0005] The flash memory may include a large number of cache latches in the page buffer

circuit. When the flash memory initializes a large number of cache latches simultaneously before a program operation, a large peak current may occur. In order to reduce the peak current, it must be divided into several units and initialized sequentially. This method requires a lot of initialization time. However, the time required for the flash memory to initialize cache latches is limited.

[0006] A conventional flash memory starts initializing cache latches when a command is input, and initializes cache latches for all planes without checking the addresses. Since cache latches are initialized for all planes, peak current and power noise may occur significantly. This problem may become more severe as the number of planes increases.

SUMMARY

[0007] In general, in some aspects, the present disclosure is directed toward a memory device that receives target plane information during a program operation and performs a cache latch initialization operation that reduces peak current by selectively initializing cache latches according to the target plane information.

[0008] According to some implementations, the present disclosure is directed to a memory device that comprises a memory cell array including first and second planes; a page buffer circuit including first cache latches for storing data to be stored in the first plane and second cache latches for storing data to be stored in the second plane; and input/output lines for receiving a command and addresses from a memory controller. Wherein the command includes target plane information for initializing the first cache latches and/or the second cache latches.

[0009] According to some implementations, the present disclosure is directed to a memory controller for controlling a memory device that comprises a memory cell array including first and second planes; a page buffer circuit including first cache latches for storing data to be

stored in the first plane and second cache latches for storing data to be stored in the second plane; and a cache latch control logic configured to provide a first cache latch initialization signal for initializing the first cache latches and a second cache latch initialization signal for initializing the second cache latches to the page buffer circuit, is configured to provide a command including target plane information to the memory device during a program operation. Wherein the first cache latches or the second cache latches are selectively initialized according to the target plane information.

[0010] According to some implementations, the present disclosure is directed to a cache latch initialization method of a memory device connected to a memory controller through input/output lines, the memory device comprises: a memory cell array including first to n-th planes; a page buffer circuit including first to n-th cache latches, first cache latches configured to store data to be stored in the first plane, and the n-th cache latches configured to store data to be stored in the n-th plane; a cache latch control logic configured to generate first to n-th cache latch initialization signals, the first cache latch initialization signal for initializing the first cache latches, the n-th cache latch initialization signal for initializing the n-th cache latches, and provide the first to n-th cache latch initialization signals to the page buffer circuit, comprises: receiving target plane information during a program operation; and providing the first cache latch initialization signal to the first cache latches or the n-th cache latch initialization signal to the n-th cache latches according to the target plane information.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] Example implementations will be more clearly understood from the following detailed description, taken in conjunction with the accompanying drawings.

[0012] FIG. 1 is a block diagram illustrating an example of a storage device according to some implementations.

[0013] FIG. 2 is a block diagram illustrating an example of the memory device illustrated in FIG. 1 according to some implementations.

[0014] FIG. 3 is a circuit diagram illustrating an example of a memory block BLK1 of the memory cell array illustrated in FIG. 2 according to some implementations.

[0015] FIG. 4 is a circuit diagram illustrating examples of cell strings selected by a first string selection line SSL1 from among the cell strings of the memory block BLK1 illustrated in FIG. 3 according to some implementations.

[0016] FIG. 5 is a diagram illustrating an example of threshold voltage distributions of memory cells illustrated in FIG. 4 according to some implementations.

[0017] FIG. 6 is a circuit diagram illustrating an example of the first page buffer PB1 shown in FIG. 4 according to some implementations.

[0018] FIG. 7 is a circuit diagram illustrating an example of the cache latch CL illustrated in FIG. 6 according to some implementations.

[0019] FIG. 8 is a block diagram illustrating an example of a cache latch initialization operation of a memory device according to some implementations.

[0020] FIG. 9 is a flowchart illustrating an example of the cache latch initialization operation of the memory device illustrated in FIG. 8 according to some implementations.

[0021] FIGS. 10, 11, 12, 13, 14 and 15 are timing diagrams illustrating an example of the cache latch initialization operation of the memory device illustrated in FIG. 9 according to some implementations.

[0022] FIGS. 16A, 16B, 16C and 16D are block diagrams illustrating examples of memory devices including various numbers of planes according to some implementations.

[0023] FIG. 17 is a diagram illustrating examples of peak currents generated during a program operation of the memory devices illustrated in FIGS. 16A, 16B, 16C and 16D according to some implementations.

[0024] FIGS. 18, 19, 20 and 21 are diagrams illustrating an example of the cache latch initialization operation of the memory device illustrated in FIG. 16C according to some implementations.

[0025] FIG. 22 is a diagram illustrating an example of a memory device having a multi-stack structure according to some implementations.

[0026] FIG. 23 is a block diagram illustrating an example in which a storage device is implemented with a solid state drive SSD according to some implementations.

DETAILED DESCRIPTION

[0027] Hereinafter, example implementations will be explained in detail with reference to the accompanying drawings.

[0028] FIG. 1 is a block diagram illustrating an example of a storage device according to some implementations. In FIG. 1, the storage device 1000 may be a flash storage device based on a flash memory. For example, the storage device 1000 may be implemented as a solid-state drive (SSD), a universal flash storage (UFS), a memory card, or the like.

[0029] In FIG. 1, the storage device 1000 may include a memory device 1100 and a memory controller 1200. The memory device 1100 may receive input/output signals IO from the memory controller 1200 through input/output lines, receive control signals CTRL through control lines, and receive external power supply PWR through power lines. The storage device 1000 may store data in the memory device 1100 under the control of the memory controller 1200.

[0030] The memory device 1100 may include a memory cell array 1110 and a peripheral circuit 1115. The memory cell array 1110 may have a vertical 3D structure. The memory cell array 1110 may include a plurality of planes. For example, the memory cell array 1110 may include first to fourth planes 1111 to 1114. Each plane may include a plurality of memory

cells. Single-bit data or multi-bit data may be stored in each memory cell.

[0031] In some implementations, the memory cell array 1110 may be located (e.g., disposed) next to or above the peripheral circuit 1115 in terms of the design layout structure. A structure in which the memory cell array 1110 is positioned over the peripheral circuit 1115 may be referred to as a cell on peripheral (COP) structure.

[0032] In some implementations, the memory cell array 1110 may be manufactured as a chip separate from the peripheral circuit 1115. An upper chip including the memory cell array 1110 and a lower chip including the peripheral circuit 1115 may be connected to each other by a bonding method. Such a structure may be referred to as a chip-to-chip (C2C) structure.

[0033] The peripheral circuit 1115 may include analog circuits and/or digital circuits required to store data in the memory cell array 1110 or read data stored in the memory cell array 1110. The peripheral circuit 1115 may receive the external power PWR through power lines and generate internal powers of various levels.

[0034] The peripheral circuit 1115 may receive commands, addresses, and/or data from the memory controller 1200 through input/output lines. The peripheral circuit 1115 may store data in the memory cell array 1110 according to the control signals CTRL. Additionally, the peripheral circuit 1115 may read data stored in the memory cell array 1110 and provide the read data to the memory controller 1200.

[0035] The peripheral circuit 1115 may include a large number of cache latches therein. When the memory device 1100 initializes a large number of cache latches simultaneously, a large peak current may occur. In order to reduce the peak current, it is necessary to divide into several units and sequentially initialize them. A large initialization time may be required to perform this. However, the time from command input to data loading is fixed.

[0036] The peripheral circuit 1115 may include a cache latch control logic 2000. The cache latch control logic 2000 may perform a cache latch initialization operation during a program

operation. The cache latch control logic 2000 may receive target plane information during a program operation and selectively initialize only the cache latches of target planes according to the target plane information, thereby reducing the peak current.

[0037] FIG. 2 is a block diagram illustrating an example of the memory device illustrated in FIG. 1 according to some implementations. In FIG. 2, the memory device 1100 may include the memory cell array 1110 and the peripheral circuit 1115 (see FIG. 1). The peripheral circuit 1115 may include an address decoder 1120, a page buffer circuit 1130, a data input/output circuit 1140, a word line voltage generator 1150, and a control logic 1160.

[0038] The memory cell array 1110 may include a plurality of planes. For example, the memory cell array 1110 may include first to fourth planes 1111 to 1114. The first plane 1111 may include a plurality of memory blocks BLK1 to BLKn. Each memory block may include a plurality of pages. Each page may include a plurality of memory cells. Each memory cell may store multi-bit data (e.g., two or more bits). Each memory block may correspond to an erase unit, and each page may correspond to a read unit and/or a write unit.

[0039] The memory cell array 1110 may be formed in a direction perpendicular to a substrate. A gate electrode layer and an insulation layer may be alternately deposited on the substrate. Each memory block (e.g., BLK1) may be connected to one or more string selection lines SSL, a plurality of word lines WL1 to WLm, and one or more ground selection lines GSL. WLk is a selected word line sWL and the remaining word lines (WL1 to WLk-1, WLk+1 to WLm) are unselected word lines uWL.

[0040] The address decoder 1120 may be connected to the memory cell array 1110 through selection lines SSL and GSL and word lines WL1 to WLm. The address decoder 1120 may select a word line during a program or read operation. The address decoder 1120 may receive the word line voltage VWL from the word line voltage generator 1150 and provide a program voltage or read voltage to the selected word line.

[0041] The page buffer circuit 1130 may be connected to the memory cell array 1110 via bit lines BL. The page buffer circuit 1130 may include first to fourth page buffer circuits 1131 to 1134. The first page buffer circuit (PGBUF1, 1131) may be connected to the first plane 1111 via bit lines BL. Similarly, the fourth page buffer circuit (PGBUF4, 1134) may be connected to the fourth plane 1114 via bit lines BL.

[0042] The page buffer circuit 1130 may temporarily store data to be stored in the memory cell array 1110 or data read from the memory cell array 1110. The page buffer circuit 1130 may include page buffers connected to respective bit lines. Each page buffer may include a plurality of latches to store or read multi-bit data.

[0043] The input/output circuit 1140 may be internally connected to the page buffer circuit 1130 through data lines and externally connected to the memory controller 1200 (refer to FIG. 1) through the input/output lines IO1 to IO_n. The input/output circuit 1140 may receive program data from the memory controller 1200 during a program operation. Also, the input/output circuit 1140 may provide data read from the memory cell array 1110 to the memory controller 1200 during a read operation.

[0044] The word line voltage generator 1150 may receive internal power from the control logic 1160 and generate a word line voltage VWL required to read or write data. The word line voltage VWL may be provided to a selected word line sWL or unselected word lines uWL through the address decoder 1120.

[0045] The word line voltage generator 1150 may include a program voltage generator 1151 and a pass voltage generator 1152. The program voltage generator 1151 may generate a program voltage V_{pgm} provided to the selected word line sWL during a program operation. The pass voltage generator 1152 may generate a pass voltage V_{pass} provided to the selected word line sWL and the unselected word lines uWL.

[0046] The word line voltage generator 1150 may include a read voltage generator 1153 and

a read pass voltage generator 1154. The read voltage generator 1153 may generate a select read voltage V_{rd} provided to the select word line sWL during a read operation. The read pass voltage generator 1154 may generate a read pass voltage V_{rdps} provided to unselected word lines uWL . The read pass voltage V_{rdps} may be a voltage sufficient to turn on memory cells connected to the unselected word lines uWL during a read operation.

[0047] The control logic 1160 may control operations, such as read, write, and erase, of the memory device 1100 using commands CMD , addresses $ADDR$, and control signals $CTRL$ provided from the memory controller 1200. The addresses $ADDR$ may include a block selection address for selecting one memory block, a row address for selecting one page, and a column address for selecting one memory cell.

[0048] The memory device 1100 may include a large number of cache latches. For example, each plane may include 16KB of cache latches. That is, the number of first cache latches $CL1$ of the first page buffer ($PGBUF1$, 1131) may be 16KB. The number of second to fourth cache latches $CL2$ to $CL4$ may each be 16 KB. When the memory device 1100 initializes a large number of cache latches simultaneously, a large peak current may occur. In order to reduce the peak current, it is necessary to divide into several units and sequentially initialize them. A large initialization time may be required to perform this.

[0049] However, the time from command input to data loading is limited. The time required for the memory device 1100 to perform a cache latch initialization operation is limited. The memory device 1100 receives a command, addresses, and data. If the memory device 1100 attempts to initialize the cache latches before receiving an address and loading data, the initialization operation may not be completed within the limited time.

[0050] Accordingly, cache latches begin to be initialized immediately when a command is input. The memory device initializes the cache latches of all planes without checking the addresses. Because the cache latches of all planes are initialized, peak current and power noise

may be large, and may become more severe as the number of planes increases.

[0051] The memory device 1100 may include cache latch control logic 2000. The cache latch control logic 2000 may reduce peak current by receiving target plane information during program operation and selectively initializing only the cache latches of the target planes according to the target plane information.

[0052] FIG. 3 is a circuit diagram illustrating an example of a memory block BLK1 of the memory cell array illustrated in FIG. 2 according to some implementations. In FIG. 3, in the memory block BLK1, a plurality of cell strings STR11 to STR8z may be formed between the bit lines BL1 to BLz and a common source line CSL. Each cell string includes a string selection transistor SST, a plurality of memory cells MC1 to MCm, and a ground selection transistor GST.

[0053] The string selection transistors SST may be connected with string selection lines SSL1 to SSL8. The ground selection transistors GST may be connected with ground selection lines GSL1 to GSL8. The string selection transistors SST may be connected with the bit lines BL1 to BLz, and the ground selection transistors GST may be connected with the common source line CSL.

[0054] The first to m-th word lines WL1 to WLm may be connected with the plurality of memory cells MC1 to MCm in a row direction. The first to z-th bit lines BL1 to BLz may be connected with the plurality of memory cells MC1 to MCm in a column direction. First to z-th page buffers PB1 to PBz may be connected with the first to z-th bit lines BL1 to BLz.

[0055] The first word line WL1 may be placed above the first to eighth ground selection lines GSL1 to GSL8. The first memory cells MC1 that are placed at the same height from the substrate may be connected with the first word line WL1. The m-th word line WLm may be located below the first to eighth string selection lines SSL1 to SSL8. The m-th memory cells MCm located at the same height from the substrate may be connected to the m-th word line

WL_m. In a similar manner, the second to (m-1)-th memory cells MC₂ to MC_{m-1} that are placed at the same heights from the substrate may be respectively connected with the second to (m-1)-th word lines WL₂ to WL_{m-1}, respectively.

[0056] FIG. 4 is a circuit diagram illustrating examples of cell strings selected by the first string selection line SSL₁ from among the cell strings of the memory block BLK₁ illustrated in FIG. 3 according to some implementations. In FIG. 4, the 11th to 1z-th cell strings STR₁₁ to STR_{1z} may be selected by the first string selection line SSL₁. The eleventh to 1z-th cell strings STR₁₁ to STR_{1z} may be connected to the first to z-th bit lines BL₁ to BL_z, respectively. The first to z-th page buffers PB₁ to PB_z may be connected to the first to z-th bit lines BL₁ to BL_z, respectively.

[0057] The eleventh cell string STR₁₁ may be connected to the first bit line BL₁ and the common source line CSL. The eleventh cell string STR₁₁ may include string selection transistors SST selected by the first string selection line SSL₁, first to m-th memory cells MC₁ to MC_m connected to the first to m-th word lines WL₁ to WL_m, and ground selection transistors GST selected by the first ground selection line GSL₁. The twelfth cell string STR₁₂ may be connected to the second bit line BL₂ and the common source line CSL. The 1z cell string STR_{1z} may be connected to the z-th bit line BL_z and the common source line CSL.

[0058] The first word line WL₁ and the m-th word line WL_m may be edge word lines (edge WL). The second word line WL₂ and the (m-1)-th word line WL_{m-1} may be edge adjacent word lines. The k-th word line WL_k may be a selected word line sWL. The (k-1)-th word line WL_{k-1} and the (k+1)-th word line WL_{k+1} may be adjacent word lines adjacent to the selected word line. If the k-th word line WL_k is the selected word line sWL, the remaining word lines WL₁ to WL_{k-1} and WL_{k+1} to WL_m may be unselected word lines uWL.

[0059] The first memory cells MC₁ and the m-th memory cells MC_m may be edge memory

cells. The second memory cells MC2 and the $(m-1)$ -th memory cells MC $m-1$ may be edge adjacent memory cells. The k -th memory cells MC k may be selected memory cells sMC. The $(k-1)$ -th memory cells MC $k-1$ and the $(k+1)$ -th memory cells MC $k+1$ may be memory cells adjacent to the selected memory cells (adjacent MC). If the k -th memory cells MC k are selected memory cells sMC, the remaining memory cells MC1 to MC $k-1$ and MC $k+1$ to MC m may be unselected memory cells uMC.

[0060] A set of memory cells selected by one string selection line and connected to one word line may be one page. For example, memory cells selected by the first string selection line SSL1 and connected to the k -th word line WL k may be one page. For example, eight pages may be configured on the k -th word line WL k . Among the eight pages, a page connected to the first string selection line SSL1 is a selected page, and pages connected to the second to eighth string selection lines SSL2 to SSL8 are unselected pages.

[0061] The first word line WL1 is a first edge word line (Edge1 WL), and the second word line WL2 is a first edge adjacent word line (Edge1 adjacent WL). The m -th word line WL m is the second edge word line (Edge2 WL), and the $(m-1)$ -th word line WL $m-1$ is the second edge adjacent word line (Edge2 adjacent WL). And word lines between the first and second edge adjacent word lines are middle word lines. For example, the k -th word line WL k ($k = 3$ to $m-2$) between the second word line WL2 and the $(m-1)$ -th word line WL $m-1$ is a middle word line.

[0062] In the read operation, if the second word line WL2 is the selected word line sWL, the remaining word lines may be unselected word lines uWL. The second word line WL2 may be a first edge adjacent word line (Edge1 adjacent WL). The second memory cells MC2 may be selected memory cells sMC. The remaining memory cells may be unselected memory cells uMC.

[0063] If the $(m-1)$ -th word line WL $m-1$ is the selected word line sWL, the remaining word

lines may be unselected word lines uWL. The $(m-1)$ -th word line WL_{m-1} may be a second edge adjacent word line. The $(m-1)$ -th memory cells MC_{m-1} may be selected memory cells sMC. The remaining memory cells may be unselected memory cells uMC.

[0064] FIG. 5 is a diagram illustrating an example of threshold voltage distributions of memory cells illustrated in FIG. 4 according to some implementations. An abscissa denotes a threshold voltage V_{th} of a memory cell, and an ordinate denotes the number of memory cells. 3-bit data may be stored in one memory cell. A 3-bit memory cell may have one of eight states (E0, P1 to P7) according to the threshold voltage distribution. E0 represents an erase state, and P1 to P7 represent program states.

[0065] During a read operation, the selection read voltages V_{rd1} to V_{rd7} may be provided to the selected word line sWL, and the pass voltage V_{ps} and/or the read pass voltage V_{rdps} may be provided to the unselected word lines uWL. The pass voltage V_{ps} and/or the read pass voltage V_{rdps} may be a voltage sufficient to turn on the memory cells. For example, the pass voltage V_{ps} may be provided to the adjacent word lines $WL_{k\pm 1}$, and the read pass voltage V_{rdps} may be provided to the unselected word lines other than the adjacent word lines.

[0066] The first selection read voltage V_{rd1} may be a voltage level between the erase state E0 and the first program state P1. The second selection read voltage V_{rd2} may be a voltage level between the first and second program states P1 and P2. In this way, the seventh selection read voltage V_{rd7} may be a voltage level between the sixth and seventh program states P6 and P7.

[0067] When the first selection read voltage V_{rd1} is applied, the memory cell in the erase state E0 may be an on cell and the memory cell in the first to seventh program states P1 to P7 may be an off cell. When the second selection read voltage V_{rd2} is applied, the memory cell in the erase state E0 and the first program state P1 may be an on cell, and the memory cell in the second to seventh program states P2 to P7 may be an off cell. In this way, when the seventh

selection read voltage Vrd7 is applied, the memory cell in the erase state E0 and the first to sixth program states P1 to P6 may be an on cell and the memory cell in the seventh program state P7 may be an off cell.

[0068] During a read operation, the k-th word line WLk may be selected. A power supply voltage may be applied to the string selection line SSL1 and the ground selection line GSL1, and the string select transistor SST and the ground select transistor GST may be turned on. Also, the selection read voltage Vrd may be provided to the selected word line sWL, and the read pass voltage Vrdps and/or the pass voltage Vps may be provided to the unselected word lines uWL.

[0069] FIG. 6 is a circuit diagram illustrating an example of first page buffer PB1 shown in FIG. 4 according to some implementations. In FIG. 6, the first page buffer PB1 may be connected to the first bit line BL1. A cell string STR11 may be connected to the first bit line BL1.

[0070] The cell string STR11 may include a string select transistor SST, a plurality of memory cells MC1 to MCm, and a ground select transistor GST. The cell string STR11 may be connected between the first bit line BL1 and the common source line CSL. The cell string STR11 may include a string selection transistor SST selected by a string selection line SSL, first to m-th memory cells MC1 to MCm connected to the first to m-th word lines WL1 to WLM, and a ground selection transistor GST selected by the ground selection line GSL. The k-th memory cell MCK may be a selected memory cell, and the k-th word line WLk may be a selected word line.

[0071] The first page buffer PB1 may be connected to the cell string STR11 through the first bit line BL1. A first NMOS transistor NM1 may be included between the first bit line BL1 and the first node N1. The first NMOS transistor NM1 may be a bit line select transistor driven by the bit line select signal BLSLT. The bit line select transistor may be implemented

as a high voltage transistor. The bit line select transistor may be disposed in the high voltage region.

[0072] A second NMOS transistor NM2 may be included between the first node N1 and the second node N2. The second NMOS transistor NM2 may be a bit line shut-off transistor driven by the bit line shut-off signal BLSHF.

[0073] A third NMOS transistor NM3 may be included between the SO node and the SOC node. The third NMOS transistor NM3 may be a sensing node pass transistor driven by the SOPASS signal. The SO node may have a Cso capacitance. A cache latch CL may be connected to the SOC node. The cache latch CL may be used to temporarily store data provided from the memory controller 1200.

[0074] A fourth NMOS transistor NM4 may be included between the second node N2 and the SO node. The fourth NMOS transistor NM4 may be a bit line connection transistor driven by the bit line connection control signal CLBLK.

[0075] A first PMOS transistor PM1 may be included between the SO node and the power terminal. The first PMOS transistor PM1 may be a precharge load transistor driven by the load signal LOAD. A pre-charge circuit 1137 may be included between the SO node and the second node N2. The precharge circuit 1137 may include a precharge transistor and a discharge transistor driven by the Lat_nS node.

[0076] A sensing latch SL, a force latch FL, a most significant bit latch ML, and a least significant bit latch LL may be connected to the SO node. The sensing latch SL may store data stored in the selected memory cell sMC or a sensing result of the threshold voltage of the selected memory cell sMC during a read or program verify operation. Also, the sensing latch SL may be used to apply a program bit line voltage or a program inhibit voltage to the first bit line BL1 during a program operation.

[0077] The force latch FL may be used to improve threshold voltage distribution during a

program operation. The most significant bit latch ML and the least significant bit latch LL may be utilized to store data input from the outside during a program operation.

[0078] The sensing latch SL may include an S latch LATs connected between the Lat_S node and the Lat_nS node. The S latch LATs may include first and second inverters IV1 and IV2. The Lat_nS node may be connected to an input terminal of the first inverter IV1 and an output terminal of the second inverter IV2. The Lat_S node may be connected to an output terminal of the first inverter IV1 and an input terminal of the second inverter IV2.

[0079] An NMa NMOS transistor may be included between the Lat_S node and a fifth node N5. The NMa NMOS transistor may be used to reset the Lat_S node in response to the RST_S signal. When the Lat_S node is reset, the Lat_S node may be a ground level and may store data 0.

[0080] An NMb NMOS transistor may be included between the Lat_nS node and the fifth node N5. The NMb NMOS transistor may be used to set the Lat_S node in response to the SET_S signal. When the Lat_S node is set, the Lat_S node may be a power supply voltage level and may store data 1.

[0081] An NMc NMOS transistor may be included between the fifth node N5 and the ground terminal. The NMc NMOS transistor may adjust the voltage level of the fifth node N5 in response to the RFSH signal. The NMd NMOS transistor may be included between the fifth node N5 and the ground terminal. The NMd NMOS transistor may adjust the voltage level of the fifth node N5 in response to the voltage level of the SO node. The bit line control signals (e.g., BLSLT, BLSHF, etc.) may be provided from the control logic 1160.

[0082] FIG. 7 is a circuit diagram illustrating an example of the cache latch CL illustrated in FIG. 6 according to some implementations. In FIG. 7, the cache latch CL may include a C latch LATc connected between the Lat_C node and the Lat_nC node.

[0083] The C latch LATc may include third and fourth inverters IV3 and IV4. The input

terminal of the third inverter IV3 and the output terminal of the fourth inverter IV4 may be connected to the Lat_nC node. The output terminal of the third inverter IV3 and the input terminal of the fourth inverter IV4 may be connected to the Lat_C node.

[0084] An NM_e NMOS transistor may be connected between the Lat_nC node and the SOC node. The NM_e NMOS transistor may be a cache latch monitoring transistor driven by the MON_C signal.

[0085] An NM_f NMOS transistor may be connected between the Lat_C node and the sixth node N6. The NM_f NMOS transistor may be used to reset the Lat_C node in response to the nDI signal. When the Lat_C node is reset, the Lat_C node may be ground level and may store data 0.

[0086] An NM_g NMOS transistor may be connected between the Lat_nC node and the sixth node N6. The NM_g NMOS transistor may be used to set the Lat_C node in response to the DI signal. When the Lat_C node is set, the Lat_C node may be the power voltage level and may store data 1.

[0087] An NM_h NMOS transistor may be connected between the sixth node N6 and the seventh node N7. The NM_h NMOS transistor may be used to dump data stored in the C latch LAT_c to the force latch FL, the most significant bit latch ML, or the least significant bit latch LL in response to the Dump_C signal.

[0088] An NM_i NMOS transistor may be connected between the sixth node N6 and the ground terminal. The NM_i NMOS transistor may adjust the voltage level of the sixth node N6 in response to the DIO_W signal. The NM_j NMOS transistor may be connected between the seventh node N7 and the ground terminal. The NM_j NMOS transistor may control the voltage level of the seventh node N7 according to the voltage level of the SOC node.

[0089] An NM_k NMOS transistor may be connected between the eighth node N8 and the ground terminal. The NM_k NMOS transistor may be turned on or off according to the voltage

level of the Lat_C node. When the Lat_C node is reset, a current path may be blocked between the eighth node N8 and the ground terminal. When the Lat_C node is set, a current path may be formed between the eighth node N8 and the ground terminal.

[0090] The NMo NMOS transistor may be connected between the eighth node N8 and the ninth node N9. The NMo NMOS transistor may perform a data input/output operation during a read operation in response to a DIO_R signal. The ninth node N9 may receive an RDI signal. The control signals (e.g., DI, nDI, Dump_C, etc.) of the cache latch CL may be provided from the control logic 1160.

[0091] FIG. 8 is a block diagram illustrating an example of a cache latch initialization operation of a memory device according to some implementations. In FIG. 8, the memory device 1100 may include a memory cell array 1110, a page buffer circuit 1130, and a cache latch control logic 2000.

[0092] The memory cell array 1110 may include first to fourth planes 1111 to 1114. The page buffer circuit 1130 may include first to fourth page buffer circuits 1131 to 1134.

[0093] The first page buffer circuit (PGBUF1, 1131) may include first cache latches CL1, the second page buffer circuit (PGBUF2, 1132) may include second cache latches CL2, the third page buffer circuit (PGBUF3, 1133) may include third cache latches CL3, and the fourth page buffer circuit (PGBUF4, 1134) may include fourth cache latches CL4.

[0094] The cache latch control logic 2000 may include first to fourth page buffer drivers PBD1 to PBD4. The cache latch control logic 2000 may receive a command including target plane information and generate first to fourth cache latch initialization signals DI1 to DI4.

[0095] The first page buffer driver PBD1 may generate a first cache latch initialization signal DI1 and provide it to the first page buffer circuit (PGBUF1, 1131). The first page buffer circuit (PGBUF1, 1131) may receive the first cache latch initialization signal DI1 to initialize the first cache latches CL1. The first cache latch initialization signal DI1 may be a signal for

resetting the Lat_nC node described in FIG. 7.

[0096] The second page buffer driver PBD2 may generate a second cache latch initialization signal DI2 and provide it to the second page buffer circuit (PGBUF2, 1132). The second page buffer circuit (PGBUF2, 1132) may receive the second cache latch initialization signal DI2 to initialize the second cache latches CL2.

[0097] The third and fourth page buffer drivers PBD3 and PBD4 may generate third and fourth cache latch initialization signals DI3 and DI4, respectively, and provide them to the third and fourth page buffer circuits 1133 and 1134, respectively. The third and fourth page buffer circuits 1133 and 1134 may receive third and fourth cache latch initialization signals DI3 and DI4, respectively, and initialize the third and fourth cache latches CL3 and CL4, respectively.

[0098] The cache latch control logic 2000 may receive a command including target plane information from the memory controller 1200 and selectively initialize the first to fourth cache latches CL1 to CL4. For example, if the command includes first plane information, the cache latch control logic 2000 may provide a first cache latch initialization signal DI1 to the first cache latches CL1 through the first page buffer driver PBD1.

[0099] If the command includes second plane information, the cache latch control logic 2000 may initialize the second cache latches CL2. If the command includes third plane information, the cache latch control logic 2000 may initialize the third cache latches CL3. If the command includes fourth plane information, the cache latch control logic 2000 may initialize the fourth cache latches CL4.

[0100] The command may include one or more plane information. For example, the command may include first and second plane information. When the command includes first and second plane information, the cache latch control logic 2000 may activate the first and second page buffer drivers PBD1 and PBD2 and initialize the first and second cache latches

CL1 and CL2.

[0101] FIG. 9 is a flowchart illustrating an example of the cache latch initialization operation of the memory device illustrated in FIG. 8 according to some implementations. The cache latch initialization operation of the memory device 1100 may include a command input operation, a column address and row address input operation, an operation of initializing cache latches of target planes, and a data loading operation.

[0102] The data loading operation may be an operation of loading data into cache latches of the page buffer circuit 1130. Before performing the data loading operation, the memory device 1100 may receive a command including target plane information and selectively initialize cache latches.

[0103] In operation S110, the memory device 1100 may receive a command including target plane information from the memory controller 1200. The command may be input through input/output lines (see FIG. 2, IO1 to IO_n). The command may be a data loading command for loading data into cache latches of the page buffer circuit 1130. The memory device 1100 may temporarily store data in the cache latches before programming data to the memory cell array 1110.

[0104] In operation S120, the memory device 1100 may receive addresses from the memory controller 1200. The addresses may include a column address CA and a row address RA. The row address may include a plane selection address for selecting one plane, a block selection address for selecting one memory block, and a word line selection address for selecting one word line.

[0105] In operation S130, the memory device 1100 may initialize cache latches corresponding to one or more target planes. The cache latch initialization operation may be performed while receiving addresses. The cache latch initialization operation may be performed through a cache latch initialization signal (see FIG. 7, DI). The cache latch

initialization signal DI may be provided from the cache latch control logic 2000.

[0106] In operation S140, the memory device 1100 may receive data from the memory controller 1200 and load the data into the initialized cache latches. And then, the memory device 1100 may provide the data stored in the cache latches to the most significant bit latch ML or the least significant bit latch LL through a dump operation. The memory device 1100 may program the data stored in the page buffer circuit 1130 to the memory cells of the memory cell array 1110.

[0107] FIGS. 10 to 15 are timing diagrams illustrating examples of the cache latch initialization operation of the memory device illustrated in FIG. 9 according to some implementations. In FIG. 10, the memory device 1100 may receive a command, addresses, and data from the memory controller 1200 through input/output lines IOx. When the number of input/output lines IOx is 8, the memory device 1100 may receive input in byte units. One byte is a data unit composed of 8 bits.

[0108] The command may include target plane information. The target plane information is plane information for initializing cache latches of a specific plane during a cache latch initialization operation. For example, the target plane information may be 8xh. Hexa code 8 is 1000 in binary code, and hexa code x may include plain information.

[0109] When the memory device 1100 initializes a large number of cache latches simultaneously, a large peak current may occur. In order to reduce the peak current, it is necessary to divide it into several units and initialize them sequentially. This may require a lot of initialization time.

[0110] The memory device 1100 has a limited time required to perform a program operation. In FIG. 10, the time from command input to data loading is fixed. 2 cycles of column address CA and 4 cycles of row address RA may be input during tWC time, respectively. tWC stands for Write Cycle Time, which means the time it takes to write data in the memory device 1100.

tADL stands for Address to Data Loading Time, which means the time from the rising edge of the write enable signal of the last address cycle to the rising edge of the write enable signal of the first data cycle in a program operation.

[0111] The time required for the memory device 1100 to perform a cache latch initialization operation is limited. The memory device 1000 may sequentially perform command input, address input, and data loading operations. If the address is input and the cache latches are initialized after confirming the plain address, the initialization operation may not be completed within the specified time.

[0112] For this reason, conventional memory devices start initializing the cache latches immediately after the command is input, and initialize the cache latches for all planes without confirming the address. Since conventional memory devices initialize the cache latches for all planes, a large peak current may occur. This problem may be more severe as the number of planes increases.

[0113] The cache latch control logic 2000 may receive target plane information during program operation, and selectively initializes cache latches according to the target plane information. The cache latch control logic 2000 may complete the program operation within a limited time and reduce peak current.

[0114] In FIGS. 10 and 11, when the hexa code x is 0, the binary code is 0000, and 80h may be a data loading command that uses all planes as target plane information. When the data loading command is 80h, the first to fourth cache latch initialization signals DI1 to DI4 may be provided to the first to fourth cache latches CL1 to CL4. The first to fourth cache latches CL1 to CL4 may be initialized by the first to fourth cache latch initialization signals DI1 to DI4, respectively.

[0115] In FIGS. 10 and 12, when the hexa code x is 1, the binary code is 0001, and 81h may be a data loading command that uses the first plane as plane information. When the data

loading command is 81h, the first cache latch initialization signals DI1 may be provided to the first cache latches CL1. The first cache latches CL1 may be initialized by the first cache latch initialization signal DI1.

[0116] In FIGS. 10 and 13, when the hexa code x is 2, the binary code is 0010, and 82h may be a data loading command that uses the second plane as plane information. When the data loading command is 82h, the second cache latch initialization signals DI2 may be provided to the second cache latches CL2. The second cache latches CL2 may be initialized by the second cache latch initialization signal DI2.

[0117] In FIG. 10 and FIG. 14, when the hexa code x is 3, the binary code is 0011, and 83h may be a data loading command that uses the third plane as plane information. When the data loading command is 83h, the third cache latch initialization signals DI3 may be provided to the third cache latches CL3. The third cache latches CL3 may be initialized by the third cache latch initialization signal DI3.

[0118] In FIG. 10 and FIG. 15, when the hexa code x is 4, the binary code is 0100, and 84h may be a data loading command that uses the fourth plane as plane information. If the data loading command is 84h, the fourth cache latch initialization signals DI4 may be provided to the fourth cache latches CL4. The fourth cache latches CL4 may be initialized by the fourth cache latch initialization signal DI4.

[0119] In FIG. 10, the memory device 1100 may load the data loading command 8xh, the column address CA, the row address RA, and the data through the input/output lines IOx. The data loading command 8xh may include target plane information. The data loading command 8xh may be matched one-to-one with each plane. For example, 80h may be matched with all planes, 81h may be matched with the first plane, 82h may be matched with the second plane, 83h may be matched with the third plane, and 84h may be matched with the fourth plane. The data loading command may have different commands for each plane.

[0120] The cache latch control logic 2000 may receive target plane information during program operation, and selectively initialize the first to fourth cache latches CL1 to CL4 according to the target plane information. The cache latch control logic 2000 may complete the cache latch initialization operation within a limited time and reduce peak current.

[0121] FIGS. 16A to 16D are block diagrams illustrating examples of memory devices including various numbers of planes according to some implementations. In FIGS. 16A to 16D, each of the memory devices 1100A to 1100D may include a plurality of planes, page buffer drivers matching each plane, and cache latches.

[0122] In FIG. 16A, the memory device 1100A may include two planes Plane1 and Plane2. The memory device 1100A may include a first page buffer driver PBD1 that correspond to the first plane and a second page buffer driver PBD2 matching the second plane. The first page buffer driver PBD1 may initialize the first cache latches CL1. The second page buffer driver PBD2 may initialize the second cache latches CL2.

[0123] In FIG. 16B, the memory device 1100B may include four planes Plane1 to Plane4. The memory device 1100B may include first to fourth page buffer drivers PBD1 to PBD4 that correspond to the first to fourth planes, respectively. The first to fourth page buffer drivers PBD1 to PBD4 may initialize the first to fourth cache latches CL1 to CL4, respectively.

[0124] In FIG. 16C, the memory device 1100C may include six planes Plane1 to Plane6. The memory device 1100C may include first to sixth page buffer drivers PBD1 to PBD6 that correspond to the first to sixth planes, respectively. Each of the first to sixth page buffer drivers PBD1 to PBD6 may initialize the first to sixth cache latches CL1 to CL6, respectively.

[0125] In FIG. 16D, the memory device 1100D may include eight planes Plane1 to Plane8. The memory device 1100D may include first to eighth page buffer drivers PBD1 to PBD8 that correspond to the first to eighth planes, respectively. Each of the first to eighth page buffer drivers PBD1 to PBD8 may initialize the first to eighth cache latches CL1 to CL8,

respectively.

[0126] FIG. 17 is a diagram illustrating examples of peak currents generated during a program operation of the memory devices illustrated in FIGS. 16A to 16D according to some implementations. The memory cell array may include a plurality of planes and page buffers matching each plane. The number of page buffers may also increase proportionally as the number of planes increases.

[0127] According to some implementations, when the number of planes is 2, the number of page buffers may be 32 KB. When the number of planes is 4, the number of page buffers may be 64 KB. When the number of planes is 6, the number of page buffers may be 96 KB. When the number of planes is 8, the number of page buffers may be 128 KB. In this case, the peak current generated by the initialization of the cache latches may increase in proportion to the number of planes or the number of page buffers.

[0128] In FIG. 17, when the number of planes is 2, the peak current may be 223.3 mA during the cache latch initialization operation. When the number of planes is 4, the peak current may be 446.6 mA. When the number of planes is 6, the peak current may be 669.9 mA. When the number of planes is 8, the peak current may be 893.2 mA.

[0129] In this case, a method of increasing the initialization allowance time may be considered to reduce the increased peak current. However, if the initialization allowance time is increased, the time required for the program operation of the memory device 1100 may increase. It may be impossible to avoid a degradation in the performance of the entire program operation.

[0130] The memory device 1100 may complete the cache latch initialization operation within the initialization allowance time and reduce the peak current by receiving target plane information during a program operation and selectively initializing cache latches according to the target plane information.

[0131] FIGS. 18 to 21 are diagrams illustrating examples of the cache latch initialization operation of the memory device illustrated in FIG. 16C according to some implementations. In FIG. 18, the memory device 1100C may include first to sixth planes Plane1 to Plane6. The memory device 1100C may include first to sixth page buffer drivers PBD1 to PBD6 and first to sixth cache latches CL1 to CL6 corresponding to the first to sixth planes, respectively.

[0132] The memory device 1100C may perform a cache latch initialization operation by matching target plane information included in the command with the input/output lines IOx. For example, the first input/output line IO1 may be matched with the first plane. The second input/output line IO2 may be matched with the second plane. The third to sixth input/output lines IO3 to IO6 may be matched with the third to sixth planes, respectively. The seventh and eighth input/output lines IO7 and IO8 may be set to 1.

[0133] In FIGS. 18 and 19, with reference to Example 1, the target plane may be the first plane. The first plane may be matched with the first input/output line IO1. When the target plane is the first plane, IO[8:1] may be 1100 0001, and the hexa code may be C1h. When the data loading command is C1h, the first cache latches CL1 matching the first plane may be initialized.

[0134] In FIGS. 18 and 20, with reference to Example 2, the target planes may be the second plane, the fourth plane, and the sixth plane. The second plane may be matched with the second input/output line IO2, the fourth plane may be matched with the fourth input/output line IO4, and the sixth plane may be matched with the sixth input/output line IO6. When the target planes are the second, fourth, and sixth planes, IO[8:1] may be 1110 1010, and the hexa code may be EAh. When the data loading command is EAh, the second, fourth, and sixth cache latches CL2, CL4, and CL6 matching the second, fourth, and sixth planes may be initialized.

[0135] In FIGS. 18 and 21, with reference to Example 3, the target planes may be the first to sixth planes. When the target planes are the first to sixth planes, IO[8:1] may be 1111 1111,

and the hexa code may be FFh. When the data loading command is FFh, the first to sixth cache latches CL1 to CL6 matching the first to sixth planes may all be initialized.

[0136] In FIG. 18, the cache latch control logic 2000 may receive a data loading command including target plane information during a program operation, and may selectively initialize the first to sixth cache latches CL1 to CL6 according to the target plane information. The data loading command may match the command bits of each input/output line with each plane. The cache latch control logic 2000 may complete the cache latch initialization operation within a limited time, and may reduce the peak current.

[0137] FIG. 22 is a diagram illustrating an example of a memory device having a multi-stack structure according to some implementations. The memory device with a multi-stack structure may perform the cache latch initialization operation described above. In FIG. 22, the memory device 3000 may have a first stack ST1 and a second stack ST2. The first stack ST1 may be located at the bottom, and the second stack ST2 may be located at the top.

[0138] A pillar of the memory device 3000 may be formed by bonding the first and second stacks ST1 and ST2. A plurality of dummy word lines (e.g., Dummy1 WL and Dummy2 WL) may be included at junctions of the first and second stacks ST1 and ST2. The first stack ST1 may be positioned between the common source line CSL and the first dummy word line Dummy1 WL. The second stack ST2 may be positioned between the second dummy word line Dummy2 WL and the bit line BL.

[0139] The first stack ST1 may include a ground selection line GSL, a first edge word line Edge1 WL, and first stack word lines Stack1 WLs. The second stack ST2 may include second stack word lines Stack2 WLs and second edge word lines Edge2 WL. Memory cells connected to the first and second edge word lines Edge1 WL and Edge2 WL may store bit data different from the other memory cells. For example, memory cells connected to the first and second edge word lines Edge1 WL and Edge2 WL may be SLC or MLC, and memory

cells connected to the other word lines may be TLC or QLC.

[0140] FIG. 23 is a block diagram illustrating an example in which a storage device is implemented with a solid state drive (SSD) according to some implementations. In FIG. 23, an SSD 4000 may include a plurality of memory devices 4101 to 4104 and an SSD controller 4200.

[0141] The first and second memory devices 4101 and 4102 may be connected with the SSD controller 4200 through a first channel CH1. The third and fourth memory devices 4103 and 4104 may be connected with the SSD controller 4200 through a second channel CH2. The number of channels connected with the SSD controller 4200 may be 2 or more. The number of memory devices connected with one channel may be 2 or more.

[0142] The SSD controller 4200 may include a host interface 4201, a memory interface 4202, a buffer interface 4203, a control unit 4210, and a work memory 4220. The SSD controller 4200 may be connected with a host 1500 through the host interface 4201. Depending on a request of the host 1500, the SSD controller 4200 may write data in the corresponding memory device or may read data from the corresponding memory device.

[0143] The SSD controller 4200 may be connected with the plurality of memory devices 4101 to 4104 through the memory interface 4202 and may be connected with a buffer memory 1300 through the buffer interface 4203. The memory interface 4202 may provide data, which are temporarily stored in the buffer memory 1300, to the plurality of memory devices through the channels CH1 and CH2. The memory interface 4202 may transfer the data read from the plurality memory devices 4101 to 4104 to the buffer memory 1300.

[0144] The control unit 4210 may analyze and process the signal received from the host 1500. The control unit 4210 may control the host 1500 or the plurality memory devices 4101 to 4104 through the host interface 4201 or the memory interface 4202. The control unit 4210 may control operations of the plurality memory devices 4101 to 4104 by using firmware for

driving the SSD 4000.

[0145] The SSD controller 4200 may manage data to be stored in the plurality of memory devices 4101 to 4104. In a sudden power-off event, the SSD controller 4200 may back up the data stored in the work memory 4220 or the buffer memory 1300 to the plurality of memory devices 4101 to 4104.

[0146] According to the present disclosure, a memory device may complete a cache latch initialization operation within an initialization allowable time and reduce peak current by receiving a command including target plane information during a program operation and selectively initializing cache latches according to the target plane information. While this disclosure contains many specific implementation details, these should not be construed as limitations on the scope of what may be claimed, equivalents thereof, as well as claims to be described later. Certain features that are described in this disclosure in the context of separate implementations can also be implemented in combination in a single implementation. Conversely, various features that are described in the context of a single implementation can also be implemented in multiple implementations separately or in any suitable subcombination. Moreover, although features may be described above as acting in certain combinations, one or more features from a combination can in some cases be excised from the combination, and the combination may be directed to a subcombination or variation of a subcombination.

WHAT IS CLAIMED IS:

1. A memory device, comprising:
 - a memory cell array including a first plane and a second plane;
 - a page buffer circuit including first cache latches configured to store data in the first plane and second cache latches configured to store data in the second plane; and
 - input/output lines configured to receive a command and addresses from a memory controller,wherein the command includes target plane information configured to initialize at least one of the first cache latches and the second cache latches.
2. The memory device of claim 1, wherein the memory device is configured to initialize cache latches of a target plane according to the command.
3. The memory device of claim 2, further comprising a cache latch control logic configured to provide, to the page buffer circuit, a first cache latch initialization signal for initializing the first cache latches and a second cache latch initialization signal for initializing the second cache latches.
4. The memory device of claim 2 or claim 3, wherein the command comprises different commands for each of the first plane, the second plane, and the target plane.
5. The memory device of any one of claims 2 to 4, wherein the command is configured to be one-to-one matched with the first plane, the second plane, and the target plane.

6. The memory device of any one of claims 2 to 5, wherein command bits of each input/output line are configured to be matched with the first plane, the second plane, and the target plane.

7. The memory device of claim 6,
wherein the first cache latches are configured to be initialized based on a command bit of a first input/output line being 1, and

wherein the second cache latches are configured to be initialized based on a command bit of a second input/output line being 1.

8. The memory device of claim 6, wherein the first cache latches and the second cache latches are both configured to be initialized based on command bits of first and second input/output lines all being 1.

9. The memory device of any one of claims 3 to 8, wherein the cache latch control logic includes:

a first page buffer driver configured to generate the first cache latch initialization signal and provide the first cache latch initialization signal to the first cache latches according to the target plane information; and

a second page buffer driver configured to generate the second cache latch initialization signal and provide the second cache latch initialization signal to the second cache latches according to the target plane information.

10. The memory device of any one of claims 3 to 9, further comprising:

third to n-th planes; and

third to n-th cache latches,

wherein the cache latch control logic is configured to initialize the first cache latches, the second cache latches, and the third to n-th cache latches according to the command.

11. A memory controller for controlling a memory device,

the memory device comprising:

a memory cell array including a first plane and a second plane;

a page buffer circuit including first cache latches configured to store data in the first plane and second cache latches configured to store data in the second plane; and

a cache latch control logic configured to provide, to the page buffer circuit, a first cache latch initialization signal for initializing the first cache latches and a second cache latch initialization signal for initializing the second cache latches,

wherein the memory controller is configured to provide a command comprising target plane information to the memory device during a program operation, and

wherein at least one of the first cache latches and the second cache latches are configured to be selectively initialized according to the target plane information.

12. The memory controller of claim 11, wherein the command is configured to have different commands for each of the first plane and the second plane.

13. The memory controller of claim 11 or claim 12, wherein the command is configured to be one-to-one matched with the first plane and the second plane.

14. The memory controller of any one of claims 11 to 13, wherein command bits of

input/output lines are matched with the first plane and the second plane.

15. The memory controller of claim 14,

wherein the first cache latches are configured to be initialized based on a command bit of a first input/output line being 1, and

wherein the second cache latches configured to be are initialized based on a command bit of a second input/output line being 1.

16. A cache latch initialization method of a memory device connected to a memory controller through input/output lines,

the memory device comprising:

a memory cell array including first to n-th planes;

a page buffer circuit including first to n-th cache latches, first cache latches configured to store data in the first plane, and the n-th cache latches configured to store data in the n-th plane;

a cache latch control logic configured to generate first to n-th cache latch initialization signals, the first cache latch initialization signal configured to initialize the first cache latches, the n-th cache latch initialization signal configured to initialize the n-th cache latches, and provide the first to n-th cache latch initialization signals to the page buffer circuit,

wherein the cache latch initialization method comprises:

receiving target plane information during a program operation; and

providing, according to the target plane information, one of the first cache latch initialization signal to the first cache latches or the n-th cache latch initialization signal to the n-th cache latches.

17. The cache latch initialization method of claim 16,

wherein the program operation includes:

receiving a command including the target plane information from the memory controller;

receiving column addresses and row addresses from the memory controller;

and

receiving data from the memory controller, and

wherein the first to n-th cache latch initialization signals are provided during receiving the column addresses and/or the row addresses.

18. The cache latch initialization method of claim 17, wherein the command is configured to have a different command for each of the first to n-th planes.

19. The cache latch initialization method of claim 17 or claim 18, wherein the command is configured to be one-to-one matched with each of the first to n-th planes.

20. The cache latch initialization method of any one of claims 17 to 19, wherein command bits of input/output lines are matched with each of the first to n-th planes.