C L A I M S

1. A storage system comprising:

a ~~wafer~~ first stocker that is capable of storing a plurality of ~~semiconductor wafers~~memory devices, each of the plurality of ~~semiconductor wafers~~memory devices including a plurality of non-volatile memory ~~devices that are formed therein~~chips;

a ~~cassetter~~ mounter configured to ~~accommodate~~ mount at least one of the plurality of memory devices~~semiconductor wafers~~ in a ~~cassette~~ case ~~that is capable of accommodating at least one of the plurality of semiconductor wafers~~;

a second~~wafer cassette~~ stocker that is capable of storing a case-mounted memory device~~wafer cassette~~, the case-mounted memory device~~wafer cassette~~ including ~~a~~ the ~~cassette~~ case and the at least one of the plurality of memory devices mounted ~~a semiconductor wafer accommodated~~ in the ~~cassette~~ case;

a host apparatus including at least one slot to which the case-mounted memory device~~wafer cassette~~ is connectable, ~~and~~ the host apparatus being configured to read ~~and~~ or write data from ~~and~~ or to the at least one of the plurality of memory devices ~~semiconductor wafer~~ included in the case-mounted memory device~~wafer cassette~~ connected to the slot;

a first ~~wafer~~ transport device configured to transport the plurality of memory devices ~~semiconductor wafer~~ between the ~~wafer~~ first stocker and the mounter~~cassetter~~; and

a second~~wafer cassette~~ transport device configured to transport the case-mounted memory device~~wafer cassette~~ among the mounter~~cassetter~~, the second~~wafer cassette~~ stocker, and the host apparatus, wherein

the host apparatus is further configured to:

determine a first ~~semiconductor wafer~~memory device to be accessed among the plurality of memory devices~~semiconductor wafers~~;

when ~~the wafer cassette~~a first case-mounted memory device, which is the case-mounted memory device ~~to be accessed~~ that includes the first ~~semiconductor wafer~~memory device, is connected to the slot of the host apparatus, execute reading or writing of data from or to the first ~~semiconductor wafer~~memory device;

when the ~~wafer cassette~~first case-mounted memory device ~~to be accessed~~ is not connected to the slot of the host apparatus and is stored in the second~~wafer cassette~~ stocker, cause the ~~wafer cassette~~second transport device to transport the ~~wafer cassette~~first case-mounted memory device ~~to be accessed,~~ to the slot of the host apparatus, and to connect ~~it~~ the first case-mounted memory device to the slot; and

when the ~~wafer cassette~~first case-mounted memory device ~~to be accessed~~ is not connected to the slot of the host apparatus and is not stored in the ~~wafer cassette~~second stocker, cause the ~~wafer~~ first transport device to transport the first ~~semiconductor wafer~~memory device from the ~~wafer~~ first stocker to the mounter~~cassetter~~, cause the mounter~~cassetter~~ to ~~accommodate~~ mount the transported first ~~semiconductor wafer~~ memory device in the ~~cassette~~ case for assembling the first case-mounted memory device, and cause the ~~wafer cassette~~second transport device to transport the ~~wafer cassette~~first case-mounted memory device ~~to be accessed that includes the first semiconductor wafer,~~ to the slot of the host apparatus, and to connect ~~it~~ the first case-mounted memory device to the slot.

2. The storage system of claim 1, wherein

the host apparatus is configured to:

when the ~~wafer cassette~~first case-mounted memory device ~~to be accessed~~ that is connected to the slot is not recognized as a storage device,

cause the ~~wafer cassette~~second transport device to remove the ~~wafer cassette~~first case-mounted memory device ~~to be accessed~~ from the slot and to reconnect ~~it~~ the first case-mounted memory device to the slot.

~~3. The storage system of claim 2, wherein~~

~~the host apparatus is configured to:~~

~~when, even after the reconnecting, the wafer cassette to be accessed that is connected to the slot is still not recognized as a storage device,~~

~~cause the wafer cassette transport device to transport the wafer cassette to be accessed, from the slot of the host apparatus to the cassetter,~~

~~cause the cassette transport device to disassemble the transported wafer cassette to be accessed, and to accommodate the first semiconductor wafer removed from the wafer cassette to be accessed, in a first cassette case that is the cassette case obtained by disassembling the wafer cassette to be accessed,~~

~~cause the wafer cassette transport device to transport and connect a wafer cassette including the first cassette case and the first semiconductor wafer to the slot of the host apparatus,~~

~~when, even after reconnecting the wafer cassette including the first cassette case, the wafer cassette including the first cassette case and being connected to the slot is not recognized as a storage device,~~

~~cause the wafer cassette transport device to transport the wafer cassette including the first cassette case from the slot of the host apparatus to the cassetter,~~

~~cause the cassetter to disassemble the transported wafer cassette including the first cassette case, and to accommodate the first semiconductor wafer removed from the wafer cassette including the first cassette~~

~~case, in a second cassette case which is different from the first cassette case; and~~

~~cause the wafer cassette transport device to transport the wafer cassette including the second cassette case and the first semiconductor wafer to the slot of the host apparatus, and to connect it to the slot.~~

~~4~~3. The storage system of claim 1, wherein

the host apparatus is configured to:

manage a priority of each of the plurality of memory devices~~semiconductor wafers~~, and

control a location where each of the plurality of memory devices~~semiconductor wafers~~ is present, based on the priority of each of the plurality of memory devices~~semiconductor wafers~~, such that the ~~wafer cassette~~case-mounted memory device including a ~~semiconductor wafer~~memory device having a priority of a first level is connected to the slot of the host apparatus, the ~~wafer cassette~~case-mounted memory device including a ~~semiconductor wafer~~memory device having a priority of a second level lower than the first level is stored in the ~~wafer cassette~~second stocker, and a ~~semiconductor wafer~~memory device having a priority of a third level lower than the second level is stored in the ~~wafer~~ first stocker.

~~5~~4. The storage system of claim ~~4~~3, wherein

the host apparatus is configured to:

when ~~a~~ the priority of a second ~~semiconductor wafer~~memory device among the plurality of memory devices~~semiconductor wafers~~ stored in the ~~wafer~~ first stocker is raised from the third level to the second level,

cause the ~~wafer~~ first transport device to transport the second ~~semiconductor wafer~~memory device from the ~~wafer~~ first stocker to the ~~cassetter~~mounter,

cause the mounter~~cassetter~~ to ~~accommodate~~ mount the transported second ~~semiconductor wafer~~memory device in the ~~cassette~~ case for assembling a second case-mounted memory device, and

cause the ~~wafer cassette~~ second transport device to transport the ~~wafer cassette~~second case-mounted memory device ~~including the second semiconductor wafer~~ from the mounter~~cassetter~~ to the ~~wafer cassette~~second stocker.

~~6. The storage system of claim 1, wherein~~

~~a plurality of electrodes are formed on the semiconductor wafer,~~

~~the cassette case includes:~~

~~a lower case on which the semiconductor wafer is capable of being placed;~~

~~an upper case;~~

~~a probe card including a plurality of probe pins contactable to the plurality of electrodes of the semiconductor wafer placed on the lower case; and~~

~~a controller configured to execute reading or writing of data from or to at least one of the plurality of nonvolatile memory devices through the probe card based on a read request and a write request received from the host apparatus, and~~

~~the cassetter is configured to bring the plurality of electrodes and the plurality of probe pins into contact with each other by joining the upper case and the lower case on which the semiconductor wafer is placed to each other.~~

~~7. The storage system of claim 6, wherein~~

~~the lower case includes a heater that raising a temperature of the semiconductor wafer placed on the lower case, and~~

~~the heater is driven by electric power supplied from the host apparatus when the wafer cassette is connected to the slot of the host apparatus.~~

~~8. The storage system of claim 6, wherein~~

~~the lower case includes three or more centering members, the three or more centering members being arranged at equal intervals from each other along a circumference having a predetermined radius from a center of a wafer mounting region in the lower case, and three or more centering members being movable toward the center of the wafer mounting region, and~~

~~the cassetter aligns a center of the semiconductor wafer placed on the lower case with the center of the wafer mounting region by moving the three or more centering members toward the center of the wafer mounting region.~~

~~9. The storage system of claim 6, wherein~~

~~one of the upper case and the lower case includes a groove, and~~

~~the other of the upper case and the lower case includes a protruding member that is to be fitted into the groove.~~

~~10. The storage system of claim 6, wherein~~

~~the probe card includes:~~

~~a first surface on which the plurality of probe pins are provided, and~~

~~a second surface on an opposite side to the first surface, and~~

~~the probe card is provided in the upper case so as to expose at least the second surface to outside of the cassette case.~~

~~11. The storage system of claim 6, wherein~~

~~the upper case includes a plurality of protruding portions that abut a region on a surface of the semiconductor wafer placed on the lower case when the upper case and the lower case are joined to each other, the region being a region other than the plurality of electrodes on the surface of the semiconductor wafer.~~

~~12. The storage system of claim 6, wherein~~

~~the upper case include a cushion material that abuts a region on a surface of the semiconductor wafer placed on the lower case and contracts when the upper case and the lower case are joined to each other, the region being a region other than the plurality of electrodes on the surface of the semiconductor wafer,~~

~~each of the plurality of probe pins is connected to the probe card via a conductive member having elasticity, and~~

~~when the upper case and the lower case are joined together, each of the plurality of probe pins is contact with a corresponding electrode and the conductive member contracts.~~

~~13. The storage system of claim 6, wherein~~

~~in each of the plurality of semiconductor wafers stored in the wafer stocker, edge processing to uniformize diameters of the plurality of semiconductor wafers to a first length has been subjected.~~

~~14. The storage system of claim 1, wherein~~

~~the wafer stocker includes a first side plate having a first opening,~~

~~the cassetter includes a second side plate opposing the first side plate of the wafer stocker, the second side plate having a second opening disposed in a position opposing the first opening, and~~

~~the wafer transport device transports the semiconductor wafer between the wafer stocker and the cassetter through the first opening and the second opening.~~

~~15. The storage system of claim 14, wherein~~

~~the wafer transport device includes a first robot arm disposed in the wafer stocker and a second robot arm disposed in the cassetter, and~~

~~the semiconductor wafer is passed between the first robot arm and the second robot arm through the first opening and the second opening.~~

~~16. The storage system of claim 15, wherein~~

~~the first robot arm is disposed in a central position between a front surface and a rear surface of the wafer stocker, and~~

~~in the wafer stocker, each of a first space between the first robot arm and the front surface and a second space between the first robot arm and the rear surface is capable of being storing the semiconductor wafer.~~

~~17. The storage system of claim 14, wherein~~

~~the cassetter includes a third side plate located on an opposite to the second side plate, and the third side plate having a third opening,~~

~~the wafer cassette stocker includes a fourth side plate opposing the third side plate of the cassetter and a fifth side plate located on an opposite side to the fourth side plate, the fourth side plate having a fourth opening located at a position opposing the third opening, and the fifth side plate having a fifth opening,~~

~~the host apparatus is included in a server rack, and the server rack including a sixth side plate opposing the fifth side plate of the wafer stocker, and the sixth side~~

~~plate having a sixth opening located at a position opposing the fifth opening, and~~

~~the wafer cassette transport device is configured to:~~

~~transport the wafer cassette between the cassetter and the wafer cassette stocker, through the third opening and the fourth opening; and~~

~~transport the wafer cassette between the wafer cassette stocker and the server rack including the host apparatus, through the fifth opening and the sixth opening.~~

~~18. The storage system of claim 17, wherein~~

~~the wafer transport device includes a first robot arm disposed in the wafer stocker and a second robot arm disposed in the cassetter,~~

~~the wafer cassette transport device includes a third robot arm disposed in the wafer cassette stocker and a fourth robot arm disposed in the server rack including the host apparatus,~~

~~the semiconductor wafer is passed between the first robot arm and the second robot arm through the first opening and the second opening, and~~

~~the wafer cassette is passed between the second robot arm and the third robot arm through the third opening and the fourth opening, and is passed between the third robot arm and the fourth robot arm through the fifth opening and the sixth opening.~~

~~19~~5. The storage system of claim 1, wherein

the ~~wafer cassette~~case includes a plug terminal, and

the host apparatus includes:

a host case including the slot; and

a receptacle terminal provided in the host case, which is connected to the plug terminal of the ~~cassette~~ case when

the ~~cassette~~ case-mounted memory device is inserted to the slot.

6. The storage system of claim 1, wherein

the plurality of memory devices is a plurality of semiconductor wafers, respectively,

the first stocker is capable of storing the plurality of semiconductor wafers,

the case is a cassette case that is capable of accommodating at least one of the plurality of semiconductor wafers,

the mounter is configured to accommodate the at least one of the plurality of semiconductor wafers in the cassette case,

the second stocker is capable of storing a wafer cassette, the wafer cassette including the cassette case and the at least one of the plurality of semiconductor wafers accommodated in the cassette case,

the first transport device is configured to transport the plurality of semiconductor wafers between the first stocker and the mounter,

the second transport device is configured to transport the wafer cassette among the mounter, the second stocker, and the host apparatus,

the host apparatus includes the at least one slot to which the wafer cassette is connectable, and configured to read or write data from or to the at least one of the plurality of semiconductor wafers included in the wafer cassette connected to the slot, and

the host apparatus is configured to:

determine a first semiconductor wafer to be accessed among the plurality of semiconductor wafers;

when a first wafer cassette, which is the wafer cassette that includes the first semiconductor wafer, is

connected to the slot of the host apparatus, execute reading or writing of data from or to the first semiconductor wafer;

when the first wafer cassette is not connected to the slot of the host apparatus and is stored in the second stocker, cause the second transport device to transport the first wafer cassette to the slot of the host apparatus, and to connect the first wafer cassette to the slot; and

when the first wafer cassette is not connected to the slot of the host apparatus and is not stored in the second stocker, cause the first transport device to transport the first semiconductor wafer from the first stocker to the mounter, cause the mounter to accommodate the transported first semiconductor wafer in the cassette case for assembling the first wafer cassette, and cause the second transport device to transport the first wafer cassette to the slot of the host apparatus, and to connect the first wafer cassette to the slot.

7. The storage system of claim 6, wherein

the host apparatus is configured to:

when the first wafer cassette that is connected to the slot is not recognized as a storage device,

cause the second transport device to remove the first wafer cassette from the slot and to reconnect the first wafer cassette to the slot.

8. The storage system of claim 6, wherein

the host apparatus is configured to:

manage a priority of each of the plurality of semiconductor wafers, and

control a location where each of the plurality of semiconductor wafers is present, based on the priority of each of the plurality of semiconductor wafers, such that the wafer cassette including a semiconductor wafer having a

priority of a first level is connected to the slot of the host apparatus, the wafer cassette including a semiconductor wafer having a priority of a second level lower than the first level is stored in the second stocker, and a semiconductor wafer having a priority of a third level lower than the second level is stored in the first stocker.

9. The storage system of claim 8, wherein

the host apparatus is configured to:

when the priority of a second semiconductor wafer among the plurality of semiconductor wafers stored in the first stocker is raised from the third level to the second level,

cause the first transport device to transport the second semiconductor wafer from the first stocker to the mounter,

cause the mounter to accommodate the transported second semiconductor wafer in the cassette case for assembling a second wafer cassette, and

cause the second transport device to transport the second wafer cassette from the mounter to the second stocker.

10. The storage system of claim 6, wherein

a plurality of electrodes is formed on each of the plurality of semiconductor wafers,

the cassette case includes:

a lower case on which the at least one of the plurality of semiconductor wafers is capable of being placed;

an upper case;

a probe card including a plurality of probe pins contactable to the plurality of electrodes of the at least one of the plurality of semiconductor wafers placed on the lower case; and

a controller configured to execute reading or writing of data from or to at least one of the plurality of

nonvolatile memory chips through the probe card based on a read request or a write request received from the host apparatus, and

the mounter is configured to bring the plurality of electrodes and the plurality of probe pins into contact with each other by joining the upper case and the lower case on which the at least one of the plurality of semiconductor wafers is placed, to each other.

11. The storage system of claim 10, wherein

the lower case includes three or more centering arms, the three or more centering arms being arranged at equal intervals from each other along a circumference having a predetermined radius from a center of a wafer mounting region in the lower case, the three or more centering arms being movable toward the center of the wafer mounting region, and

the mounter aligns a center of the at least one of the plurality of semiconductor wafers placed on the lower case with the center of the wafer mounting region by moving the three or more centering members toward the center of the wafer mounting region.

12. The storage system of claim 10, wherein

one of the upper case and the lower case includes a groove, and

the other of the upper case and the lower case includes a protruding portion that is to be fitted into the groove.

13. The storage system of claim 10, wherein

the upper case includes a plurality of protruding portions that abut a region on a surface of the at least one of the plurality of semiconductor wafers placed on the lower case when the upper case and the lower case are joined to each other, the region being a region other than the

plurality of electrodes on the surface of the at least one of the plurality of semiconductor wafers.

14. The storage system of claim 10, wherein

the upper case includes a cushion material that abuts a region on a surface of the at least one of the plurality of semiconductor wafers placed on the lower case and contracts when the upper case and the lower case are joined to each other, the region being a region other than the plurality of electrodes on the surface of the at least one of the plurality of semiconductor wafers,

each of the plurality of probe pins is connected to the probe card via a conductive elastic member, and

when the upper case and the lower case are joined together, each of the plurality of probe pins is contact with a corresponding electrode, and the conductive elastic member contracts.

15. The storage system of claim 10, wherein

in each of the plurality of semiconductor wafers stored in the first stocker, edge processing to uniformize diameters of the plurality of semiconductor wafers to a first length has been subjected.

16. The storage system of claim 6, wherein

the first stocker includes a first side plate having a first opening,

the mounter includes a second side plate opposing the first side plate of the first stocker, the second side plate having a second opening disposed in a position opposing the first opening, and

the first transport device is configured to transport the plurality of semiconductor wafers between the first

stocker and the mounter through the first opening and the second opening.

17. The storage system of claim 16, wherein

the first transport device includes a first robot arm disposed in the first stocker and a second robot arm disposed in the mounter, and

each of the plurality of semiconductor wafers is configured to be passed between the first robot arm and the second robot arm through the first opening and the second opening.

18. The storage system of claim 16, wherein

the mounter includes a third side plate located on an opposite to the second side plate, and the third side plate having a third opening,

the second stocker includes a fourth side plate opposing the third side plate of the mounter and a fifth side plate located on an opposite side to the fourth side plate, the fourth side plate having a fourth opening located at a position opposing the third opening, and the fifth side plate having a fifth opening,

the host apparatus is included in a server rack, and the server rack including a sixth side plate opposing the fifth side plate of the second stocker, and the sixth side plate having a sixth opening located at a position opposing the fifth opening, and

the second transport device is configured to:

transport the wafer cassette between the mounter and the second stocker, through the third opening and the fourth opening; and

transport the wafer cassette between the second stocker and the server rack including the host apparatus, through the fifth opening and the sixth opening.

19. The storage system of claim 6, wherein the cassette case includes a plug terminal, and the host apparatus includes:

a host case including the slot; and

a receptacle terminal provided in the host case, which is connected to the plug terminal of the cassette case when the wafer cassette is inserted to the slot.

20. The storage system of claim 6, wherein each of the plurality of semiconductor wafers includes a redistribution layer,

a plurality of electrodes included in the redistribution layer are electrically connected to a plurality of electrodes of the nonvolatile memory chip, respectively, by internal wiring in the redistribution layer,

a size of each of the plurality of electrodes included in the redistribution layer is larger than a size of each of the plurality of electrodes of the nonvolatile memory chip, and

an interval between each other of the plurality of electrodes included in the redistribution layer is wider than an interval between each other of the plurality of electrodes of the nonvolatile memory chip.

~~20. The storage system of claim 1, wherein~~

~~each of the plurality of semiconductor wafers includes a redistribution layer,~~

~~a plurality of electrodes included in the redistribution layer are electrically connected to a plurality of electrodes of the nonvolatile memory device, respectively, by internal wiring in the redistribution layer,~~

~~a size of each of the plurality of electrodes included in the redistribution layer is larger than a size of each of the plurality of electrodes of the nonvolatile memory device, and~~

~~an interval between each other of the plurality of electrodes included in the redistribution layer is wider than an internal between each other of the plurality of electrodes of the nonvolatile memory device.~~