

SEMICONDUCTOR MEMORY

ABSTRACT

A semiconductor memory includes storage arrays, at least one verification module and gating circuits. Each verification module corresponds to multiple storage arrays. The verification module is configured to verify whether an error occurs in data information of the corresponding storage arrays. Each verification module is connected to a group of global data buses. The gating circuits are respectively connected to the storage arrays and the global data buses, and the gating circuits are configured to control on and off of a data transmission path connecting the global data buses to the storage arrays.

[Fig. 1]