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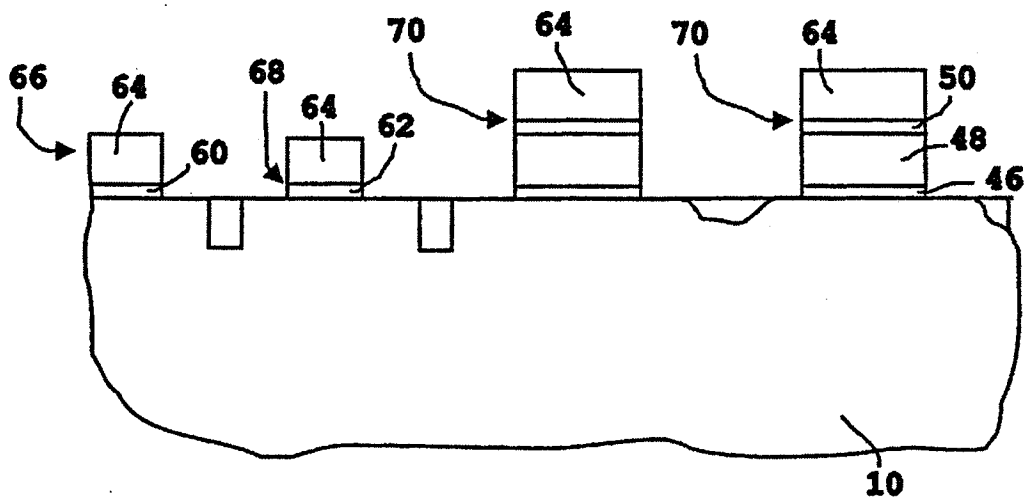
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(54) Title: NITRIDATION BARRIERS FOR NITRIDATED TUNNEL OXIDE FOR CIRCUITRY FOR FLASH MEMORY TECHNOLOGY AND FOR LOCOS/STI ISOLATION



(57) Abstract: An improved flash memory device, which has shallow trench isolation in the periphery region and LOCOS isolation in the core region is provided. A hard mask is used first to create the shallow trench isolation. The LOCOS isolation is then created. Subsequent etching is used to remove stringers. The flash memory is able to use shallow trench isolation to limit encroachment. The flash memory may also have a nitridated tunnel oxide layer. A hard mask is used to prevent nitride contamination of the gate oxide layer.

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NITRIDATION BARRIERS FOR NITRIDATED TUNNEL OXIDE FOR CIRCUITRY FOR FLASH MEMORY TECHNOLOGY AND FOR LOCOS/STI ISOLATION

TECHNICAL FIELD

The present invention relates to nonvolatile memory devices. Even more particularly, the present invention relates to flash memory utilizing periphery and core stacks.

BACKGROUND ART

Memory devices such as flash memory or electrically erasable programmable read only memory (EEPROM) are known. Memory devices such as flash memory comprise, core stacks, which hold the erasable programmable data, and periphery stacks which are used to program the core stacks. It is advantageous to manufacture periphery stacks and core stacks on the same chip, which is done in the prior art. However, sometimes it is desirable to use local oxidation of silicon (LOCOS) on part of the flash memory and shallow trench isolation (STI) on other parts of the flash memory. US-A-6004862 discloses a process for forming a semiconductor integrated circuit with core and periphery areas populated with active devices, by forming isolating regions in the said core or periphery areas. US-A-5712205 relates to a semiconductor isolation method for high density semiconductor devices, providing a wide isolation pitch on one area of a chip and a narrow isolation pitch on a different area of the pitch. EP-A-0751560 discloses a process for forming an integrated circuit providing at least one matrix of non-volatile memory cells with simultaneous provision in peripheral zones of different transistor types.

In the case where shallow trench isolation is used for the periphery stacks, corner recesses form around the shallow trench isolation for the periphery stacks, which are detrimental to the periphery stacks.

In addition, core stacks and periphery stacks require different manufacturing steps. Some of these different processing steps for the core stacks are harmful to the periphery stacks and vice versa. One example of these problems is related to the use of a nitrogen implant or other nitridation methods to improve the functionality of the tunnel oxide of the core stacks. In the prior art, such a nitrogen implant tends to contaminate the gate oxide of the periphery stack diminishing the performance of the gate oxide of the periphery stacks.

It is desirable to manufacture periphery stacks and core stacks on a single chip and minimizing damage to the periphery stacks and core stacks due to different processes required to manufacture the different stacks.

In addition, it is desirable to have periphery stacks with gate oxides of different thicknesses.

BRIEF SUMMARY OF THE INVENTION

Accordingly, the present invention involves the use of successive hard masks to provide STI and LOCOS isolation on a single chipand the fabrication of a flash memory device on a

substrate by using a hard mask to protect the periphery before forming a NITRIDATED tunnel oxide. Advantages of the present invention include the capability of fabricating a plurality of semiconductor devices on a single chip, wherein some of the devices are separated by shallow trench isolation and other devices are separated by local oxidation of silicon, the capability of fabricating a flash memory with a reduced contamination of the gate oxide, and the capability of fabricating a flash memory device with improved stack isolation.

Other features of the present invention are disclosed or apparent in the section entitled: "DETAILED DESCRIPTION OF THE INVENTION."

BRIEF DESCRIPTION OF DRAWINGS

For a fuller understanding of the present invention, reference is made to the accompanying drawings wherein:

Figure 1 is a cross sectional view of a semiconductor substrate used in a preferred embodiment of the invention;

Figure 2 is a cross sectional view of the substrate shown in figure 1, with trenches;

Figure 3 is a cross sectional view of the substrate shown in figure 2, with a trench oxide;

Figure 4 is a cross sectional view of the substrate shown in figure 3, with corner recesses;

Figure 5 is a cross sectional view of the substrate shown in figure 4, before LOCOS;

Figure 6 is a cross sectional view of the substrate shown in figure 5, with LOCOS;

Figure 7 is a cross sectional view of the substrate shown in figure 6, after the removal of the hard mask used for LOCOS;

Figure 8 is a cross sectional view of the substrate shown in figure 7, with a hard mask layer;

Figure 9 is a cross sectional view of the substrate shown in figure 8, with a tunnel oxide and first polysilicon layer;

Figure 10 is a cross sectional view of the substrate shown in figure 9, with an interpoly dielectric layer;

Figure 11 is a cross sectional view of the substrate shown in figure 10, with a first gate oxide layer;

Figure 12 is a cross sectional view of the substrate shown in figure 11, where the first gate oxide layer is etched back;

Figure 13 is a cross sectional view of the substrate shown in figure 12, after the photoresist mask has been removed;

Figure 14 is a cross sectional view of the substrate shown in figure 13, with thin and thick oxide layers; and

Figure 15 is a cross sectional view of the substrate shown in figure 14, with periphery stacks and core stacks.

Reference numbers refer to the same or equivalent parts of the present invention throughout the several figures of the drawing.

MODES FOR CARRYING OUT THE INVENTION

Figure 1 is a cross sectional view of a semiconductor substrate 10 used in a preferred embodiment of the invention. A pad oxide layer 12 is formed over a surface of the semiconductor substrate 10. A 1,000 to 2,000 Å first hard mask layer 14 is formed over the pad oxide layer 12. In the preferred embodiment of the invention, the first hard mask layer 14 is of the group consisting of silicon oxynitride (SiON), silicon nitride (Si_3N_4), and polysilicon. A photoresist mask 16 is formed over the first hard mask layer 14.

Regions of the first hard mask layer 14 that are not covered by the photoresist mask 16 are etched away to form apertures 18 in the first hard mask layer 14, as shown in figure 1. In this embodiment the apertures 18 are only over the periphery region and interface region of the semiconductor substrate 10.

The photoresist mask is removed and the semiconductor substrate 10 is subjected to an etch, which creates shallow trenches 20 in the semiconductor substrate 10 below the apertures 18 in the first hard mask layer 14, as shown in figure 2. In the preferred embodiment, the depths of the trenches 20 into the substrate surface is approximately 0.15 μ to 0.35 μ. A trench oxide 22 is formed in the trenches, as shown in figure 3.

The semiconductor substrate 10 is then subjected to an etch to remove the first hard mask layer, as shown in figure 4. In the preferred embodiment the substrate 10 is then subjected to a cleaning step and the top of the trench oxide 22 has corner recesses 24 greater than about 50 Å deep. In the prior art, such corner recesses could be severely extended below the silicon surface.

A second hard mask 26, which in the preferred embodiment is about 1,000 to 2,000 Å thick is formed over the surface of the trench oxide 22 and pad oxide 12, as shown in figure 5. In the preferred embodiment of the invention, the second hard mask 26 is of the group consisting of silicon oxynitride (SiON), silicon nitride (Si_3N_4) and polysilicon. A photoresist mask is used to form apertures 28 in the second hard mask 26 over the core region and interface region of the substrate 10. The photoresist mask is then removed. The semiconductor substrate 10 is subjected to a clean step to remove greater than about 30 Å of oxide.

The semiconductor substrate 10 is then subjected to a low temperature oxidation at about 1050° C to form LOCOS oxides 30, as shown in figure 6. The second hard mask 26 is then removed, and the remaining oxide is subjected to a clean step with an HF step to remove any remaining stringers in the oxide, as shown in figure 7. The semiconductor substrate 10 has STI isolation and LOCOS isolation on a single substrate and is ready for the manufacture of periphery and core stacks between the LOCOS oxides 30 and the trench oxide 22.

To begin the manufacture of the periphery and core stacks, a 100 to 500 Å third hard mask layer 42 is placed on the pad oxide 12 over both the periphery region and core region, as shown in figure 8. In the preferred embodiment of the invention, the third hard mask layer 42 is of the group consisting of silicon oxynitride (SiON), silicon nitride (Si_3N_4), and polysilicon. A photoresist layer is placed over the top surface of the third hard mask layer 42 and then etched back to form a photoresist mask 44 that does not cover the core section of the semiconductor substrate 10, as shown in figure 8. The trench oxide 22, pad oxide 12, and LOCOS oxide 30 are not drawn to scale so that more features may be shown.

The semiconductor substrate 10 is subjected to an etching process, which removes the third hard mask layer 42 and the pad oxide 12 over the core region, as shown in figure 9. The photoresist mask is then removed. A tunnel oxide layer 46 is formed over the core region. The tunnel oxide layer 46 may also be formed over the third hard mask layer 42. Various methods are known for forming the tunnel oxide layer

46, such as growing an oxide layer or depositing an oxide layer. In the preferred embodiment, the tunnel oxide layer 16 is nitridated (a nitride dopant is added to the tunnel oxide layer). There are various methods known for nitridating a tunnel oxide layer such as providing nitrogen dioxide (NO_2) during the oxidation process or implanting nitrogen into a tunnel oxide layer or in situ growth of NO_x, where x = an integer. A first polysilicon layer 48 is formed over the tunnel oxide layer 46. A photoresist mask 49 is place over parts of the first polysilicon layer 48 over the core region.

The semiconductor substrate 10 is subjected to an etching process, which removes parts of the first polysilicon layer 48 and tunnel oxide layer 46, as shown in figure 10. The photoresist mask is removed. An interpoly dielectric layer 50 is formed over the substrate 10, third hard mask 42, and first polysilicon layer. In the preferred embodiment, the interpoly dielectric layer 50 is an oxide-nitride-oxide (ONO) layer. A photoresist mask 52 is formed over the interpoly dielectric layer 50 over the core region.

. The semiconductor substrate 10 is then subjected to a two step etch that first removes the portion of the interpoly dielectric layer 50 over the periphery region and then removes the third hard mask 42 and the remaining pad oxide, as shown in figure 11. The photoresist mask 52 is then removed. The semiconductor substrate 10 is then subjected to a first thermal oxidation which forms a first gate oxide layer 54 over the semiconductor substrate 10 in the periphery region. In the preferred embodiment the first gate oxide layer 54 is about 100 Å. A photoresist mask 56 is formed over portions of the first gate oxide layer 54 in the periphery region and over the interpoly dielectric layer 50.

The parts of the first gate oxide layer 54 not covered by the photoresist mask 56 are etched away, as shown in figure 12. The photoresist layer 56 is then stripped away, as shown in figure 13 with the remaining first oxide layer 54 becoming the thick oxide regions 58. The semiconductor substrate 10 is then subjected to a second thermal oxidation, which forms thin oxide layers 60 in the uncovered regions of the substrate 10 and thick oxide layers 62 at the thick oxide regions 58, as shown in figure 14. In the preferred embodiment, the thin oxide layers 60 are 40 to 80 Å thick and the thick oxide layers 62 are 100 to 150 Å thick. A second polysilicon layer 64 is placed on the substrate 10, the thin oxide layers 60, the thick oxide layers 62 and the interpoly layer 50 and then etched back to form periphery stacks with thin gates 66, periphery stacks with thick gates 68, and core stacks 70, as shown in figure 15.

Conventional processes are then used to complete the flash memory structure. The inventive method allows the production of periphery gates with thin gates and thick gates to provide gates with different threshold voltages. In addition, core stacks with nitridated tunnel oxide layers are provided, without contaminating the gate oxide layers and allows the use of STI and LOCOS isolation on a single chip.

Information as herein shown and described in detail is fully capable of attaining the above-described object of the invention, it is understood that it is the presently preferred embodiment of the present invention and is thus representative of the subject matter which is broadly contemplated by the present invention, that the scope of the present invention fully encompasses other embodiments which may

become obvious to those skilled in the art, and that the scope of the present invention is accordingly to be limited by nothing other than the appended claims, in which reference to an element in the singular is not intended to mean "one and only one" unless explicitly so stated, but rather "one or more." All structural and functional equivalents to the elements of the above-described preferred embodiment that are known to be known to those of ordinary skill in the art are expressly incorporated herein by reference and are intended to be encompassed by the present claims. Moreover, it is not necessary for a device or method to address each and every problem sought to be solved by the present invention, for it to be encompassed by the present claims. Furthermore, no element, component, or method step in the present disclosure is intended to be dedicated to the public regardless of whether the element, component, or method step is explicitly recited in the claims. No claim element herein is to be construed under the provisions of 35 U.S.C. 112, sixth paragraph, unless the element is expressly recited using the phrase "means for."

Claims

1. A semiconductor chip having a plurality of flash memory devices, comprising:

a silicon semiconductor substrate (10);

at least one periphery stack (66), comprising a thin gate oxide layer (60) and at least one polysilicon (poly-Si) layer (64), formed on a periphery region of said substrate;

at least one periphery stack (68), comprising a thick gate oxide layer (62) and at least one polysilicon (poly-Si) layer (64), formed on the periphery region of said substrate;

at least one core stack (70), comprising a nitridated tunnel oxide barrier layer (46), at least two polysilicon (poly-Si) layers (48,64), and an interpoly dielectric layer (50), formed on a core region of said substrate;

at least one shallow trench isolation (STI) (22) formed in the periphery region of said substrate; and

at least one local oxidation of silicon (LOCOS) (30) isolation formed in the core region of said substrate.

2. A semiconductor chip as claimed in claim 1, wherein said thin gate oxide layer comprises at least one material selected from a group consisting essentially of thermal silicon oxide (SiO) and thermal silicon dioxide (SiO_2), and wherein said thin gate oxide layer comprises a thickness in a range of 40 Å to 80 Å.

3. A semiconductor chip as claimed in claim 1 or claim 2, wherein said thick gate oxide layer comprises at least one material selected from a group consisting essentially of thermal silicon oxide (SiO) and thermal silicon dioxide (SiO_2), and wherein said thick gate oxide layer comprises a thickness in a range of 100Å to 150 Å.

4. A semiconductor chip as claimed in claim 1, 2 or 3, wherein said nitridated tunnel oxide barrier layer comprises at least one dopant selected from a group

consisting essentially of nitrogen (N_2) and nitric oxide (NO), and wherein said interpoly dielectric layer comprises an oxide-nitride-oxide (ONO) layer.

5. A semiconductor chip as claimed in any one of claims 1- 4, wherein said at least one shallow trench isolation (STI) comprises a trench oxide, and wherein said at least one shallow trench isolation (STI) comprises a depth in a range of approximately 0.15μm to approximately 0.35μm.

6. A semiconductor chip as claimed in any one of claims 1 – 5, wherein said at least one local oxidation of silicon (LOCOS) isolation comprises a LOCOS oxide, and wherein said at least one local oxidation of silicon (LOCOS) isolation is formed at a temperature of approximately 1050°C.

7. A semiconductor chip as claimed in any one of claims 1-6, wherein each said at least one shallow trench isolation (STI) insulates each said at least one periphery stack from one another.

8. A semiconductor chip as claimed in any one of claims 1-7, wherein each said at least one local oxidation of silicon (LOCOS) isolation insulates each said at least one core stack from one another.