SEMICONDUCTOR STRUCTURE AND MANUFACTURING METHOD THEREOF

CROSS-REFERENCE TO RELATED APPLICATION

[0001] The present application claims benefit of Chinese Patent Application No. 202010816754.X, filed on August 14, 2020 and entitled "SEMICONDUCTOR STRUCTURE AND MANUFACTURING METHOD THEREOF", the contents of which are hereby incorporated by reference in its entirety.

TECHNICAL FIELD

[0002] The disclosure relates to the field of semiconductor manufacture, and more particularly, to a semiconductor structure and a manufacturing method thereof.

BACKGROUND

[0003] Dynamic random access memory (DRAM) is a common semiconductor storage device in computers, and has a storage array region composed of a number of repeated storage units. Each storage unit typically includes a capacitor and a transistor. In a transistor, a gate connects to a bit line structure, either a drain or a source connects to the bit line structure, and another of the drain and the source connects to the capacitor. A voltage signal on the bit line structure can control on or off of the transistor, and then through the bit line structure, data information stored in the capacitor can be read, or through the bit line structure, the data information can be written into the capacitor for storage.

[0004] Upon miniaturization of the manufacture procedure, the contact resistance at each wire connection position in the DRAM becomes increasingly important. Among them, the contact resistance at a conductive connection position of a capacitor with a

transistor in the array region of the DRAM, and the contact resistance at a wire connection position of a source-drain region of a Metal Oxide Semiconductor (MOS) tube in the peripheral circuit region are particularly important. At present, during manufacture of a wire structure, a transition layer is deposited first prior to deposition of a metal wire, so as to reduce the contact resistance, and increase the connection performance between layers.

[0005] The transition layer in the array region and in the peripheral circuit region has the same thickness because it is formed in the same step. For the array region, the thicker the transition layer, the larger the conducting current, and the better the wire performance; whereas for the peripheral circuit region, the excessively thick transition layer will result in an overhigh conducting current thereby possibly causing the breakdown effect and increased current leakage.

[0006] Therefore, how to form a transition layer having different thicknesses respectively in the array region and in the peripheral circuit region becomes a problem to be solved urgently at present.

SUMMARY

[0007] The technical problem to be solved by the disclosure is to provide a semiconductor structure and a manufacturing method thereof, which can form a transition layer having different thicknesses respectively in the array region and in the peripheral circuit region, to improve the conductivity of the wire in the array region and to avoid the current leakage in the peripheral circuit region due to the excessive thickness of the transition layer.

[0008] In order to solve the above-mentioned problem, the disclosure provides a method for manufacturing a semiconductor structure, which may include the following steps, in which a semiconductor substrate is provided, which includes an array region and a peripheral circuit region, in which in the array region, multiple capacitor contact holes are provided on the semiconductor substrate, and a first conductive layer is deposited on a bottom of each of the capacitor contact holes, and in the peripheral circuit region, a

device layer is provided on the semiconductor substrate; the first conductive layer is treated with performing an ion implantation step to increase its roughness; wire contact holes are formed in the peripheral circuit region, in which the semiconductor substrate is exposed by the wire contact holes; a transition layer is formed, which at least covers a surface of the first conductive layer and a surface of the semiconductor substrate exposed by the wire contact holes; and a second conductive layer is formed, which covers the transition layer, and fills the capacitor contact holes and the wire contact holes.

[0009] Further, multiple discrete bit line structures are formed on the semiconductor substrate, and the capacitor contact holes are respectively provided between the bit line structures, and before the step of treating the first conductive layer, the bit line structures of the array region and the device layer of the peripheral circuit region are thinned.

[0010] Further, each of the bit line structures may include a bit line contact island and a bit line, in which the bit line contact island contacts the semiconductor substrate, the bit line is arranged on the bit line contact island, and the bit line includes a conductive layer and a dielectric layer which is disposed on the conductive layer, and in the thinning step, the dielectric layer is thinned.

[0011] Further, the step of treating the first conductive layer further includes that: ion implantation is performed to the first conductive layer to damage surface evenness of the first conductive layer and increase the roughness of the first conductive layer.

[0012] Further, the conductive layer is a polysilicon layer, and the step of performing the ion implantation to the first conductive layer includes performing germanium ion, carbon ion or arsenic ion implantation to the first conductive layer.

[0013] Further, in the step of performing the ion implantation to the first conductive layer, a deposition layer is also formed on a surface of the device layer of the peripheral circuit region.

[0014] Further, the method further includes the following steps: an isolation layer, which covers surfaces of the array region and the peripheral circuit region, is formed after the step of treating the first conductive layer; and the isolation layer is removed after the step that the wire contact holes are formed in the peripheral circuit region.

[0015] Further, the step of forming the transition layer further includes that: a cobalt layer is deposited at the bottom of each of the capacitor contact holes and a bottom of each of the wire contact holes, cobalt reacts with the first conductive layer and the semiconductor substrate to form the transition layer; and a rapid thermal process (RTP) is performed.

[0016] Further, a thickness of the transition layer located in the array region is greater than that of the transition layer located in the peripheral circuit region.

[0017] Further, the second conductive layer may include an adhesion layer and a metal conductive layer, and the step of forming the second conductive layer further includes that the adhesion layer is formed on a surface of the transition layer.

[0018] The metal conductive layer is formed on a surface of the adhesion layer, and the metal conductive layer fills the capacitor contact holes and the wire contact holes.

~~[0019] The disclosure further provides a semiconductor structure, which may include: a semiconductor substrate including an array region and a peripheral circuit region, in which in the array region, multiple capacitor contact holes are provided on the semiconductor substrate, which expose the semiconductor substrate, and in the peripheral circuit region, multiple wire contact holes are provided on the semiconductor substrate, which expose the semiconductor substrate; multiple capacitor conductive structures are respectively arranged in the capacitor contact holes, each of the capacitor conductive structures includes a first conductive layer filling a part of the capacitor contact holes, a transition layer at least covering the first conductive layer and a second conductive layer covering the transition layer and filling the capacitor contact holes, in which the first conductive layer contacts the semiconductor substrate; and multiple wire structures are respectively arranged in the conductive contact holes, each of the wire structures includes a transition layer covering a surface of the semiconductor substrate, and a second conductive layer covers the transition layer and fills the wire contact holes, in which the transition layer contacts the semiconductor substrate, wherein thickness of the transition layer of the capacitor conductive structure is greater than that of the transition layer of the wire structure.~~

~~[0020] Further, in the peripheral circuit region, a structure layer is provided on the semiconductor substrate, and the wire contact holes penetrate through the structure layer.~~

~~[0021] Further, each of the capacitor conductive structures further includes an ion implantation layer, the ion implantation layer is located in the first conductive layer, and in the peripheral circuit region, the structure layer further includes a device layer and a deposition layer located on the device layer, and the deposition layer and the ion implantation layer are the layers of a same material.~~

~~[0022] Further, in the array region, multiple discrete bit line structures are arranged on the semiconductor substrate, and the capacitor contact holes are respectively arranged between the bit line structures.~~

~~[0023] Further, each of the bit line structures includes a bit line contact island and a bit line, the bit line contact island contacts the semiconductor substrate, the bit line is arranged on the bit line contact island, and the bit line includes a conductive layer and a dielectric layer which is disposed on the conductive layer.~~

~~[0024] Further, the second conductive layer may include an adhesion layer and a metal conductive layer, in which the adhesion layer at least covers a surface of the transition layer, and the metal conductive layer covers the adhesion layer, and fills the capacitor contact holes and the wire contact holes.~~

~~[0025]~~[0019] The disclosure has the following advantages: in the array region, roughening is performed on the surface of the first conductive layer, such that the transition layer formed in the same step has different thicknesses in the array region and in the peripheral circuit region, thereby meeting different requirements of the array region and the peripheral circuit region on the thicknesses of the transition layer, which improves the conductivity of the wire in the array region, avoids the current leakage of the peripheral circuit region due to the excessive thickness of the transition layer, thus greatly improves the performance of the semiconductor structure. Moreover, the method has simple processes, and does not involve any additional troublesome processes.

BRIEF DESCRIPTION OF THE DRAWINGS

[~~0026~~][0020] FIG. 1 illustrates a schematic diagram of steps of a method for manufacturing a semiconductor structure in an example of the disclosure.

[~~0027~~][0021] FIG. 2 to FIG. 9 illustrate the process flow diagrams of a method for manufacturing a semiconductor structure in an example of the disclosure.

DETAILED DESCRIPTION

[~~0028~~][0022] The specific examples of the semiconductor structure and the method for manufacturing the same provided by the disclosure will be described below in detail in combination with the accompanying drawings.

[~~0029~~][0023] FIG. 1 illustrates a schematic diagram of steps of a method for manufacturing a semiconductor structure in an example of the disclosure. Referring to FIG. 1, the method for manufacturing the semiconductor structure may include the following steps. At S10, a semiconductor substrate is provided. The semiconductor substrate includes an array region and a peripheral circuit region. In the array region, multiple capacitor contact holes are provided on the semiconductor substrate, and a first conductive layer is deposited at a bottom of the capacitor contact holes. In the peripheral circuit region, a device layer is provided on the semiconductor substrate. At S11, the first conductive layer is treated to increase its roughness. At S12, the wire contact holes are formed in the peripheral circuit region. The wire contact holes expose the semiconductor substrate. At S13, a transition layer is formed, which at least covers a surface of the first conductive layer and a surface of the semiconductor substrate. The surface of the semiconductor substrate exposed by the wire contact holes. At S14, a second conductive layer is formed, which covers the transition layer, and fills the capacitor contact holes and the wire contact holes.

[~~0030~~][0024] FIG. 2 to FIG. 9 illustrate the process flow diagrams of the a method for manufacturing a semiconductor structure in an example of the disclosure.

[0031][0025] Referring to S10 and FIG. 2, a semiconductor substrate 200 is provided. The semiconductor substrate 200 includes an array region A and a peripheral circuit region B. In the array region A, multiple capacitor contact holes 210 are provided on the semiconductor substrate 200, and a first conductive layer 220 is deposited at a bottom of each of the capacitor contact holes 210. In the peripheral circuit region B, a device layer 230 is provided on the semiconductor substrate 200.

[0032][0026] The semiconductor substrate 200 includes but is not limited to a silicon substrate or a germanium substrate.

[0033][0027] In the array region A, a shallow trench isolation structure 201 and an active region 202 separated by the shallow trench isolation structure 201 are arranged on the semiconductor substrate 200. The capacitor contact holes 210 expose part of the active region 202. The first conductive layer 220 is deposited at the bottom of each of the capacitor contact holes 210, and electrically connects to the active region 202. In the example, the first conductive layer 220 is a polysilicon layer.

[0034][0028] Further, multiple discrete bit line structures 203 are formed on the semiconductor substrate 200, spaces are respectively provided between adjacent bit line structures 203. The capacitor contact holes 210 are respectively provided in the spaced regions between the adjacent bit line structures 203. The bit line structure 203 extends along a set direction. For example, in this example, the bit line structure 203 extends along a direction perpendicular to the paper.

[0035][0029] Each bit line structure 203 includes a bit line contact island 203A and a bit line arranged on the bit line contact island 203A. The bit line contact islands 203A are arranged in an interval distribution on the semiconductor substrate 200. For example, in this example, the bit line contact islands 203A are sequentially arranged in the extension direction of the bit lines 203. Each of the bit line contact islands 203A contacts the active region 202 in the semiconductor substrate 200, thereby electrically connecting the bit line to the active region 202. Specifically, in the sectional schematic diagram shown in FIG. 2, in a region presented with the bit line contact island 203A, the bit line is electrically connected to the active region 202 through the bit line contact island 203A. In a region without the bit line contact island 203A, an insulation layer is provided between the bit

line and the active region, i.e., the bit line is not electrically connected with the active region 202. The bit line contact island 203A may be formed by a material such as polysilicon etc. Each of the bit lines may be constructed by multiple conductive layers 2031. In an example, for example, each of the bit lines may be constructed by conductive layers of a polysilicon layer, a TiN layer, a metal tungsten layer and the like. A dielectric layer 2032 is provided on the conductive layer 2031, so as to protect the conductive layer. The dielectric layer 2032 may include but is not limited to a silicon nitride layer.

[~~0036~~][0030] Further, each of the bit line structures 203 further include a protective layer 2033 disposed on the sidewall of the conductive layer 2031 and the sidewall of the dielectric layer 2032. The protective layer 2033 may be a silicon nitride layer.

[~~0037~~][0031] In the peripheral circuit region B, the semiconductor substrate 200 includes a shallow trench isolation structures 201, an active region 202 separated by the shallow trench isolation structure 201, and a device layer 230 provided on the semiconductor substrate 200. The device layer 230 includes a conductive structure layer 231 and an insulation layer 232 that are arranged on the surface of the semiconductor substrate. A conductive structure is provided in the conductive structure layer 231, which corresponds to the active region 202. The conductive structure may serve as a gate of the transistor. The insulation layer 232 covers the conductive structure layer 231 to protect the conductive structure layer 231.

[~~0038~~][0032] Further, for ease of performance of the subsequent process, for example, for ease of the filling of the subsequent second conductive layer (shown in FIG. 9), a thinning step is further included after S10. Specifically, referring to FIG. 3, the bit line structures 203 in the array region A and the device layer 230 in the peripheral circuit region B are thinned. In this step, in the array region A, the dielectric layer 2032 and the protective layer 2033 on the sidewall thereof are thinned, and the conductive layer 2031 of the bit line is not exposed; meanwhile in the peripheral circuit region B, the insulation layer 232 of the device layer 230 is thinned, and the conductive structure in the conductive structure layer 231 of the device layer 230 is not exposed. Further, the dielectric layer 2032, the protective layer 2033 and the insulation layer 232 may be thinned by etching and the like.

[~~0039~~][0033] Referring to S11 and FIG. 4, the first conductive layer 220 is treated, to increase its roughness. In this step, with the increasing of the surface roughness of the first conductive layer 220, the surface area of its surface is increased, such that the contact area between the transition layer and the first conductive layer 220 is increased and thus the thickness of the transition layer is increased in the subsequent process of forming the transition layer 250 (shown in FIG. 8).

[~~0040~~][0034] In the example, ion implantation is performed to the first conductive layer 220 to damage the surface evenness of the first conductive layer 220 thereby increasing the roughness of the first conductive layer 220. The affected region 220A on the surface of the first conductive layer 220 is shown by the shadow in FIG. 4. When the ion implantation is performed to the first conductive layer 220, ions bombard the surface of the first conductive layer 220, break the chemical bonds of the first conductive layer 220, and damage the surface evenness of it, such that the surface roughness of the first conductive layer 220 is increased. For example, when the material of the first conductive layer 220 is polysilicon, Si-Si chemical bonds in the polysilicon are broken by the ion implantation, and the surface evenness of the polysilicon is damaged, such that the surface roughness of the polysilicon is increased, and thus the subsequent reaction area between the transition layer and the polysilicon is increased, and as a result the thickness of the transition layer is increased.

[~~0041~~][0035] The ion having a large atomic radius, such as the germanium ion, carbon ion or arsenic ion, may be used for the ion implantation, to further break the chemical bonds of the first conductive layer 220, and to further increase the roughness of the first conductive layer 220.

[~~0042~~][0036] As shown in FIG. 4, after the step of ion implantation, in the array region A, an ion implantation layer 400 is formed in the first conductive layer 220. In the peripheral circuit region B, due to the obstruction effect of the device layer 230, specifically, due to the obstruction effect of the insulation layer 232, the ions are not implanted into the device layer 230 but are deposited on the surface of the device layer 230, thereby forming the deposition layer 410. The depth of the ion implantation may be determined according to an actual condition; as long as the position of the ion implantation layer 400

formed after the ion implantation does not affect the formation of the subsequent transition layer 250.

[~~0043~~][0037] Further, in order to avoid oxidation of the first conductive layer in the subsequent process, a step of forming an isolation layer is further included after S11. Specifically, referring to FIG. 5, the isolation layer 500 is formed. The isolation layer 500 covers the surface of the array region A and the surface of the peripheral circuit region B. In the example, the isolation layer 500 is a silicon nitride layer. In the array region A, it covers the surface of each bit line structure 203 and the surface of the first conductive layer 220. In the peripheral circuit region B, the isolation layer 500 covers the surface of the deposition layer 410.

[~~0044~~][0038] Referring to S12 and FIG. 6, in the peripheral circuit region B, wire contact holes 240 are formed which expose the semiconductor substrate 200. Specifically, in the example, the wire contact holes 240 are formed by photoetching and etching processes. Each of the wire contact holes 240 penetrates through the deposition layer 410 and the device layer 230, and exposes the active region 202 of the semiconductor substrate 200. Each wire contact hole 240 is arranged at either sides of the conductive structure of the conductive structure layer 231.

[~~0045~~][0039] It is understood that during the formation of the wire contact holes 240, the array region A is shielded by a mask, so as not to be etched.

[~~0046~~][0040] Further, referring to FIG. 7, after the wire contact holes are formed at S12, the following step may be further included: the isolation layer 500 is removed, to expose the first conductive layer 220. In this step, the isolation layer 500 may be removed by etching.

[~~0047~~][0041] Referring to S13 and FIG. 8, a transition layer 250 is formed, the transition layer 250 at least coves a surface of the first conductive layer 220 and a surface of the semiconductor substrate 200 exposed by the wire contact holes 240.

[~~0048~~][0042] In the example, the method for forming the transition layer 250 is that cobalt is deposited in the array region A and the peripheral circuit region B. At the bottom of each capacitor contact hole 210 and the bottom of each wire contact hole 240, the cobalt reacts

with the semiconductor substrate 200 and the first conductive layer 220 to form the transition layer 250. In other regions, for example, on the sidewall of the capacitor contact hole 210 and on the sidewall of the wire contact hole 240, the cobalt is deposited to form a cobalt layer. After the cobalt is deposited, the cobalt layer on the sidewall of the capacitor contact hole 210 and the sidewall of the wire contact hole 240 is removed by a method of acid cleaning and the like, and the transition layer 250 is retained. Specifically, when the semiconductor substrate is the silicon substrate, and the first conductive layer 220 is the polysilicon layer, the cobalt reacts with the silicon at the bottoms of the capacitor contact holes 210 and the wire contact holes 240 to form a cobalt silicate (CoSix) layer. The cobalt silicate layer is the transition layer. In other regions, the cobalt is deposited to form the cobalt layer. After the cobalt is deposited, the cobalt layer is removed by cleaning. In FIG 8 in order to clearly show the structure of the transition layer 250, the size of the transition layer 250 is appropriately exaggerated.

~~[0049]~~[0043] Further, after the transition layer 250 is formed, the RTP is performed under the environment of an inert gas. For example, the temperature of the manufacturing process is between 700°C and 850°C. Therefore, the unreacted cobalt and the incompletely reacted CoSi-phase silicate in the capacitor contact holes 210 and the wire contact holes 240 are completely reacted to form the integral cobalt silicate layer, thereby further reducing the resistance.

~~[0050]~~[0044] At S13, the first conductive layer 220 is roughened, whereas the semiconductor substrate 200 exposed by the wire contact holes 240 is not roughened and has a flat surface, and thus the roughness of the surface of the first conductive layer 220 is greater than that of the semiconductor substrate 200 exposed by the wire contact holes 240. As a result,when the cobalt is deposited, the contact area between the cobalt and the first conductive layer 220 is greater than that between the cobalt and the semiconductor substrate 200 exposed by the wire contact holes 240, and the thickness of the transition layer 250 formed in the capacitor contact holes 210 is far greater than that of the transition layer 250 formed in the wire contact holes 240. For the array region A, the thicker the transition layer 250, the larger the conducting current, and the better the wire performance. For the peripheral circuit region B, the transition layer 250 is not too thick and does not lead to the overhigh conducting current, to avoid the breakdown effect and

the increase of a current leakage.

[~~0051~~][0045] Referring to S14 and FIG. 9, a second conductive layer 260 is formed. The second conductive layer 260 covers the transition layer 250, and fills the capacitor contact holes 210 and the wire contact holes 240.

[~~0052~~][0046] In the example, the second conductive layer 260 includes an adhesion layer 261 and a metal conductive layer 262. The step of forming the second conductive layer 260 further includes the following steps. The adhesion layer 261 is formed on the surface of the transition layer 250, the sidewall of the capacitor contact hole 210 and the sidewall of the wire contact hole 240. The adhesion layer 261 including but not limited to a TiN layer. The metal conductive layer 262 is formed on the surface of the adhesion layer 261. The metal conductive layer 262 fills the capacitor contact holes 210 and the wire contact holes 240. The metal conductive layer 262 may be a metal tungsten layer.

[~~0053~~][0047] In the array region A, the first conductive layer 220, the transition layer 250 and the second conductive layer 260 are formed into a capacitor conductive structure. The transition layer 250 can reduce the contact resistance between the first conductive layer 220 and the second conductive layer 260.

[~~0054~~][0048] In the peripheral circuit region B, the transition layer 250 and the second conductive layer 260 are formed to the wire structure. The transition layer 250 is connected to the semiconductor substrate 200 and the second conductive layer 260 respectively, and can reduce the contact resistance between the semiconductor substrate 200 and the second conductive layer 260 and increase the connection performance between the layers. In the peripheral circuit region, the wire structure contacts a source-drain region of the transistor of the semiconductor substrate 200, and is configured to lead out the source-drain region. The conductive structure in the conductive structure layer 231 of the device layer 230 serves as the gate of the transistor, and is configured to control the conduction of the transistor. The transistor mainly serves as a control circuit.

[~~0055~~][0049] The method for manufacturing the semiconductor structure provided by the disclosure can form the transition layer thicker in the array region A and thinner in the peripheral circuit region B in the same step, which meets the requirements of the array

region A and the peripheral circuit region B as well on the thickness of the transition layer, and greatly improves the performance of the semiconductor structure.

[~~0056~~][0050] The disclosure further provides a semiconductor structure manufactured with the aforementioned preparation method. Referring to FIG. 9, the semiconductor structure includes a semiconductor substrate 200, multiple capacitor conductive structures and multiple wire structures.

[~~0057~~][0051] The semiconductor substrate 200 includes an array region A and a peripheral circuit region B. In the array region A, multiple capacitor contact holes 210 are provided on the semiconductor substrate 200, which expose the semiconductor substrate 200. In the peripheral circuit region B, multiple wire contact holes 240 are provided on the semiconductor substrate 200, which expose the semiconductor substrate 200. Multiple capacitor conductive structures are respectively arranged in the capacitor contact holes 210. Each of the capacitor conductive structures includes a first conductive layer 220 filling a part of each of the capacitor contact holes 210, a transition layer 250 at least covering the first conductive layer 220 and a second conductive layer 260 covering the transition layer 250 and filling the capacitor contact holes 220. The first conductive layer 220 contacts the semiconductor substrate 200, and the transition layer 250 is formed on the first conductive layer 220. The transition layer 250 can reduce the contact resistance between the first conductive layer 220 and the second conductive layer 260, and improve the performance of the capacitor conductive structure.

[~~0058~~][0052] Further, in the array region A, multiple discrete bit line structures 203 are arranged on the semiconductor substrate 200. Each of the capacitor contact holes 210 is provided between the bit line structures 203. Each of he capacitor conductive structure is also located between the bit line structures 203. Each of the bit line structure 203 includes a bit line contact island 203A and a bit line. The bit line contact island 203A contacts the semiconductor substrate 200, and the bit line is arranged on the bit line contact island 203A. Further, the bit line includes a conductive layer 2031 and a dielectric layer 2032 disposed on the conductive layer 2031.

[~~0059~~][0053] Further, the capacitor conductive structure further includes an ion implantation layer 400, and the ion implantation layer 400 is located in the first conductive layer 220.

[0060][0054] The multiple wire structures are respectively arranged in the conductive contact holes 240. Each of the wire structure includes a transition layer 250 covering a surface of the semiconductor substrate 200, and a second conductive layer 260 covering the transition layer 250 and filling the wire contact hole 240. The transition layer 250 contacts the semiconductor substrate 200. Further, in the peripheral circuit region B, a structure layer is provided on the semiconductor substrate 200. The wire contact hole 240 penetrates through the structure layer. The structure layer includes a device layer 230 and a deposition layer 410 located on the device layer 230. The deposition layer 410 and the ion implantation layer 400 are layers of a same material. For example, both are a germanium material layer, a carbon material layer or an arsenic material layer.

[0061][0055] Further, the second conductive layer 260 includes an adhesion layer 261 and a metal conductive layer 262. The adhesion layer 261 at least covers a surface of the transition layer 250, and the metal conductive layer 262 covers the adhesion layer 261, and fills the capacitor contact holes 210 and the wire contact holes 240.

[0062][0056] The thickness of the transition layer 250 of the capacitor conductive structure is more than that of the transition layer 250 of the wire structure, which meets requirements of the array region A and the peripheral circuit region B on the thickness of the transition layer, and greatly improves the performance of the semiconductor structure.

[0063][0057] The above are only preferred examples of the disclosure. It should be pointed out that those of ordinary skill in the art may further make multiple improvements and modifications without departing from the principle of the disclosure, and these improvements and modifications are also should be considered within the scope of protection of the disclosure.

CLAIMS

1. A method for manufacturing a semiconductor structure, comprising the following steps:

providing a semiconductor substrate which comprises an array region and a peripheral circuit region, wherein in the array region, multiple capacitor contact holes are provided on the semiconductor substrate, and a first conductive layer is deposited on a bottom of each of the capacitor contact holes, and in the peripheral circuit region, a device layer is on the semiconductor substrate;

treating the first conductive layer with performing an ion implantation step to increase roughness of the first conductive layer;

forming wire contact holes exposing the semiconductor substrate in the peripheral circuit region;

forming a transition layer covering a surface of the first conductive layer and a surface of the semiconductor substrate exposed by the wire contact holes, wherein a thickness of the transition layer located in the array region is greater than that of the transition layer located in the peripheral circuit region; and

forming a second conductive layer covering the transition layer, and filling the capacitor contact holes and the wire contact holes.;

2. The method for manufacturing the semiconductor structure of claim 1, wherein forming multiple discrete bit line structures on the semiconductor substrate, providing the capacitor contact holes respectively between the bit line structures, and before the step of treating the first conductive layer, thinning the bit line structure of the array region and the device layer of the peripheral circuit region.

32. The method for manufacturing the semiconductor structure of claim 21, wherein each of

the bit line structures comprises a bit line contact island and a bit line, wherein the bit line contact island contacts the semiconductor substrate, the bit line is arranged on the bit line contact island, and the bit line comprises a conductive layer and a dielectric layer disposed on the conductive layer, wherein the dielectric layer is thinned in the thinning step.

43. The method for manufacturing the semiconductor structure of claim 1, wherein the step of treating the first conductive layer further comprises performing ion implantation to the first conductive layer, to damage a surface evenness of the first conductive layer, thereby increasing the roughness of the first conductive layer.

54. The method for manufacturing the semiconductor structure of claim 43, wherein the conductive layer is a polysilicon layer, and the step of performing the ion implantation to the first conductive layer is of performing germanium ion, carbon ion or arsenic ion implantation to the first conductive layer.

65. The method for manufacturing the semiconductor structure of claim 43, wherein in the step of performing the ion implantation to the first conductive layer, a deposition layer is also formed on a surface of the device layer of the peripheral circuit region.

76. The method for manufacturing the semiconductor structure of claim 1, further comprising the following steps: forming an isolation layer, which covers a surface of the array region and a surface of the peripheral circuit region after the step of treating the first conductive layer; and removing the isolation layer after the step of forming the wire contact holes in the peripheral circuit region.

87. The method for manufacturing the semiconductor structure of claim 1, wherein the step of

forming the transition layer further comprises the steps of:

depositing a cobalt layer, wherein at the bottom of each of the capacitor contact hole and a bottom of each of the wire contact hole, cobalt reacts with the first conductive layer and the semiconductor substrate to form the transition layer; and

performing a rapid thermal process.

~~9. The method for manufacturing the semiconductor structure of claim 1, wherein a thickness of the transition layer located in the array region is greater than that of the transition layer located in the peripheral circuit region.~~

~~10~~8. The method for manufacturing the semiconductor structure of claim 1, wherein the second conductive layer comprises an adhesion layer and a metal conductive layer, and the step of forming the second conductive layer further comprises the following steps:

forming the adhesion layer on a surface of the transition layer; and

forming the metal conductive layer on a surface of the adhesion layer, wherein the metal conductive layer fills the capacitor contact holes and the wire contact holes.

~~11. A semiconductor structure, comprising:~~

~~a semiconductor substrate, comprising an array region and a peripheral circuit region, wherein in the array region, multiple capacitor contact holes are provided on the semiconductor substrate, which expose the semiconductor substrate, and in the peripheral circuit region, multiple wire contact holes is provided on the semiconductor substrate, which expose the semiconductor substrate;~~

~~multiple capacitor conductive structures, respectively arranged in the capacitor contact holes, wherein each of the capacitor conductive structures comprises a first conductive layer~~

~~filling a part of each of the capacitor contact holes, a transition layer at least covering the first conductive layer and a second conductive layer covering the transition layer and filling the capacitor contact hole, in which the first conductive layer contacts the semiconductor substrate; and~~

~~multiple wire structures, respectively arranged in the conductive contact holes, each of the wire structure comprises the transition layer covering a surface of the semiconductor substrate, and the second conductive layer covering the transition layer and filling the wire contact holes, in which the transition layer contacts the semiconductor substrate,~~

~~wherein a thickness of the transition layer of the capacitor conductive structures is greater than that of the transition layer of the wire structures.~~

~~12. The semiconductor structure of claim 11, wherein in the peripheral circuit region, a structure layer is on the semiconductor substrate, and the wire contact holes penetrate through the structure layer.~~

~~13. The semiconductor structure of claim 12, wherein each of the capacitor conductive structures further comprises an ion implantation layer, in which the ion implantation layer is located in the first conductive layer, and in the peripheral circuit region, the structure layer further comprises a device layer and a deposition layer located on the device layer, wherein the deposition layer and the ion implantation layer are layers of a same material.~~

~~14. The semiconductor structure of claim 11, wherein in the array region, multiple discrete bit line structures are arranged on the semiconductor substrate, wherein the capacitor contact holes are respectively arranged between the bit line structures.~~

~~15. The semiconductor structure of claim 14, wherein each of the bit line structures comprises~~

~~a bit line contact island and a bit line, wherein the bit line contact island contacts the semiconductor substrate, the bit line is arranged on the bit line contact island, and the bit line comprises a conductive layer and a dielectric layer disposed on the conductive layer.~~

~~16. The semiconductor structure of claim 11, wherein the second conductive layer comprises an adhesion layer and a metal conductive layer, wherein the adhesion layer at least covers a surface of the transition layer, and the metal conductive layer covers the adhesion layer, and fills the capacitor contact holes and the wire contact holes.~~