CLAIMS

What is claimed is:

1. An apparatus for implementing signed numerical values, the apparatus comprising:

an optical detector comprising a first terminal and a second terminal;

a first switch coupling the first terminal of the optical detector to either a node or a reference voltage;

a second switch coupling the second terminal of the optical detector to either the node or to a voltage rail; and

control circuitry configured to:

produce a positively-signed numerical value output at least in part by setting the first switch to couple the first terminal to the reference voltage and setting the second switch to couple the second terminal to the node; and

produce a negatively-signed numerical value output at least in part by setting the first switch to couple the first terminal to the node and setting the second switch to couple the second terminal to the voltage rail.

2. The apparatus of claim 1, wherein the optical detector comprises a photodiode;

the first terminal comprises an anode; and

the second terminal comprises a cathode.

3. The apparatus of claim 1, wherein the first switch and the second switch each comprise a transistor switch.

4. The apparatus of claim 1, wherein the reference voltage is ground.

5. The apparatus of claim 1, wherein the control circuitry comprises logical gate configured to output a sign orientation bit, wherein the sign orientation bit comprises information indicative of whether the numerical value output comprises a positively-signed or negatively-signed numerical value.

6. The apparatus of claim 5, wherein the logical gate comprises an XOR gate.

7. The apparatus of claim 5, wherein the logical gate is configured to compare a sign of a value of an input vector element and a sign of a value of an input matrix element.

8. An optical processing system, comprising:

a first plurality of optical modulators, each configured to receive an input optical signal, modulate the input optical signal, and output a first optical signal representing an element of a vector;

a second plurality of optical modulators, each optically coupled to an optical modulator of the first plurality of optical modulators and configured to receive the first optical signal, modulate the first optical signal, and output a second optical signal representing a portion of a matrix-vector multiplication between the vector and a matrix;

a plurality of optical detectors each optically coupled to optical modulators of the second plurality of optical modulators and configured to convert the second optical signal into an electrical signal representing the portion of the matrix-vector multiplication, wherein each optical detector of the plurality of optical detectors comprises a first terminal and a second terminal;

a first switch coupling the first terminal of a first optical detector to either an output node or a reference voltage;

a second switch coupling the second terminal of the first optical detector to either the output node or to a voltage rail; and

control circuitry configured to:

produce a positively-signed numerical value output at least in part by setting the first switch to couple the first terminal of the first optical detector to the reference voltage and setting the second switch to couple the second terminal of the first optical detector to the output node; and

produce a negatively-signed numerical value output at least in part by setting the first switch of the first optical detector to couple the first terminal to the output node and setting the second switch of the first optical detector to couple the second terminal to the voltage rail.

9. The optical processing system of claim 8, wherein the optical detector comprises a photodiode;

the first terminal comprises an anode; and

the second terminal comprises a cathode.

10. The optical processing system of claim 9, wherein the first switch and the second switch each comprise a transistor switch.

11. The optical processing system of claim 9, wherein the reference voltage is grounded.

12. The optical processing system of claim 9, further comprising a plurality of electrical summing circuits, wherein:

a first electrical summing circuit of the plurality is coupled to two or more output nodes, each output node of the two or more output nodes being coupled to an optical detector through the first switch or the second switch; and

the first electrical summing circuit is configured to output an electrical signal representing a sum of the portions of the matrix-vector operation output by the optical detectors coupled to the two or more output nodes.

13. The optical processing system of claim 8, wherein the control circuitry comprises logical gate configured to output a sign orientation bit, wherein the sign orientation bit comprises information indicative of whether the numerical value output comprises a positively-signed or negatively-signed numerical value.

14. The optical processing system of claim 13, wherein the logical gate comprises an XOR gate.

15. The optical processing system of claim 13, wherein the logical gate is configured to compare a sign of a value of an input vector element and a sign of a value of an input matrix element.

16. A method for implementing signed numerical values output by optical detectors of an optical processor, the method comprising:

converting, using an optical detector comprising a first terminal and a second terminal, an output optical signal into a first electrical signal, the output optical signal being output by a portion of the optical processor;

determining, using an at least one conventional processor coupled to the optical processor, whether the first electrical signal represents a positively-signed numerical value or a negatively-signed numerical value;

arranging, using control circuitry of the optical processor, settings of a first switch coupled to the first terminal and settings of a second switch coupled to the second terminal in response to determining whether the first electrical signal represents the positively-signed

numerical value or the negatively-signed numerical value, wherein the control circuitry is configured to:

produce a positively-signed numerical value output at least in part by setting the first switch to couple the first terminal to a reference voltage and setting the second switch to couple the second terminal to a node; and

produce a negatively-signed numerical value output at least in part by setting the first switch to couple the first terminal to the node and setting the second switch to couple the second terminal to a voltage rail; and

outputting, from the optical detector, the first electrical signal so that the first electrical signal passes through either the first switch or the second switch based on the determination of whether the first electrical signal represents a positively-signed numerical value or a negatively-signed numerical value.

17. The method of claim 16, wherein arranging settings of the first switch and the second switch comprises sending, from the control circuitry, one or more electrical signals to the first switch and the second switch, wherein the first switch and the second switch each comprise a transistor switch.

18. The method of claim 16, further comprising:

modulating an input optical signal using a first optical modulator to optically represent an element of a vector in a first optical signal;

modulating the first optical signal using a second optical modulator to optically represent a summand in the output optical signal, wherein the summand, when summed with other summands, represents a product between the vector and a matrix row; and

detecting the output optical signal using the optical detector.

19. The method of claim 16, wherein arranging settings of a first switch and settings of a second switch further comprises using a logical gate to generate a sign orientation bit, wherein the sign orientation bit comprises information indicative of whether the first electrical signal comprises a positively-signed or negatively-signed numerical value.

20. The method of claim 19, wherein using the logical gate comprises using an XOR gate.