

A METHOD AND DEVICE FOR IMPROVED SALICIDE RESISTANCE ON POLYSILICON GATES

FIELD OF THE INVENTION

The present invention relates to the field of semiconductor devices. More particularly, the present invention relates to a method and device for improved resistance on gate electrodes. Specifically, the present invention relates to a method and device for improved salicide resistance on polysilicon gates.

BACKGROUND OF THE INVENTION

Transistors are commonly used in semiconductor circuitry to control current flow. For example, a transistor can be used as a switching mechanism to allow the flow of current between a source and a drain region in a circuit when a certain threshold voltage is met. Transistors generally include a gate electrode that allows or prevents the flow of current in the transistor based on applied voltage.

Figure 1a shows a cross-sectional view of a conventional gate electrode 100 formed on a substrate 110, the underlying structure of which is not shown. It should be noted that the figures are merely illustrative and have been simplified for clarity purposes. A thin insulative layer 120 is formed on the substrate 110 to act as a barrier between the substrate 110 and the conductive portions of the gate electrode 100. An example of an insulative layer 120 can be an oxide layer, such as silicon dioxide (SiO_2). Formed on the insulative layer 120 is a gate layer 130. An example of a gate layer 130 can be a polysilicon layer. Formed on the gate layer 130 is a conductive layer 160. An example of a conductive layer 160 can be a polycide layer, such as titanium salicide (TiSi_2). When a threshold voltage is applied to the gate layer 130 by the conductive layer 160, current will flow through the gate layer 130. Often insulative spacers 140 and 150

are formed to each side of the gate layer 130 to prevent transfer of current between the gate layer 130 and surrounding structures in the semiconductor.

In semiconductor circuit design, frequently, gate electrodes are designed in long continuous lines on the semiconductor substrate to efficiently provide current to several transistors in a circuit. Currently, improved semiconductor transistor performance is being achieved through device scaling in which the gate layer widths are being reduced from .20 μm to .15 μm and below (sub-.15 μm). As the gate layer width dimensions decrease, so do the conductive layer line widths formed above them.

When the gate layer widths decrease below .20 μm , current process techniques produce conductive lines with sharply increasing resistance. This is detrimental to the efficiency of the semiconductor, as higher resistance decreases the speed of the semiconductor circuitry. Additionally, process yields drop due to defective conductive line formation reducing manufacturing output. These problems have been particularly noted in current fabrication processes where titanium salicide (TiSi_2) is formed as the conductive layer in a polysilicon gate.

Figure 1b illustrates a cross-sectional view of a conventional gate electrode 100 formed on a substrate 110, the underlying structure of which is not shown. An example of a gate electrode 100 can be a polysilicon gate electrode. Formed on the substrate 110 is an insulative layer 120. An example of an insulative layer 120 can be an oxide. Formed on the insulative layer 120 is a conductive gate layer 130. An example of a gate layer 130 is a polysilicon layer. Formed on the gate layer 130 is a conductive layer 160. An example of a conductive layer 160 can be a polycide, such as titanium salicide. Insulative spacers 140 and 150 are formed adjacent to the gate layer 130 and conductive layer 160 to prevent current flow between the gate layer 100 and surrounding structures.

During formation of the conductive layer 160, components from underlying gate layer 130 often out diffuse into a reactant layer that is used to form the conductive layer

160. For example, silicon components of an underlying gate layer 130 may out diffuse into the conductive layer 160. This out diffusion results in a conductive layer 160 wider than the gate layer 130. When the gate layer 100 width is decreased below $.20\mu\text{m}$, the conductive layer 160 becomes stressed by its enclosure between the side walls of the spacers 140. This results in increased resistance in the conductive layer 160. Increased resistance in the conductive layer directly impacts the quality of the semiconductor circuit. The circuit becomes inefficient and circuit failure or device failure may occur.

Another result of decreasing the gate line widths below $.20\mu\text{m}$ is a decrease in process yields. This is due to non-formation of the conductive layer. This is attributed to the reduced reaction area, or nucleation sites, available at such small dimensions. The reduced dimensions of the gate layer reduces nucleation sites on which the conductive layer can form during processing. Using current process techniques, if sufficient nucleation sites are not provided, the conductive layer often won't form. This directly impacts the semiconductor manufacturer by reducing output.

Based on the above described problems, it would be desirable to have a method and/or device which will improve the polycide resistance in polysilicon gate widths below $.20\mu\text{m}$.

BRIEF SUMMARY OF THE INVENTION

The present invention provides a method and a device which improves polycide resistance in gate electrode widths below $.20\mu\text{m}$. The invention provides several embodiments one embodiment of which is described below.

In one embodiment of the present invention there is provided a gate electrode comprising a thin insulative layer. A gate layer is formed on the thin insulative layer. A conductive layer is formed on the gate layer. Thick first spacers are formed adjacent to opposite sides of the gate layer. Thick second spacers are formed adjacent to the thick

first spacers. The thick first spacers are recessed to create an open space between the gate layer and thick second spacers.

BRIEF DISCUSSION OF THE SEVERAL VIEWS OF THE DRAWINGS

For fuller understanding of the present invention, reference is made to the accompanying drawings in the following detailed description of the invention. In the drawings:

Figure 1(a) is a cross-sectional illustration of a conventional gate electrode in the prior art depicting a non-stressed conductive layer.

Figure 1(b) is a cross-sectional illustration of a conventional gate electrode in the prior art depicting a stressed conductive layer.

Figures 2 (a) - (h) are cross-sectional illustrations of the formation of a gate electrode with a conductive layer and recessed thick inner spacers and non-recessed thick outer spacers.

Figures 3 (a) - (i) are cross-sectional illustrations of the formation of a gate electrode with a conductive layer and recessed thin inner spacers and recessed thick outer spacers.

Figures 4 (a) - (i) are cross-sectional illustrations of the formation of a gate electrode with a conductive layer and non-recessed thin inner spacers and partially recessed outer spacers.

Figures 5 (a) - (m) are cross-sectional illustrations of the formation of a gate electrode with a conductive layer and two spacer stacks. The outermost spacer stack having recessed thin inner spacers and recessed thick outer spacers. The inner spacer stack having non-recessed thin inner spacers and non-recessed thin outer spacers.

Figures 6 (a) - (p) are cross-sectional illustrations of the formation of a gate electrode with a conductive layer and two spacer stacks. The outermost spacer stack

having recessed thin inner spacers and recessed thick outer spacers. The inner spacer stack having recessed thin inner spacers and recessed thin outer spacers.

DETAILED DESCRIPTION OF THE INVENTION

The present invention provides a method and a device to improve polycide resistance on gate electrodes less than $.20\text{ }\mu\text{m}$ in width. In the following description of the several embodiments of the invention, numerous details are set forth in order to provide a thorough understanding of the present invention. It will be appreciated by one having ordinary skill in the art that the present invention may be practiced without such specific details. In other instances, well-known structures and techniques have not been described in detail in order to avoid obscuring the subject matter of the present invention. It will be understood by those having ordinary skill in the art that the structures of the present invention may be formed by various techniques.

Referring now to the drawings, one embodiment of the present invention is shown in Figures 2a - h. Figure 2a illustrates a gate layer 220 formed on a thin insulative layer 210 on a substrate 200. In one embodiment, the gate layer 220 can be a polysilicon. In one embodiment, the gate layer 220 is less than $.20\text{ }\mu\text{m}$ in width. These structures are formed using conventional deposition and etching techniques well-known in the art.

In Figure 2b, a thick first spacer layer 230 is deposited or grown on the gate layer 220 and substrate 200. In one embodiment, the thick first spacer layer 230 can be an oxide. In one embodiment, the thick first spacer layer 230 can be deposited or grown to a thickness in the range of approximately $200 - 600\text{ }\text{\AA}$, for example, $300\text{ }\text{\AA}$. It should be noted that the thick first spacer layer 230 can be deposited or grown using deposition techniques that are well known in the art and are not described in detail herein.

In Figure 2c, a thick second spacer layer 240 is deposited or grown on the thick first spacer layer 230. In one embodiment, the thick second spacer layer 240 can be a nitride. In one embodiment, the thick second spacer layer 240 can be deposited or grown

to a thickness in the range of approximately 300 - 2000Å, for example, 800Å. It should be noted that the thick second spacer layer 240 can be deposited or grown using deposition techniques that are well known in the art and are not described in detail herein.

The thick second spacer layer 240 is etched to form the spacer structure illustrated in Figure 2d. In one embodiment, this etch is an anisotropic (directional) etch which will remove nitride, but not oxide. Examples of anisotropic etches are a dry etch or a plasma etch.

The thick first spacer layer 230 is recessed by etching to form the spacer structure illustrated in Figure 2e. The recessing creates an open space between the thick second spacer layer 240 and the gate layer 220. In one embodiment, the thick first spacer layer 230 is etched approximately 60 nm deeper than the surface of the gate layer 220. In one embodiment, the etching forms a space approximately 200 - 600Å, for example, 300Å, between the thick second spacer layer 240 and the gate layer 220. In one embodiment this etch is an isotropic (multidirectional) etch which will remove oxide, but not nitride. Examples of isotropic etches are dry or wet etches. It should be noted that the side walls of the gate layer 220 are now exposed creating a larger contact (reaction) surface area.

In Figure 2f, a reactant layer 250 is deposited, for example by sputter, electron beam evaporation, chemical vapor, or plasma deposition. In one embodiment, the reactant layer 250 can be a metal, such as titanium. However, other metals, such as cobalt, nickel, tantalum and platinum may also be used. The reactant layer 250 and the gate layer 220 are then annealed to form a conductive layer 260 as shown in Figure 2g. In one embodiment, the formed conductive layer 260 can be a polycide layer, which may also be called a polysilicide layer. It should be noted that silicides can be self-aligning or non-self-aligning, and if the silicide is self-aligning, it may be called a salicide. In one embodiment, the polycide can be titanium salicide (TiSi_2). Other polycides can be cobalt

salicide (CoSi_2), nickel salicide (NiSi), tantalum salicide (TaSi), or platinum salicide (PtSi). It is to be understood by one of ordinary skill in the art that polycides, other than self-aligning silicides, may also be formed. In one embodiment, the anneal may be performed using a rapid thermal annealing process in a nitrogen ambient. In one embodiment, additional anneals can be performed to decrease the resistance of the conductive layer 260. It is to be noted that the conductive layer 260 can now extend beyond the edges of the gate layer 220 and is not constrained and stressed by the thick first spacer layer 230.

The unreacted portion of reactant layer 250 is etched away leaving the conductive layer 260 as illustrated in Figure 2h. In one embodiment, this etch is an isotropic etch which will remove unreacted titanium, but not titanium salicide.

Another embodiment of the present invention is illustrated in Figures 3 a - i. Figure 3a illustrates a gate layer 320 formed on a thin insulative layer 310 on a substrate 300. In one embodiment, the gate layer 320 can be a polysilicon. In one embodiment, the gate layer 320 is less than $.20\text{ }\mu\text{m}$ in width. These structures are formed using conventional deposition and etching techniques well-known in the art.

In Figure 3b, a thin first spacer layer 330 is deposited or grown on the gate layer 320 and substrate 300. In one embodiment, the thin first spacer layer 330 can be an oxide. In one embodiment, the thin first spacer layer 330 is deposited or grown to a thickness in the range of approximately $50 - 300\text{ }\text{\AA}$, for example, $100\text{ }\text{\AA}$. It should be noted that the thin first spacer layer 330 can be deposited or grown using deposition techniques that are well known in the art and are not described in detail herein.

In Figure 3c, a thick second spacer layer 340 is deposited or grown on the thin first spacer layer 330. In one embodiment, the thick second spacer layer 340 can be a nitride. In one embodiment, the thick second spacer layer 340 is deposited or grown to a thickness in the range of approximately $300 - 2000\text{ }\text{\AA}$, for example, $800\text{ }\text{\AA}$. It should be

noted that the thick second spacer layer 340 can be deposited or grown using deposition techniques that are well known in the art and are not described in detail herein.

The thick second spacer layer 340 is etched a first time to form the structure illustrated in Figure 3d. In one embodiment, this etch is an anisotropic (directional) etch which will remove nitride, but not oxide. Examples of anisotropic etches are a dry etch or a plasma etch.

The thick second spacer layer 340 is then recessed by etching a second time to form the spacer structure illustrated in Figure 3e. In one embodiment, the thick second spacer layer 340 is etched approximately 60 nm deeper than the surface level of the gate layer 320. In one embodiment, this etch is an isotropic (multidirectional) etch which will remove nitride, but not oxide. Examples of isotropic etches are a wet or dry etch.

The thin first spacer layer 330 is then recessed by etching to form the spacer structure illustrated in Figure 3f. In one embodiment, this etch is an isotropic (multidirectional) etch which will remove oxide, but not nitride. Examples of isotropic etches are a dry, wet or chemical bath etch. It should further be noted that the side walls of the gate layer 320 are now exposed creating a larger contact (reaction) surface area.

In Figure 3g, a reactant layer 350 is deposited, for example, by sputter, electron beam evaporation, chemical vapor, or plasma deposition. In one embodiment, the reactant layer 350 can be a metal, such as titanium. However, other metals, such as cobalt, nickel, tantalum and platinum may also be used.

The reactant layer 350 and the gate layer 320 are then annealed to form a conductive layer 360 as shown in Figure 3h. In one embodiment, the formed conductive layer 360 can be a polycide, which may also be called a polysilicide layer. It should be noted that silicides can be self-aligning or non-self-aligning, and if the silicide is self-aligning, it may be called a salicide. In one embodiment, the polycide can be titanium salicide (TiSi_2). Other polycides can be cobalt salicide (CoSi_2), nickel salicide (NiSi),

tantalum salicide (TaSi), or platinum salicide (PtSi). It is to be understood by one of ordinary skill in the art that polycides, other than self-aligning silicides, may also be formed. In one embodiment, the anneal may be performed using a rapid thermal annealing process in a nitrogen ambient. In one embodiment, additional anneals can be performed to decrease the resistance of the conductive layer 360. It is to be noted that the conductive layer 360 can now extend beyond the edges of the gate layer 320 and is not constrained and stressed.

The unreacted portion of reactant layer 350 is etched away leaving the conductive layer 360 as illustrated in Figure 3i. In one embodiment, this etch is an isotropic etch which will remove unreacted titanium, but not titanium salicide.

Another embodiment of the present invention is illustrated in Figures 4 a - i. Figure 4a illustrates a gate layer 420 formed on a thin insulative layer 410 on a silicon substrate 400. In one embodiment, the gate layer 420 can be polysilicon. In one embodiment, the gate layer 420 is less than .20 μm in width. These structures are formed using conventional deposition and etching techniques well-known in the art.

In Figure 4b, a thin first spacer layer 430 is deposited or grown on the gate layer 420 and substrate 400. In one embodiment, the thin first spacer layer 430 can be an oxide. In one embodiment, the thin first spacer layer 430 is deposited or grown to a thickness in the range of approximately 50 - 300Å, for example, 100Å. It should be noted that the thin first spacer layer 430 can be deposited or grown using deposition techniques that are well known in the art and are not described in detail herein.

In Figure 4c, a thick second spacer layer 440 is deposited or grown on the thin first spacer layer 430. In one embodiment, the thick second spacer layer 440 can be a nitride. In one embodiment, the thick second spacer layer 440 can be deposited or grown to a thickness in the range of approximately 300 - 2000Å, for example, 800Å. It should be noted that the thick second spacer layer 440 can be deposited or grown using

deposition techniques that are well known in the art and are not described in detail herein.

The thick second spacer layer 440 is etched a first time to form the structure illustrated in Figure 4d. In one embodiment, this etch is an anisotropic (directional) etch which will remove nitride, but not oxide. Examples of anisotropic etches are a dry etch or a plasma etch.

The thick second spacer layer 440 is then partially recessed by etching a second time to form the spacer structure illustrated in Figure 4e. In one embodiment, the partial recess creates a thin second spacer wall 470 adjacent to the thin first spacer layer 430. In one embodiment, the thin second spacer wall 470 can be in the range of approximately 50 - 200Å, for example, 100Å, in width and can extend approximately 60 nm deeper than the surface level of the gate layer 420. In one embodiment, this etch is an anisotropic (directional) etch which will remove nitride, but not oxide. Examples of anisotropic etches are a dry etch or a plasma etch.

Following the partial recessing of the thick second spacer layer 440, the thin first spacer layer 430 is etched to form the spacer structure illustrated in Figure 4f. In one embodiment, this etch is an isotropic (multidirectional) etch which will remove oxide, but not nitride. Examples of isotropic etches are a dry, wet or chemical bath etch.

In Figure 4g, a reactant layer 450 is deposited, for example, by sputter, electron beam evaporation, chemical vapor, or plasma deposition. In one embodiment, the reactant layer 450 can be a metal, such as titanium. However, other metals, such as cobalt, nickel, tantalum and platinum may also be used.

The reactant layer 450 and the gate layer 420 are then annealed to form a conductive layer 460 as shown in Figure 4h. In one embodiment, the conductive layer 460 can be a polycide, which may also be called a polysilicide layer. It should be noted that silicides can be self-aligning or non-self-aligning, and if the silicide is self-aligning,

it may be called a salicide. In one embodiment, the polycide can be titanium salicide (TiSi_2). Other polycides can be cobalt salicide (CoSi_2), nickel salicide (NiSi), tantalum salicide (TaSi), or platinum salicide (PtSi). It is to be understood by one of ordinary skill in the art that polycides, other than self-aligning silicides, may also be formed. In one embodiment, the anneal may be performed using a rapid thermal annealing process in a nitrogen ambient. In one embodiment, additional anneals can be performed to decrease the resistance of the conductive layer 460. It is to be noted that the conductive layer 460 can now extend beyond the edges of the gate layer 420 due to flexibility in the thin spacer walls formed from the thin first spacer layer 430 and the thin second spacer walls 470.

The unreacted portion of reactant layer 450 is etched away leaving the conductive layer 460 as illustrated in Figure 4i. In one embodiment, this etch is an isotropic etch which will remove unreacted titanium, but not titanium salicide.

Another embodiment of the present invention is illustrated in Figures 5 a - m. Figure 5a illustrates a gate layer 520 formed on a thin insulative layer 510 on a substrate 500. In one embodiment, the gate layer 520 can be polysilicon. In one embodiment, the polysilicon gate layer 520 is less than $.20\ \mu\text{m}$ in width. These structures are formed using conventional deposition and etching techniques well-known in the art.

In Figure 5b, a thin first spacer layer 530 is deposited or grown on the gate layer 520 and substrate 500. In one embodiment, the thin first spacer layer 530 can be an oxide. In one embodiment, the thin first spacer layer 530 is deposited or grown to a thickness in the range of approximately $50 - 150\text{\AA}$, for example, $50\text{\AA}$. It should be noted that the thin first spacer layer 530 can be deposited or grown using deposition techniques that are well known in the art and are not described in detail herein.

In Figure 5c, a thin second spacer layer 540 is deposited or grown on the thin first spacer layer 530. In one embodiment, the thin second spacer layer 540 can be a nitride.

In one embodiment, the thin second spacer layer 540 can be deposited or grown to a thickness in the range of approximately 50 - 150Å, for example, 50Å. It should be noted that the thin second spacer layer 540 can be deposited or grown using deposition techniques that are well known in the art and are not described in detail herein.

The thin second spacer layer 540 is etched a first time to form the structure illustrated in Figure 5d. In one embodiment, this etch is an anisotropic (directional) etch which will remove nitride, but not oxide. Examples of anisotropic etches are a dry etch or a plasma etch.

Following the etch of the thin second spacer layer 540, the thin first spacer layer 530 is etched to form the structure illustrated in Figure 5e. In one embodiment, this etch is an isotropic (multidirectional) which will remove oxide, but not nitride. Examples of isotropic etches are dry or wet etches. It should be further noted that at this point in a process flow, implants of dopants can be added to the structure to enhance circuit performance.

In Figure 5f, a thin third spacer layer 550 is deposited or grown. In one embodiment, the thin third spacer layer 550 can be an oxide. In one embodiment, the thin third spacer layer 550 is deposited or grown to a thickness in the range of approximately 50 - 300Å, for example, 100Å. It should be noted that the thin third spacer layer 550 can be deposited or grown using deposition techniques that are well known in the art and are not described in detail herein.

In Figure 5g, a thick fourth spacer layer 560 is deposited or grown on the thin third spacer layer 550. In one embodiment, the thick fourth spacer layer 560 can be a nitride. In one embodiment, the thick fourth spacer layer 560 is deposited or grown to a thickness in the range of approximately 300 - 2000Å, for example, 800Å. It should be noted that the thick fourth spacer layer 560 can be deposited or grown using deposition techniques that are well known in the art and are not described in detail herein.

The thick fourth spacer layer 560 is etched a first time to form the structure illustrated in Figure 5h. In one embodiment, this etch is an anisotropic (directional) etch which will remove nitride, but not oxide. Examples of anisotropic etches are a dry etch or a plasma etch.

The thick fourth spacer layer 560 is then recessed by etching a second time to form the spacer structure illustrated in Figure 5i. In one embodiment, the thick fourth spacer layer 560 is etched approximately 60 nm deeper than the surface level of the gate layer 520. In one embodiment, this etch is an isotropic (multidirectional) etch which will remove nitride, but not oxide. Examples of isotropic etches are wet or dry etches.

The thin third spacer layer 550 is then recessed by etching to form the spacer structure illustrated in Figure 5j. In one embodiment, this etch is an isotropic (multidirectional) etch which will remove oxide, but not nitride. Examples of isotropic etches are a dry, wet or chemical bath etch.

In Figure 5k, a reactant layer 570 is deposited, for example, by sputter, electron beam evaporation, chemical vapor, or plasma deposition. In one embodiment, the reactant layer 570 can be a metal such as titanium. However, other metals, such as cobalt, nickel, tantalum and platinum may also be used.

The reactant layer 570 and the gate layer 520 are then annealed to form a conductive layer 580 as shown in Figure 5l. In one embodiment, the conductive layer 580 can be a polycide, which may also be called a polysilicide layer. It should be noted that silicides can be self-aligning or non-self-aligning, and if the silicide is self-aligning, it may be called a salicide. In one embodiment, the polycide can be titanium salicide (TiSi_2). Other polycides can be cobalt salicide (CoSi_2), nickel salicide (NiSi), tantalum salicide (TaSi), or platinum salicide (PtSi). It is to be understood by one of ordinary skill in the art that polycides, other than self-aligning silicides, may also be formed. In one embodiment, the anneal may be performed using a rapid thermal annealing process in a

nitrogen ambient. In one embodiment, additional anneals can be performed to decrease the resistance of the conductive layer 580. It is to be noted that the conductive layer 580 can now extend beyond the edges of the gate layer 520 due to flexibility in the thin spacer walls formed from the thin first spacer layer 530 and the thin second spacer layer 540.

The unreacted reactant layer 570 is etched away leaving the conductive layer 580 as illustrated in Figure 5m. In one embodiment, this etch is an isotropic etch which will remove unreacted titanium, but not titanium salicide.

Another embodiment of the present invention is illustrated in Figures 6 a - p. Figure 6a illustrates a gate layer 620 formed on a thin insulative layer 610 on a substrate 600. In one embodiment, the gate layer 620 can be polysilicon. In one embodiment, the gate layer 620 is less than .20 μm in width. These structures are formed using conventional deposition and etching techniques well-known in the art.

In Figure 6b, a thin first spacer layer 630 is deposited or grown on the gate layer 620 and substrate 600. In one embodiment, the thin first spacer layer 630 can be an oxide. In one embodiment, the thin first spacer layer 630 is deposited or grown to a thickness in the range of approximately 50 - 150Å, for example, 50Å. It should be noted that the thin first spacer layer 630 can be deposited or grown using deposition techniques that are well known in the art and are not described in detail herein.

In Figure 6c, a thin second spacer layer 640 is deposited or grown on the thin first spacer layer 630. In one embodiment, the thin second spacer layer 640 can be a nitride. In one embodiment, the thin second spacer layer 640 can be deposited or grown to a thickness in the range of approximately 50 - 150Å, for example, 50Å. It should be noted that the thin second spacer layer 640 can be deposited or grown using deposition techniques that are well known in the art and are not described in detail herein.

The thin second spacer layer 640 is etched a first time to form the structure illustrated in Figure 6d. In one embodiment, this etch is an anisotropic (directional) etch which will remove nitride, but not oxide. Examples of anisotropic etches are a dry etch or a plasma etch.

Following the etch of the thin second spacer layer 640, the thin first spacer layer 630 is etched to form the structure illustrated in Figure 6e. In one embodiment, this etch is an isotropic (multidirectional) which will attack oxide, but not nitride. Examples of isotropic etches are a dry, wet or chemical bath etch. It should be further noted that at this point in a process flow, implants of dopants can be added to the structure to enhance circuit performance.

In Figure 6f, a thin third spacer layer 650 is deposited or grown. In one embodiment, the thin third spacer layer 650 can be an oxide. In one embodiment, the thin third spacer layer 650 is deposited or grown to a thickness in the range of approximately 50 - 300Å, for example 100Å. It should be noted that the thin third spacer layer 650 can be deposited or grown using deposition techniques that are well known in the art and are not described in detail herein.

In Figure 6g, a thick fourth spacer layer 660 is deposited or grown on the thin third spacer layer 650. In one embodiment, the thick fourth spacer layer 660 can be a nitride. In one embodiment, the thick fourth spacer layer 660 is deposited or grown to a thickness in the range of approximately 300 - 2000Å, for example, 800Å. It should be noted that the thick fourth spacer layer 660 can be deposited or grown using deposition techniques that are well known in the art and are not described in detail herein.

The thick fourth spacer layer 660 is etched a first time to form the structure illustrated in Figure 6h. In one embodiment, this etch is an anisotropic (directional) etch which will remove nitride, but not oxide. Examples of anisotropic etches are a dry etch or a plasma etch.

The thick fourth spacer layer 660 is then recessed by etching a second time to form the spacer structure illustrated in Figure 6i. In one embodiment, the thick fourth spacer layer 660 is etched approximately 60 nm deeper than the surface level of the gate layer 620. In one embodiment, this etch is an isotropic (multidirectional) etch which will remove nitride, but not oxide. Examples of isotropic etches are a wet or dry etch.

The thin third spacer layer 650 is then recessed by etching to form the spacer structure illustrated in Figure 6j. In one embodiment, this etch is an isotropic (multidirectional) etch which will remove oxide, but not nitride. Examples of isotropic etches are dry or wet etches.

At this point, further etches are still to be performed, however, the substrate 600 is left exposed. Thus, if a following etch chemistry is utilized which can remove the substrate 600, the substrate 600 will need to be protected. Thus, a protective layer, for example, an oxide layer, can be provided. The provision of a protective layer is described together with the figures that follow. Alternatively, if a following etch chemistry does not remove the substrate 600, then the process can continue without the necessity of providing and removing a protective layer.

In Figure 6k, a thin protective layer 670 is deposited or grown on the substrate 600. In one embodiment, the thin protective layer 670 can be oxide. In one embodiment, the thin protective layer 670 is deposited or grown to a thickness in the range of approximately 50 - 300Å, for example, 50Å. In one embodiment, the thin protective layer 670 can be an oxide grown by annealing a silicon substrate 600 in an oxygen ambient.

The thin second spacer layer 640 is recessed by etching to form the spacer structure illustrated in Figure 6l. In one embodiment, this etch is an anisotropic (directional) etch which will remove nitride, but not oxide. Examples of anisotropic etches are a dry etch or a plasma etch.

The thin protective layer 670 is removed and the thin first spacer layer 630 recessed by etching a second time to form the spacer structure illustrated in Figure 6m. In one embodiment, the thin first spacer layer 630 is recessed approximately 60 nm deeper than the surface level of the gate layer 620. In one embodiment, this etch is an isotropic (multidirectional) etch which will remove oxide, but not nitride. Examples of isotropic etches are a wet, dry or chemical bath etch. It should be noted that the side walls of the gate layer 620 are now exposed creating a larger contact (reaction) surface area.

In Figure 6n, a reactant layer 680 is deposited, for example, by sputter, electron beam evaporation, chemical vapor, or plasma deposition. In one embodiment, the reactant layer 680 can be a metal, such as titanium. However, other metals, such as cobalt, nickel, tantalum and platinum may also be used.

The reactant layer 680 and the gate layer 620 are then annealed to form a conductive layer 690 as shown in Figure 6o. In one embodiment, the conductive layer 690 can be a polycide, which may also be called a polysilicide layer. It should be noted that silicides can be self-aligning or non-self-aligning, and if the silicide is self-aligning, it may be called a salicide. In one embodiment, the polycide can be titanium salicide (TiSi_2). Other polycides can be cobalt salicide (CoSi_2), nickel salicide (NiSi), tantalum salicide (TaSi), or platinum salicide (PtSi). It is to be understood by one of ordinary skill in the art that polycides, other than self-aligning silicides, may also be formed. In one embodiment, the anneal may be performed using a rapid thermal annealing process in a nitrogen ambient. In one embodiment, additional anneals can be performed to decrease the resistance of the conductive layer 690. It is to be noted that the conductive layer 690 can now extend beyond the edges of the gate layer 620 and is not constrained and stressed.

The unreacted reactant layer 680 is etched away leaving the conductive layer 690 as illustrated in Figure 6p. In one embodiment, this etch is an isotropic etch which will remove unreacted titanium, but not titanium salicide.

Through out the specification, reference has been made to isotropic and anisotropic etching. It should be noted that the present invention may be performed using these etch processes interchangeably, however, such interchanging of etch processes may cause other complications. The process steps as defined above are the preferred manner in which to perform the present invention.

Additionally, throughout the specification, it has been stated that the etch processes remove only the nitride or oxide layers, however, it should be noted that such etch processes selectively remove the nitride or oxide. In other words, an etch to remove nitride will remove nitride at a faster rate than oxide, such that more nitride is removed and very little oxide is removed; and, an etch to remove oxide will remove oxide at a faster rate than nitride, such that more oxide is removed and very little nitride is removed.

The above described embodiments of the method and device of the present invention provide improved polycide resistance in polysilicon gate widths below $.20\mu\text{m}$. As earlier described, conductive layers, such as the polycide, titanium salicide, can expand during formation. Previous gate electrode structures had spacer structures which constrained this expansion. This led to a stressed conductive layer that exhibited increased resistance. The several embodiments of the present invention, reduce the stress on the formed conductive layer thereby improving the resistance. In some embodiments, spacers are recessed to remove constraints on the expansion of the conductive layer. In other embodiments, spacers are partially recessed to provide thin spacer walls which flex to dissipate stress. In other embodiments, dual spacer stacks that are recessed and partially recessed also dissipate or remove stress on the conductive layer. It is this

reduction in the stress by the several embodiments of the present invention, that provides improved resistance. Also, in several of the embodiments the side walls of the gate layer are exposed to allow greater surface area. This aids in formation of the conductive layer by providing for increased nucleation sites. By aiding in formation of the conductive layer, process yields increase.

In the foregoing specification, the invention has been described with reference to specific exemplary embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention as set forth in the appended claims. The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense.



CLAIMS

What is claimed is:

1. A gate electrode formed on a substrate comprising:
an insulative layer formed on a substrate;
a gate layer formed on the insulative layer;
a conductive layer formed on the gate layer;
thick first spacers formed adjacent to opposite sides of the gate layer wherein the thick first spacers are recessed to create an open space between the both the gate layer and the conductive layer and thick second spacers; and,
thick second spacers formed adjacent to each of the thick first spacers.
2. The gate electrode of claim 1 wherein the insulative layer is an oxide.
3. The gate electrode of claim 2 wherein the gate layer is a polysilicon.
4. The gate electrode of claim 3 wherein the conductive layer is a polycide.
5. The gate electrode of claim 4 wherein the thick first spacers are an oxide.
6. The gate electrode of claim 5 wherein the thick second spacers are a nitride.
7. The gate electrode of claim 6 wherein the polycide is cobalt salicide (CoSi_2).
8. The gate electrode of claim 6 wherein the polycide is nickel salicide (NiSi).
9. The gate electrode of claim 6 wherein the polycide is platinum salicide (PtSi).
10. The gate electrode of claim 6 wherein the polycide is tantalum salicide (TaSi).
11. The gate electrode of claim 6 wherein the polycide is titanium salicide (TiSi_2).
12. A gate electrode formed on a substrate comprising:
an insulative layer formed on a substrate;
a gate layer formed on the insulative layer;
a conductive layer formed on the gate layer;
thin first spacers formed adjacent to opposite sides of the gate layer wherein the thin first spacers are recessed; and,



thick second spacers formed adjacent to each of the thin first spacers wherein the thick second spacers are recessed.

13. The gate electrode of claim 12 wherein the insulative layer is an oxide.
14. The gate electrode of claim 13 wherein the gate layer is a polysilicon.
15. The gate electrode of claim 14 wherein the conductive layer is a polycide.
16. The gate electrode of claim 15 wherein the thin first spacers are an oxide.
17. The gate electrode of claim 16 wherein the thick second spacers are a nitride.
18. The gate electrode of claim 17 wherein the polycide is cobalt salicide (CoSi_2).
19. The gate electrode of claim 17 wherein the polycide is nickel salicide (NiSi).
20. The gate electrode of claim 17 wherein the polycide is titanium salicide (TiSi_2).
21. A gate electrode formed on a substrate comprising:
 - an insulative layer formed on a substrate;
 - a gate layer formed on the insulative layer;
 - a conductive layer formed on the gate layer;
 - thin first spacers formed adjacent to opposite sides of the gate layer; and,
 - thick second spacers formed adjacent to each of the thin first spacers wherein the thick second spacers are partially recessed to form thin second spacer walls adjacent to the thin first spacers in a region adjacent to the conductive layer.
22. The gate electrode of claim 21 wherein the insulative layer is an oxide.
23. The gate electrode of claim 22 wherein the gate layer is a polysilicon.
24. The gate electrode of claim 23 wherein the conductive layer is a polycide.
25. The gate electrode of claim 24 wherein the thin first spacers are an oxide.
26. The gate electrode of claim 25 wherein the thick second spacers are a nitride.
27. The gate electrode of claim 26 wherein the polycide is cobalt salicide (CoSi_2).
28. The gate electrode of claim 26 wherein the polycide is nickel salicide (NiSi).
29. The gate electrode of claim 26 wherein the polycide is titanium salicide (TiSi_2).
30. A gate electrode formed on a substrate comprising:



an insulative layer formed on a substrate;
a gate layer formed on the insulative layer;
a conductive layer formed on the gate layer;
thin first spacers formed adjacent to opposite sides of the gate layer;
thin second spacers formed adjacent to each of the thin first spacers;
thin third spacers formed adjacent to each of the thin second spacers wherein the thin third spacers are recessed; and,

thick fourth spacers formed adjacent to each of the thin third spacers wherein the thick fourth spacers are recessed.

31. The gate electrode of claim 30 wherein the insulative layer is an oxide.
32. The gate electrode of claim 31 wherein the gate layer is a polysilicon.
33. The gate electrode of claim 32 wherein the conductive layer is a polycide.
34. The gate electrode of claim 33 wherein the thin first spacers are an oxide.
35. The gate electrode of claim 34 wherein the thin second spacers are a nitride.
36. The gate electrode of claim 35 wherein the thin third spacers are an oxide.
37. The gate electrode of claim 36 wherein the thick fourth spacers are a nitride.
38. The gate electrode of claim 37 wherein the polycide is cobalt salicide (CoSi_2).
39. The gate electrode of claim 37 wherein the polycide is nickel salicide (NiSi).
40. The gate electrode of claim 37 wherein the polycide is titanium salicide (TiSi_2).

41. A gate electrode formed on a substrate comprising:
an insulative layer formed on a substrate;
a gate layer formed on the insulative layer;
a conductive layer formed on the gate layer;
thin first spacers formed adjacent to opposite sides of the gate layer wherein the thin first spacers are recessed;
thin second spacers formed adjacent to opposite sides of the thin first spacers wherein the thin second spacers are recessed;



thin third spacers formed adjacent to opposite sides of the thin second spacers wherein the thin third spacers are recessed; and,

thick fourth spacers formed adjacent to opposite sides of the thin third spacers wherein the thick fourth spacers are recessed.

42. The gate electrode of claim 41 wherein the insulative layer is an oxide.
 43. The gate electrode of claim 42 wherein the gate layer is a polysilicon.
 44. The gate electrode of claim 43 wherein the conductive layer is a polycide.
 45. The gate electrode of claim 44 wherein the thin first spacers are an oxide.
 46. The gate electrode of claim 45 wherein the thin second spacers are a nitride.
 47. The gate electrode of claim 46 wherein the thin third spacers are an oxide.
 48. The gate electrode of claim 47 wherein the thick fourth spacers are a nitride.
 49. The gate electrode of claim 48 wherein the polycide is cobalt salicide (CoSi_2).
 50. The gate electrode of claim 48 wherein the polycide is nickel salicide (NiSi).
 51. The gate electrode of claim 48 wherein the polycide is titanium salicide (TiSi_2).
 52. A method for forming a gate electrode comprising the steps of:
 - providing a substrate with an insulative layer deposited thereon;
 - forming a gate layer on the insulative layer;
 - depositing a thick first spacer layer on the gate layer and the substrate;
 - depositing a thick second spacer layer on the thick first spacer layer;
 - removing a portion of the thick second spacer layer to form thick second spacers adjacent to the thick first spacer layer;
 - removing a portion of the thick first spacer layer to form recessed thick first spacers adjacent to the gate layer wherein a space is formed between the gate layer and the thick second spacers;
 - depositing a layer of reactant on the gate layer;
 - annealing the layer of reactant and the gate layer to form a conductive layer;
- and,
- removing the unreacted reactant layer.



53. The method of claim 52 wherein removing a portion of the thick second spacer layer to form thick second spacers is by anisotropic etching.
54. The method of claim 53 wherein the removing a portion of the thick first spacer layer to form thick first spacers is by isotropic etching.
55. The method of claim 54 wherein the insulative layer is an oxide.
56. The method of claim 55 wherein the gate layer is a polysilicon.
57. The method of claim 56 wherein the reactant is a metal.
58. The method of claim 57 wherein said thick first spacer layer is an oxide.
59. The method of claim 58 wherein said thick second spacer layer is a nitride.
60. The method of claim 59 wherein the conductive layer is a polycide.
61. The method of claim 60 wherein the metal is cobalt.
62. The method of claim 61 wherein the polycide is cobalt salicide (CoSi_2).
63. The method of claim 60 wherein the metal is nickel.
64. The method of claim 63 wherein the polycide is nickel salicide (NiSi).
65. The method of claim 60 wherein the metal is platinum.
66. The method of claim 65 wherein the polycide is platinum salicide (PtSi).
67. The method of claim 60 wherein the metal is tantalum.
68. The method of claim 67 wherein the polycide is tantalum salicide (TaSi).
69. The method of claim 60 wherein the metal is titanium.
70. The method of claim 69 wherein the polycide is titanium salicide (TiSi_2).
71. A method for forming a gate electrode comprising the steps of:
providing a substrate with a gate oxide layer deposited thereon;
forming a gate layer on the insulative layer;
depositing a thin first spacer layer on the gate layer and the substrate;
depositing a thick second spacer layer on the thin first spacer layer;
removing a portion of the thick second spacer layer to form recessed thick second spacers;
removing a portion of the thin first spacer layer to form recessed thin first spacers;



- depositing a layer of reactant on the gate layer;
annealing the layer of reactant and the gate layer to form a conductive layer;
and,
removing the unreacted reactant layer.
72. The method of claim 71 wherein removing a portion of the thick second spacer layer to form thick second spacers is by anisotropic etching.
73. The method of claim 72 wherein the removing a portion of the thin first spacer layer to form thin first spacers is by isotropic etching.
74. The method of claim 73 wherein the insulative layer is an oxide.
75. The method of claim 74 wherein the gate layer is a polysilicon.
76. The method of claim 75 wherein the reactant is a metal.
77. The method of claim 76 wherein said thin first spacer layer is an oxide.
78. The method of claim 77 wherein said thick second spacer layer is a nitride.
79. The method of claim 78 wherein the conductive layer is a polycide.
80. The method of claim 79 wherein the metal is cobalt.
81. The method of claim 80 wherein the polycide is cobalt salicide (CoSi_2).
82. The method of claim 79 wherein the metal is nickel.
83. The method of claim 82 wherein the polycide is nickel salicide (NiSi).
84. The method of claim 79 wherein the metal is titanium.
85. The method of claim 84 wherein the polycide is titanium salicide (TiSi_2).
86. A method for forming a gate electrode comprising the steps of:
providing a substrate with an insulative layer deposited thereon;
forming a gate layer on the insulative layer;
depositing a thin first spacer layer on the gate layer and the substrate;
depositing a thick second spacer layer on the thin first spacer layer;
removing a portion of the thick second spacer layer to form partially recessed thick second spacers;
removing a portion of the thin first spacer layer to form thin first spacers;
depositing a layer of reactant on the gate layer;



annealing the layer of reactant and the gate layer to form a conductive layer;
and,

removing the unreacted reactant layer.

87. The method of claim 86 wherein removing a portion of the thick second spacer layer to form partially recessed thick second spacers further comprises:

removing a first portion of the thick second spacer by anisotropic etching;

and,

removing a second portion of the thick second spacer layer by isotropic etching to form thin second spacer walls adjacent to the thin first spacers and in a region adjacent to the conductive layer.

88. The method of claim 87 wherein removing a portion of the thin first spacer layer to form thin first spacers is by anisotropic etching.

89. The method of claim 88 wherein the insulative layer is an oxide.

90. The method of claim 89 wherein the gate layer is a polysilicon.

91. The method of claim 90 wherein the reactant is a metal.

92. The method of claim 91 wherein said thin first spacer layer is an oxide.

93. The method of claim 92 wherein said thick second spacer layer is a nitride.

94. The method of claim 93 wherein the conductive layer is a polycide.

95. The method of claim 94 wherein the metal is cobalt.

96. The method of claim 95 wherein the polycide is cobalt salicide (CoSi_2).

97. The method of claim 94 wherein the metal is nickel.

98. The method of claim 97 wherein the polycide is nickel salicide (NiSi).

99. The method of claim 94 wherein the metal is titanium.

100. The method of claim 99 wherein the polycide is titanium salicide (TiSi_2).

101. A method for forming a gate electrode comprising the steps of :

providing a substrate with an insulative layer deposited thereon;

forming a gate layer on the insulative layer;

depositing a thin first spacer layer on the gate layer and the substrate;

depositing a thin second spacer layer on the thin first spacer layer;



- removing a portion of the thin second spacer layer to form thin second spacers;
- removing a portion of the thin first spacer layer to form thin first spacers;
- depositing a thin third spacer layer;
- depositing a thick fourth spacer layer on the thin third spacer layer;
- removing a portion of the thick fourth spacer layer to form recessed thick fourth spacers;
- removing a portion of the thin third spacer layer to form recessed thin third spacers;
- depositing a layer of reactant on the gate layer;
- annealing the layer of reactant and the gate layer to form a conductive layer;
- and,
- removing the unreacted reactant layer.
102. The method of claim 101 wherein removing a portion of the thin second spacer layer to form thin second spacers is by anisotropic etching.
103. The method of claim 102 wherein removing a portion of the thin first spacer layer to form thin first spacers is by anisotropic etching.
104. The method of claim 103 wherein removing a portion of the thick fourth spacer layer to form recessed thick fourth spacers further comprises:
- removing a first portion of the thick fourth spacer layer by anisotropic etching; and,
- removing a second portion of the thick fourth spacer by isotropic etching.
105. The method of claim 104 wherein removing a portion of the thin third spacer layer to form recessed thin third spacers is by anisotropic etching.
106. The method of claim 105 wherein the insulative layer is an oxide.
107. The method of claim 106 wherein the gate layer is a polysilicon.
108. The method of claim 107 wherein the reactant is a metal.
109. The method of claim 108 wherein said thin first spacer layer is an oxide.
110. The method of claim 109 wherein said thin second spacer layer is a nitride.



111. The method of claim 110 wherein said thin third spacer layer is an oxide.
112. The method of claim 111 wherein said thick fourth spacer layer is a nitride.
113. The method of claim 112 wherein the conductive layer is a polycide.
114. The method of claim 113 wherein the metal is cobalt.
115. The method of claim 114 wherein the polycide is cobalt salicide (CoSi_2).
116. The method of claim 113 wherein the metal is nickel.
117. The method of claim 116 wherein the polycide is nickel salicide (NiSi).
118. The method of claim 113 wherein the metal is titanium.
119. The method of claim 118 wherein the polycide is titanium salicide (TiSi_2).
120. A method for forming a gate electrode comprising the steps of :
 - providing a substrate with an insulative layer deposited thereon;
 - forming a gate layer on the insulative layer;
 - depositing a thin first spacer layer on the gate layer and the substrate;
 - depositing a thin second spacer layer on the thin first spacer layer;
 - removing a portion of the thin second spacer layer to form thin second spacers;
 - removing a portion of the thin first spacer layer to form thin first spacers;
 - depositing a thin third spacer layer;
 - depositing a thick fourth spacer layer on the thin third spacer layer;
 - removing a portion of the thick fourth spacer layer to form recessed thick fourth spacers;
 - removing a portion of the thin third spacer layer to form recessed third spacers;
 - forming a protective layer on the substrate and gate layer;
 - removing a portion of the thin second spacers to form recessed thin second spacers;
 - removing the protective layer and removing a portion of the thin first spacers to form recessed thin first spacers;
 - depositing a layer of reactant on the gate layer;



- annealing the layer of reactant and the gate layer to form a conductive layer;
- and,
- removing the unreacted reactant layer.
121. The method of claim 120 wherein removing a portion of the thin second spacer layer to form thin second spacers is by anisotropic etching.
122. The method of claim 121 wherein removing a portion of the thin first spacer layer to form thin first spacers is by anisotropic etching.
123. The method of claim 122 wherein removing a portion of the thick fourth spacer layer to form recessed thick fourth spacers further comprises:
- removing a first portion of the thick fourth spacer layer by anisotropic etching;
- and,
- removing a second portion of the thick fourth spacer layer by isotropic etching.
124. The method of claim 123 wherein removing a portion of the thin third spacer layer to form recessed thin third spacers is by anisotropic etching.
125. The method of claim 124 wherein removing a portion of the thin second spacers to form recessed thin second spacers is by isotropic etching.
126. The method of claim 125 wherein removing the protective layer and removing a portion of the thin first spacers to form recessed thin first spacers is by isotropic etching.
127. The method of claim 126 wherein the insulative layer is an oxide.
128. The method of claim 127 wherein the gate layer is a polysilicon.
129. The method of claim 128 wherein the reactant is a metal.
130. The method of claim 129 wherein the thin first spacer layer is an oxide.
131. The method of claim 130 wherein the thin second spacer layer is a nitride.
132. The method of claim 131 wherein the thin third spacer layer is an oxide.
133. The method of claim 132 wherein the thick fourth spacer layer is a nitride.
134. The method of claim 133 wherein the protective layer is an oxide.
135. The method of claim 133 wherein the conductive layer is a polycide.



136. The method of claim 135 wherein the metal is cobalt.
137. The method of claim 136 wherein the polycide is cobalt salicide (CoSi_2).
138. The method of claim 135 wherein the metal is nickel.
139. The method of claim 138 wherein the polycide is nickel salicide (NiSi).
140. The method of claim 135 wherein the metal is titanium.
141. The method of claim 140 wherein the polycide is titanium salicide (TiSi_2).
142. A method for forming a gate electrode comprising the steps of :
providing a substrate with an insulative layer deposited thereon;
forming a gate layer on the insulative layer;
depositing a thin first spacer layer on the gate layer and the substrate;
depositing a thin second spacer layer on the thin first spacer layer;
removing a portion of the thin second spacer layer to form thin second spacers;
removing a portion of the thin first spacer layer to form thin first spacers;
depositing a thin third spacer layer;
depositing a thick fourth spacer layer on the thin third spacer layer;
removing a portion of the thick fourth spacer layer to form recessed thick fourth spacers;
removing a portion of the thin third spacer layer to form recessed third spacers;
removing a portion of the thin second spacers to form recessed thin second spacers;
removing a portion of the thin first spacers to form recessed thin first spacers;
depositing a layer of reactant on the gate layer;
annealing the layer of reactant and the gate layer to form a conductive layer;
and,
removing the unreacted reactant layer.
143. The method of claim 142 wherein removing a portion of the thin second spacer layer to form thin second spacers is by anisotropic etching.



144. The method of claim 143 wherein removing a portion of the thin first spacer layer to form thin first spacers is by anisotropic etching.
145. The method of claim 144 wherein removing a portion of the thick fourth spacer layer to form recessed thick fourth spacers further comprises:
- removing a first portion of the thick fourth spacer layer by anisotropic etching;
 - and,
 - removing a second portion of the thick fourth spacer layer by isotropic etching.
146. The method of claim 145 wherein removing a portion of the thin third spacer layer to form recessed thin third spacers is by anisotropic etching.
147. The method of claim 146 wherein removing a portion of the thin second spacers to form recessed thin second spacers is by isotropic etching.
148. The method of claim 147 wherein removing a portion of the thin first spacers to form recessed thin first spacers is by isotropic etching.
149. The method of claim 148 wherein the insulative layer is an oxide.
150. The method of claim 149 wherein the gate layer is a polysilicon.
151. The method of claim 150 wherein the reactant is a metal.
152. The method of claim 151 wherein the thin first spacer layer is an oxide.
153. The method of claim 152 wherein the thin second spacer layer is a nitride.
154. The method of claim 153 wherein the thin third spacer layer is an oxide.
155. The method of claim 154 wherein the thick fourth spacer layer is a nitride.
156. The method of claim 155 wherein the conductive layer is a polycide.
157. The method of claim 156 wherein the metal is cobalt.
158. The method of claim 157 wherein the polycide is cobalt salicide (CoSi_2).
159. The method of claim 156 wherein the metal is nickel.
160. The method of claim 159 wherein the polycide is nickel salicide (NiSi).
161. The method of claim 156 wherein the metal is titanium.
162. The method of claim 161 wherein the polycide is titanium salicide (TiSi_2).



163. The gate electrode of claim 17 wherein the polycide is platinum salicide (PtSi).
164. The gate electrode of claim 17 wherein the polycide is tantalum salicide (TaSi).
165. The gate electrode of claim 26 wherein the polycide is platinum salicide (PtSi).
166. The gate electrode of claim 26 wherein the polycide is tantalum salicide (TaSi).
167. The gate electrode of claim 37 wherein the polycide is platinum salicide (PtSi).
168. The gate electrode of claim 37 wherein the polycide is tantalum salicide (TaSi).
169. The gate electrode of claim 48 wherein the polycide is platinum salicide (PtSi).
170. The gate electrode of claim 48 wherein the polycide is tantalum salicide (TaSi).
171. The method of claim 79 wherein the metal is platinum.
172. The method of claim 171 wherein the polycide is platinum salicide (PtSi).
173. The method of claim 79 wherein the metal is tantalum.
174. The method of claim 173 wherein the polycide is tantalum salicide (TaSi).
175. The method of claim 94 wherein the metal is platinum.
176. The method of claim 175 wherein the polycide is platinum salicide (PtSi).
177. The method of claim 94 wherein the metal is tantalum.
178. The method of claim 177 wherein the polycide is tantalum salicide (TaSi).
179. The method of claim 113 wherein the metal is platinum.
180. The method of claim 179 wherein the polycide is platinum salicide (PtSi).
181. The method of claim 113 wherein the metal is tantalum.
182. The method of claim 181 wherein the polycide is tantalum salicide (TaSi).
183. The method of claim 135 wherein the metal is platinum.



184. The method of claim 183 wherein the polycide is platinum salicide (PtSi).
185. The method of claim 135 wherein the metal is tantalum.
186. The method of claim 185 wherein the polycide is tantalum salicide (TaSi).
187. The method of claim 156 wherein the metal is platinum.
188. The method of claim 187 wherein the polycide is platinum salicide (PtSi).
189. The method of claim 156 wherein the metal is tantalum.
190. The method of claim 189 wherein the polycide is tantalum salicide (TaSi).