# CROSS-POINT DIODE ARRAYS AND METHODS OF MANUFACTURING CROSS-POINT DIODE ARRAYS

## TECHNICAL FIELD

**[0001]** The present technology is related to cross-point diode arrays and other types of structures used in memory devices or other types of microelectronic devices, and methods for manufacturing such structures.

## BACKGROUND

**[0002]** The microelectronic industry is under intense pressure to produce high performance devices in small package sizes at continually decreasing costs. Smart phones, portable computers, digital cameras, portable music and media players, and many other electronic products require faster memory devices with more capacity. As such, memory device manufacturers in particular seek reliable, low-cost processes for fabricating high-performance devices.

**[0003]** Memory devices may have large arrays of memory cells, and reducing the size of individual memory cells provides a concomitant increase in the bit density of the memory devices. Cross-point memory cells are located in the vertical overlap regions between word lines and bit lines. Cross-point memory cells include structures that undergo a stable and detectable change when exposed to a current between a word line and a corresponding bit line. Because cross-point memory cells are located in the overlap regions between bit lines and word lines, these memory cells may theoretically be formed to extremely small dimensions.

**[0004]** One concern of manufacturing cross-point memory cells is that the smallest features of the structures can be difficult to form using photolithography processes. For example, it is difficult to pattern the wafers to form the drain structures of a cross-point memory cell because these features are so small that they cannot be formed reliably using existing photolithography processes. It is also difficult to photo-pattern gate structures that completely surround the individual pillars in high density cross-point memory arrays. Moreover, it is very expensive to form very small features using photolithography processes

because these processes require expensive equipment and materials. Additional concerns of cross-point memory arrays include reversed leakage current, serial resistance, and accurate control of current-voltage uniformity that are important for multi-level cell configurations. Therefore, it is desired to develop improved methods for forming highly integrated circuitry, and in particular cross-point memory cells, and to develop improved circuitry for such features.

## BRIEF DESCRIPTION OF THE DRAWINGS

**[0005]** Figure 1 is flow chart of an embodiment of a method for forming an array of memory cells in accordance with the technology.

**[0006]** Figure 2A is a cross-sectional view and Figure 2B is a top-plan view of an embodiment of a substrate at a stage of a method for forming an array of memory cells in accordance with the technology.

**[0007]** Figure 3A is a cross-sectional view and Figure 3B is a top-plan view of an embodiment of a substrate at another stage of a method for forming an array of memory cells in accordance with the technology.

**[0008]** Figure 4A is a cross-sectional view and Figure 4B is a top-plan view of an embodiment of a substrate at another stage of a method for forming an array of memory cells in accordance with the technology.

**[0009]** Figure 5A is a cross-sectional view and Figure 5B is a top-plan view of an embodiment of a substrate at another stage of a method for forming an array of memory cells in accordance with the technology.

**[0010]** Figure 6A is a cross-sectional view and Figure 6B is a top-plan view of an embodiment of a substrate at another stage of a method for forming an array of memory cells in accordance with the technology.

**[0011]** Figure 7A is a cross-sectional view and Figure 7B is a top-plan view of an embodiment of a substrate at another stage of a method for forming an array of memory cells in accordance with the technology.

**[0012]** Figure 8A is a cross-sectional view and Figure 8B is a top-plan view of an embodiment of a substrate at another stage of a method for forming an array of memory cells in accordance with the technology.

[0013] Figures 9A and 9B are a cross-sectional views and Figure 9C is a top-plan view of an embodiment of a substrate at another stage of a method for forming an array of memory cells in accordance with the technology.

[0014] Figure 10 is a cross-sectional view of an embodiment of a substrate at another stage of a method for forming an array of memory cells in accordance with the technology.

[0015] Figure 11 is a cross-sectional view of an embodiment of a substrate at another stage of a method for forming an array of memory cells in accordance with the technology.

[0016] Figure 12 is a cross-sectional view of an embodiment of a substrate at another stage of a method for forming an array of memory cells in accordance with the technology.

[0017] Figure 13 is a cross-sectional view of an embodiment of a substrate at another stage of a method for forming an array of memory cells in accordance with the technology.

[0018] Figure 14 is a cross-sectional view of an embodiment of a substrate at another stage of a method for forming an array of memory cells in accordance with the technology.

[0019] Figure 15 is a cross-sectional view of an embodiment of a substrate at another stage of a method for forming an array of memory cells in accordance with the technology.

[0020] Figure 16 is a cross-sectional view of an embodiment of a substrate at another stage of a method for forming an array of memory cells in accordance with the technology.

[0021] Figure 17 is a cross-sectional view of an embodiment of a substrate at another stage of a method for forming an array of memory cells in accordance with the technology.

[0022] Figure 18 is a cross-sectional view of an embodiment of a substrate at another stage of a method for forming an array of memory cells in accordance with the technology.

[0023] Figure 19 is a cross-sectional view of an embodiment of a substrate at another stage of a method for forming an array of memory cells in accordance with the technology.

[0024] Figure 20 is a cross-sectional view of an embodiment of a substrate at another stage of a method for forming an array of memory cells in accordance with the technology.

[0025] Figure 21 is a cross-sectional view of an embodiment of a substrate at another stage of a method for forming an array of memory cells in accordance with the technology.

[0026] Figure 22 is a cross-sectional view of an embodiment of a substrate at another stage of a method for forming an array of memory cells in accordance with the technology.

[0027] Figure 23 is a flow chart of another embodiment of a method for forming vertical memory cells in accordance with the technology.

DETAILED DESCRIPTION

[0028] Specific details of several embodiments of the new technology are described below with reference to memory cell arrays and methods for manufacturing arrays of memory cells. Many embodiments, for example, are directed to cross-point memory arrays used in phase change memory or other types of memory. Memory cells and other semiconductor components are manufactured on and/or in semiconductor wafers that can include semiconductor substrates upon which and/or in which microelectronic devices, micromechanical devices, data storage elements, optics, read/write components, and other features can be fabricated. For example, SRAM, DRAM (e.g., DDR/SDRAM), flash memory (e.g., NAND flash-memory), phase change memory (PCRAM), processors, imagers, light emitting diodes (LEDs) and other types of devices can be constructed on semiconductor wafers. Although many of the embodiments are described below with respect to semiconductor devices that have integrated circuits, other types of devices manufactured on other types of substrates may be within the scope of the new technology. Moreover, several other embodiments of the new technology can have different configurations, components, or procedures than those described in this section. A person of ordinary skill in the art, therefore, will accordingly understand that the new technology may have other embodiments with additional elements, or the new technology may have other embodiments without several of the features shown and described below with reference to Figures 1-24.

[0029] Figure 1 is a flow chart of an embodiment of a method 100 of forming an array of memory cells in accordance with the technology. The method can include forming a plurality of pillars in an array of rows and columns (block 110). The pillars are formed from a substrate of a bulk semiconductor material, and individual pillars have a sacrificial cap structure. For example, individual pillars can have a semiconductor post formed of the bulk semiconductor material and the sacrificial cap structure can be on each of the semiconductor posts. The method further includes forming source regions between columns of the pillars (block 120), and forming conductive gate lines (block 130). Individual gate lines extend along a column of pillars and are spaced apart from corresponding source regions. Each gate line completely surrounds a portion of the semiconductor posts along a corresponding column of pillars. This embodiment of the method 100 further includes selectively removing

the sacrificial cap structure and thereby forming self-aligned openings that expose a top portion of corresponding semiconductor posts (block 140), and forming individual drain contacts in the self-aligned openings that are electrically connected to corresponding semiconductor posts (block 150).

**[0030]** Figures 2A and 2B are cross-sectional and top plan views, respectively, of an embodiment of a substrate 200 (e.g., a wafer) at a stage of the method 100. At this stage, the substrate 200 has a bulk semiconductor material 210 (Figure 2A), a plurality of shallow trench isolation (STI) structures 220, and a sacrificial structure 230 (Figure 2A). The STI structures 220 can have array trenches 222, peripheral trenches 224, a dielectric liner 226 lining the array and peripheral trenches 222 and 224, and an oxide 228 filling the array and peripheral trenches. The array trenches 222 define the spacing between rows of pillars that form individual memory cells or memory units.

**[0031]** The sacrificial structure 230 can include a first sacrificial material 232 and an optional second sacrificial material 234. The first sacrificial material 232 can be selectively removable relative to the second sacrificial material 234 using a suitable solvent or other material, and the first and second sacrificial material 232 and 234 can also provide separate stop-on features for mechanical removal processes. For example, the first sacrificial material 232 can be a polymeric material and the second sacrificial material 234 can be a nitride. The sacrificial structure 230 can be separated from the bulk semiconductor material 210 by a dielectric layer 236. In one specific embodiment, the dielectric layer 236 can be a silicon oxide layer having a thickness of approximately 50 angstroms, the first sacrificial material 232 can be a polymeric material having a thickness of about 800 angstroms, and the second sacrificial material 234 can be a nitride having a thickness of approximately 400 angstroms.

**[0032]** Figures 3A and 3B are cross-sectional and top plan views, respectively, of an embodiment of the substrate 200 at a subsequent stage of the method 100 in which column trenches 240 are formed. The column trenches 240 can be perpendicular or at an oblique angle relative to the oxide 228 in the array trenches 222. The column trenches 240 can be formed by photo-patterning a resist or other material (not shown) on top of the sacrificial structure 230 using photolithography or other techniques known in the art. The array trenches 222 can have a first width $W_1$ (Figure 3B), and the column trenches 240 have a second width $W_2$ greater than the first width $W_1$ of the array trenches 222. The column trenches 240 are formed by etching through the sacrificial structure 230 and into the

semiconductor material 210 to a desired trench depth. The etching process can be a dry etch or other method known in the art. In one embodiment, the target trench depth of the column trenches 240 is approximately equal to the depth of the array trenches 222 and peripheral trenches 224 of the STI structure 220.

**[0033]** The substrate 200 has an array of pillars 250 that provide vertical channels for forming individual memory cells. The oxide 228 in the array trenches 222 supports the pillars 250. Referring to Figure 3A, individual pillars 250 can include a semiconductor post 252 of the bulk semiconductor material 210 and a sacrificial cap 254 formed from the remaining portions of the first and second sacrificial material 232 and 234. The individual semiconductor posts 252 can each include a proximal portion 256a, an intermediate section 256b, and a distal portion 256c relative to the base of the bulk semiconductor material 210 at the bottom of the column trenches 240.

**[0034]** The array of pillars 250 can be arranged in a plurality of rows ($R_1$, $R_2$, etc.) and a plurality of columns ($C_1$, $C_2$, $C_3$, $C_4$, etc.). The rows of pillars 250 are spaced apart from each other by the first width $W_1$ of the array trenches 222, and the columns of pillars 250 are spaced apart from each other by the second width $W_2$ of the column trenches 240. As described in more detail below, the first width $W_1$ and second width $W_2$ are selected based upon the thickness of a conductive gate material such that the resulting conductive gate lines completely surround a portion of each of the pillars 250. The first width $W_1$, for example, can be less than 200% of the thickness of the conductive gate material, and the second width $W_2$ of the column trenches 240 can be greater than 200% of the thickness of the conductive gate material. In more specific embodiments, the second width $W_2$ can be about 300% greater than the thickness of the conductive gate material.

**[0035]** Figures 4A-6B illustrate embodiments of the substrate 200 at subsequent stages of the method 100. Figures 4A and 4B are cross-sectional and top plan views, respectively, after forming a first dielectric liner 257 and a second dielectric liner 258 along the sidewalls of the pillars 250. The first dielectric liner 257 can be formed by growing an oxide via oxidation, and the second dielectric liner 258 can be formed by growing or otherwise depositing a thin blocking spacer material. For example, the first dielectric liner 257 can be an oxide having a thickness of approximately 20 angstroms, and the second dielectric liner 258 can be a deposited TEOS having a thickness of approximately 50-100 angstroms. The first and second dielectric liners 257 and 258 are then spacer etched to remove the portions of

the liners on the top of the pillars 250 and in the bottom of the column trenches 240. The method can further include an activation procedure to re-crystallize the semiconductor material.

**[0036]** After spacer etching the first and second liners 257 and 258, source regions 260 are formed by implanting the desired implant species into the bulk semiconductor material 210 at the bottom of the column trenches 240. The source regions 260, for example, can be an N-type species. Figures 5A and 5B are cross-sectional and top plan views, respectively, of the substrate 200 at a subsequent stage in which a silicide 262 is formed at the source regions 260 by exposing the implanted material to a source, such as Ni, Co, or Ti, that selectively forms a metal silicide. During the silicide process, the sidewalls of the pillars 250 are protected by the second dielectric liner 258 and the second sacrificial material 234 of the cap structure 254. The un-reacted metal can be removed from the silicide 262 with a wet etch or other technique, and a thin nitride liner can be formed to cap the silicide 262

**[0037]** Figures 6A and 6B are cross-sectional and top plan views, respectively, of an embodiment of the substrate 200 at a later stage in which the column trenches 240 are filled with an oxide 248 and then planarized using a chemical-mechanical planarization process or other process that stops on the second sacrificial material 234 of the sacrificial cap 254. The oxide 248 that fills the column trenches 240 can be the same as the oxide 228 that fills the array trenches 222 of the STI structure 220. The thin nitride cap deposited on the silicide 262 protects the silicid 262 from subsequent gate oxidation.

**[0038]** Figures 7A-8B illustrate embodiments of additional stages of the method 100. Figures 7A and 7B are cross-sectional and top plan views, respectively, of the substrate 200 after removing the second sacrificial material 234 and a portion of the oxides 228 and 248. The second sacrificial material 234 can be selectively removed relative to the oxides 228 and 248 in a separate process, or the second sacrificial material 234 and the oxides 228 and 248 can be removed in the same process. The oxides 228 and 248 are accordingly recessed relative to the distal portion 256c of the semiconductor posts 252. In one embodiment, the thickness of the remaining portions of the oxides 228 and 248 is about 700 angstroms.

**[0039]** Figures 8A and 8B are cross-sectional and top plan views, respectively, illustrating the substrate 200 at a further stage in which more material is removed from the oxides 228 and 248 and the sidewalls of the pillars 250 are cleaned. The remaining portions of the oxides 228 and 248 provide a dielectric spacer between the source regions 260 and the

intermediate sections 256b of the semiconductor posts 252 where the metal gates will be formed. In one embodiment, the thickness of the remaining portions of the oxide 228 and 248 is about 200 angstroms. The exposed sidewalls of the semiconductor posts 252 provide a clean semiconductor surface for forming a gate dielectric 265. The gate dielectric 265 can be formed of conventional $SiO_2$, nitride hardened $SiO_2$, or other suitable materials. The portions of the gate dielectric 265 at the intermediate sections 256b of the posts 252 define the gate dielectric for the memory cells.

**[0040]** Figures 9A-9C illustrate embodiments of the substrate 200 at a metallization stage of the method 100. Figures 9A and 9B are cross-sectional views taken along lines 9A-9A and 9B-9B of Figure 9C. The method further includes depositing a conductive gate material 270 over the pillars 250 and into the recessed portions of the array trenches 222 (Figure 9B) and the column trenches 240 (Figure 9A). The gate material 270 has a thickness T (Figure 9A) such that the smaller first width $W_1$ of the array trenches 222 causes the gate material 270 to pinch off at intersections 271 (Figure 9C) over the portions of the oxide 228 between rows of pillars 250. The thickness T of the gate material 270, however, is not so thick that it spans the larger second width $W_2$ of the column trenches 240. The gate material 270 can be tantalum nitride or other suitable materials.

**[0041]** Figure 10 is a cross-sectional view illustrating embodiments of the substrate 200 at a stage of the method 100 in which gate lines 272 are formed from the gate material 270. The gate lines 272 are formed by spacer etching the gate material 270 (Figures 9A-9C) until the remaining portions of the gate material 270 are about at or near the intermediate sections 256b (Figure 5A) of the semiconductor posts 252. The spacer etch can selectively stop on the oxide 248 at the bottom of the column channels 240. However, because the gate material 270 completely filled the array tranches 222 between pillars 250, a portion of the gate material 270 remains in the bottom of the array trenches 222 between the pillars 250. Each metal gate line 272 accordingly completely surrounds the corresponding intermediate sections 256b of the posts 252 along a column of pillars 250. After forming the gate lines 272, an optional step includes implanting an n-type implant or other species into the distal portions 256c of the semiconductor posts using an angle implant (e.g., an n-type lightly doped drain).

**[0042]** Figure 11 is a cross-sectional view of embodiments of the substrate 200 at another stage of the method 100. At this stage dielectric spacers 274 are formed above the

gate lines 272, along the sidewalls of the pillars 250. The dielectric spacers 274 can be formed by depositing a dielectric material over the substrate and spacer etching the dielectric material to remove it from horizontal or other non-vertical surfaces. The dielectric spacers 274, for example, can be a nitride that is selectively etchable relative to the gate dielectric 265 and the oxide 248 in the bottom of the column channels 240.

**[0043]** Figure 12 is a cross-sectional view of embodiments of the substrate 200 at a subsequent stage that includes depositing an oxide 278 into the open portions of the array trenches 222 and the column trenches 240. The oxide 278 can be planarized to remove (a) an over burden of the oxide 278 and (b) the portions of the gate dielectric 265 on top of the remaining portions of the first sacrificial material 232. The planarization procedure accordingly exposes the remaining portions of the first sacrificial dielectric layer 232 without any additional photolithography procedures. As such, the exposed portions of the first sacrificial material 232 over the individual semiconductor posts 252 are "self-aligned" in that a separate photolithography process is not necessary to form a pattern corresponding to the exposed portions of the first sacrificial material 232.

**[0044]** Figure 13 is a cross-sectional view illustrating embodiments of subsequent stages in which the exposed portions of the first sacrificial material 232 are selectively etched relative to the oxide 278 to form self-aligned openings 280 directly over the distal portions 256c of corresponding semiconductor posts 252. The first sacrificial material 232 is formed from a material that is selectively removable relative to the oxide 278 and the dielectric spacer 274 such that the self-aligned openings 280 can be formed directly over the distal portions 256c of the semiconductor post 252 without having to align openings of a mask with the posts 252 (e.g., a mask photo-patterned on the wafer to have openings aligned with the posts). An n-type or other species can be implanted into the distal portions 256c of the semiconductor posts 252 to form drain regions 282. The drain regions 282 can accordingly be formed by directly implanting the implant species through the openings 280 at this stage of the process either in lieu of or in addition to forming the drain regions 282 earlier in the method using an angled implant process as described above with respect to in Figure 10.

**[0045]** Figure 14 is a cross-sectional view illustrating embodiments of an additional stage of the method 100 in which a plurality of drain contact plugs 284 are formed in the openings 280 (Figure 13). The drain contact plugs 284 can be formed by depositing a metal or other suitably conductive material into the openings 280 (Figure 13), and then removing

an overburden portion of the metal from the top of the oxide 278 using a chemical-mechanical planarization or other process. The drain contact plugs 284, for example, can be tungsten or other suitable metals. The drain contact plugs 284 are accordingly mask-less, self-aligned features that are aligned with the semiconductor posts 252. At this point, the structure of each pillar 250 defines a memory cell, and the array of memory cells is ready for cell integration into a PCRAM or other type of memory device.

**[0046]** Several embodiments of the method 100 and the resulting substrate 200 can be used to form very small cross-point memory cells. Some of the smallest features of a cross-point cell array are the gate lines and the contact plugs, and current photolithographic processes may not be able to efficiently form these features at the smallest sizes. The specific embodiment of the method 100 shown and described above, however, enables the gate lines and contact plugs to be formed without having to form a pattern of either the gate lines or the contact plugs using photolithography. This not only eliminates the process errors that can be induced by photolithographically patterning very small features, but is also reduces the utilization of expensive photolithography equipment. Therefore, several embodiments of the method 100 and substrate 200 provide a cost effective process for fabricating cross-point memory cells.

**[0047]** Several embodiments of the method 100 and the substrate 200 also provide a structure that can address other concerns of cross-point memory cells. For example, because the gate lines 272 surround the intermediate sections 256b of the semiconductor posts 252 along a column of pillars 250, the issues of reversed leakage current, serial resistance along a column of pillars 250, and current-voltage control are expected to be mitigated.

**[0048]** Figures 15-22 illustrate stages of another embodiment of the method 100. Figure 15 is a cross-sectional view that illustrates a stage immediately after the stages described above with respect to Figures 2A-9C. Figure 15, more specifically, illustrates a stage of another embodiment of the process 100 in which the gate material 270 has been spacer etched to selectively stop on the gate dielectric 265 and the oxide 248. The process illustrated in Figure 15 differs from that illustrated in Figure 10 in that the gate material 270 shown in Figure 15 is not etched to the same extent as it is in Figure 10. The stage illustrated in Figure 15 accordingly forms an intermediate structure 302 for forming gate lines that surround the individual pillars 250. In several embodiments, the gate lines 272 completely surround the individual pillars 250.

**[0049]** Figure 16 is a cross-sectional view illustrating embodiments at a later stage in which an oxide 308 is deposited into the open portions of the column trenches 240. At this stage an overburdened portion of the oxide 308 is removed using a chemical-mechanical planarizing procedure or other process that stops on the first sacrificial material 232. The removal procedure accordingly removes portions of the gate dielectric 265 from the top surface of the remaining portions of the first sacrificial material 232 in alignment with the individual pillars 250.

**[0050]** Figure 17 is a cross-sectional view illustrating subsequent stages in which the remaining portions of the first sacrificial material 232 are removed from the regions over the pillars 250 to form self-aligned openings 310 aligned with corresponding pillars 250. The first sacrificial material 232 can be selectively removed such that the remaining portions of the gate dielectric 265 remain intact. Figure 18 is a cross-sectional view that shows a subsequent stage in which the remaining portions of the gate dielectric 265 are removed to expose the distal portions 256c of the semiconductor posts 252. At this point a desired implant species can be implanted into the distal portions 256 of the semiconductor posts 252 to form drain regions 282.

**[0051]** Figure 19 is a cross-sectional view illustrating a subsequent stage that includes removing a portion of the intermediate structure 302 to form the individual gate lines 272 at the intermediate sections 256b of corresponding semiconductor posts 252. The gate lines 272 are formed such that they are spaced apart from both the drain regions 282 and the source regions 260. The gate lines 272 also surround the intermediate sections 256b of the semiconductor posts 252 along a corresponding column of the pillars 250 as described above with respect to Figure 10.

**[0052]** Figures 20-22 are cross-sectional views illustrating additional stages of this embodiment of the method. Figure 20 illustrates a stage in which a dielectric spacer 311 is deposited or otherwise formed in the substrate 200. The dielectric spacer 311 can be a nitride, and the thickness of the dielectric spacer 311 can be selected to fill the gaps where the gate metal was recessed to form the gate lines 272. Figure 21 illustrates spacer etching the dielectric spacer 311 to expose the drain regions 282. More specifically, the dielectric spacer 311 can be spacer etched to form dielectric spacers 314 above the gate lines 272 and along the sidewalls of the oxide 308. The drain regions 282 are accordingly exposed. Figure 22

illustrates the substrate 200 at a subsequent stage in which contact plugs 284 are formed in the openings over the drain regions 282.

**[0053]** Figure 23 is a flow chart of a method 400 for forming an array of vertical memory cells in accordance with another embodiment of the technology. In one embodiment, the method 400 includes forming a plurality of pillars (block 410) in which each pillar has a semiconductor post and a sacrificial cap. The pillars are arranged in rows spaced apart by a row spacing and columns spaced apart by a column spacing larger than the row spacing. The method 400 can further include forming source regions at a proximal region of the semiconductor posts (block 420) and forming conductive gate lines that completely surround an intermediate section of the semiconductor posts in a corresponding column of pillars (block 430). After forming the gate lines, the sacrificial caps can be removed selectively without forming a photo-pattern corresponding to a pattern of the sacrificial caps and thereby forming self-aligned openings over a distal portion of each of the semiconductor posts (block 440). The method 400 can also include forming drain contacts in the self-aligned openings that are electrically connected to corresponding semiconductor posts (block 450).

**[0054]** From the foregoing, it will be appreciated that specific embodiments of the invention have been described herein for purposes of illustration, but well-known structures and functions have not been shown or described in detail to avoid unnecessarily obscuring the description of the embodiments of the invention. Where the context permits, singular or plural terms may also include the plural or singular term, respectively. Moreover, unless the word "or" is expressly limited to mean only a single item exclusive from the other items in reference to a list of two or more items, then the use of "or" in such a list is to be interpreted as including (a) any single item in the list, (b) all of the items in the list, or (c) any combination of the items in the list. Additionally, the term "comprising" is used throughout to mean including at least the recited feature(s) such that any greater number of the same feature and/or additional types of features are not precluded Accordingly, the invention is not limited except as by the appended claims.

CLAIMS

I/We claim:

1. A method of forming an array of memory cells, comprising:

forming a plurality of pillars comprising fabricating a shallow trench isolation structure having array trenches and an oxide in the array trenches, forming a column trench mask, and etching column trenches in the semiconductor material that space apart the columns of the pillars, wherein individual pillars have a semiconductor post formed of a semiconductor material and a sacrificial cap on the semiconductor post;

forming source regions between columns of the pillars;

forming a plurality of gate lines, wherein individual gate lines extend along a corresponding column of pillars and are spaced apart from corresponding source regions, and wherein each gate line surrounds a portion of the semiconductor posts along a column of pillars;

selectively removing the sacrificial caps and thereby forming self-aligned openings that expose a top portion of corresponding semiconductor posts; and

forming individual drain contacts in the self-aligned openings that are electrically connected to corresponding semiconductor posts.

2. The method of claim 1 wherein forming the pillars comprises fabricating a shallow trench isolation structure having array trenches and an oxide in the array trenches and etching column trenches in the semiconductor material transverse to the array trenches.

3. The method of claim 1 wherein the array trenches have a first width and the column trenches have a second width greater than the first width.

4. The method of claim 1 wherein the sacrificial cap structure comprises a first sacrificial material and a second sacrificial material, wherein the first and second sacrificial materials are selectively removable relative to each other.

5. The method of claim 1 wherein the pillars are spaced apart from each other by array trenches between the pillars and column trenches.

6. The method of claim 5, wherein forming the gate lines comprises depositing a metal into the array trenches and the column trenches such that the metal completely surrounds at least an intermediate section of each of the posts, and wherein the metal deposited into the column trenches does not span the entire width of the column trenches.

7. The method of claim 6, further comprising spacer etching the metal, forming a dielectric spacer material over the metal gate structures and the pillars, spacer etching the dielectric spacer material, filling the column trenches with an oxide, removing a portion of the oxide to expose portions of the sacrificial caps, and wherein selectively removing the sacrificial caps comprises selectively etching the sacrificial caps relative to the oxide.

8. The method of claim 7 wherein the oxide is removed by chemical-mechanical planarization.

9. The method of claim 7, further comprising implanting a drain into a top portion of each semiconductor post before forming the drain contacts.

10. The method of claim 1, further comprising directly implanting a drain into a distal portion of each semiconductor posts through the self-aligned openings.

11. A method of forming an array of memory cells, comprising:

forming a plurality of pillars comprising fabricating a shallow trench isolation structure having array trenches and an oxide in the array trenches, forming a column trench mask, and etching column trenches in the semiconductor material that space apart the columns of the pillars, wherein individual pillars have a semiconductor post formed of a semiconductor material and a sacrificial cap on the semiconductor post;

forming source regions between columns of the pillars, wherein forming the source regions comprises implanting an N-type implant into the semiconductor material at a bottom of the column trenches;

forming a plurality of gate lines, wherein individual gate lines extend along a corresponding column of pillars and are spaced apart from corresponding source regions, wherein each gate line surrounds a portion of the semiconductor posts along a column of pillars, and wherein forming the gate lines comprises filling the column trenches with an oxide, etching the oxide in the array trenches and the column trenches to a depth spaced apart from the source regions, depositing a metal into the array trenches and the column trenches such that the metal fills the array trenches but does not fill the column trenches, and spacer etching the metal to a level spaced apart from the sacrificial caps;

selectively removing the sacrificial caps and thereby forming self-aligned openings that expose a top portion of corresponding semiconductor posts, wherein selectively removing the sacrificial caps comprises etching away the sacrificial caps without photo-patterning a mask with a pattern of openings corresponding to the pattern of the self-aligned openings; and

forming individual drain contacts in the self-aligned openings that are electrically connected to corresponding semiconductor posts.

12. A method of forming an array of vertical memory cells, comprising:

forming a plurality of pillars, wherein each pillar has a semiconductor post and a sacrificial cap, and wherein the pillars are arranged in rows spaced apart by a row spacing and columns spaced apart by a column spacing larger than the row spacing;

forming source regions at a proximal region of the semiconductor posts;

forming gate lines that surround an intermediate section of the semiconductor posts;

selectively removing the sacrificial caps comprising etching away the sacrificial caps without forming a mask corresponding to a pattern of the sacrificial caps, thereby forming self-aligned openings over a distal portion of each of the semiconductor posts; and

forming drain contacts in the self-aligned openings that are electrically connected to corresponding semiconductor posts.

13. The method of claim 12 wherein forming the pillars comprises fabricating a shallow trench isolation structure having array trenches and an oxide in the array trenches and etching column trenches in the semiconductor material transverse to the array trenches.

14. The method of claim 12 wherein forming the gate lines comprises depositing a metal having a thickness into the array trenches and the column trenches such that the metal fills the array trenches but does not fill the column trenches, and spacer etching the metal to a level spaced apart from the sacrificial caps.

15. The method of claim 14 wherein the array trenches have a first width less than twice the thickness of the metal and the column trenches have a second width greater than the first width.

16. The method of claim 12 wherein selectively removing the sacrificial cap comprises planarizing a first sacrificial material and then etching a second sacrificial material.

17. The method of claim 12 wherein the sacrificial caps comprise a first sacrificial material and a second sacrificial material, wherein the first and second sacrificial materials are selectively removable relative to each other.

18. The method of claim 14, further comprising spacer etching the metal, forming a dielectric spacer material over the metal gate structures and the pillars, spacer etching the dielectric spacer material, filling the column trenches with an oxide, removing a portion of the oxide to expose portions of the sacrificial cap structure, and wherein selectively removing the sacrificial caps comprises selectively etching the sacrificial caps relative to the oxide.

19. The method of claim 12, further comprising implanting a drain into a top portion of each semiconductor post before forming the drain contacts.

20. The method of claim 19, wherein the drains are angle implanted into the distal portions of the semiconductor posts before selectively removing the sacrificial caps.

21. The method of claim 19, wherein the drains are implanted through the self-aligned openings and into the semiconductor posts.