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(54) IMPROVEMENTS IN INFORMATION PROCESSING SYSTEMS

(71) We, HITACHI LIMITED of 5-1, 1-chome, Marunouchi, Chiyoda-ku, Tokyo, Japan, a body corporate organized according to the laws of Japan, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:–

The present invention relates to an information processing system with initialization means, such as an electronic desk top computer having means for automatically clearing a memory circuit.

An information processing system such as electronic desk top computer comprises a memory circuit which is constituted by a flip-flop circuit or the like. At the switching-on of power, the stored value in the flip-flop circuit is meaningless. Therefore, a computing operation must be carried out after the meaningless contents which have been stored in the memory circuit at the switching-on of power are cleared.

The present inventors have already proposed an approach for automatically clearing the stored contents of a memory circuit at the switching-on of power. In this approach, an output signal from a flip-flop circuit which comes to one stable condition or takes one stable value at the switching-on of power is applied directly to predetermined memory circuits as a clearing signal whereas the flip-flop circuit is inverted by a key input signal from a first depressed key to release the clearing signal so that the key input signal is suitably entered. By automatically effecting the generation of a clearing signal which was manually carried out in other prior art techniques and contructing the flip-flop circuit with insulated gate or metal-insulator-semiconductor field effect transistors (hereinafter referred to as MISFET), a clearing signal generating circuit is incorporated into a one-chip semiconductor integrated circuit for electronic desk top computer or the like.

However, the above-described clearing method in which a clearing signal is automatically or manually generated and this clearing signal is applied directly to memory circuits whose contents are to be cleared at the switching-on of power, has the drawback that it is necessary to provide special signal lines for applying the clearing signal, thus resulting in the complexity of wiring. For simplification of wiring, the present invention contemplates the utilization of programable logic array (hereinafter referred to as PLA) in an initialization process such as an automatic clearing operation in electronic desk top computer or the like.

According to the present invention there is provided an information processing system including: a programable logic array in which a microprogram for processing information is stored; an address register for designating the addresses of program information stored in said programable logic array; a plurality of storage devices coupled to said programable logic array and selectively receiving program information stored in said programable logic array; and means for setting the contents of said storage devices at prescribed values upon the turn-on of said system; characterized in that said means includes: first means for generating a first prescribed signal upon the turn-on of said system; second means, coupled to said first means and said address register, for coupling said first prescribed signal to a plurality of selected bit positions of said address register corresponding to a plurality of selected addresses of said programable logic array, and wherein said plurality of selected addresses of said programable logic array have been programmed to store said prescribed values for setting the contents of said storage devices; and third means, coupled to said address register, for selectively

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addressing individual ones of the bit positions of said address register, and thereby causing the contents of the individual ones of said selected addresses of said programmable logic array to be coupled to respective ones of said plurality of storage devices.

The present invention will now be described in greater detail by way of example with reference to the accompanying drawings, in which:

Fig. 1 is a circuit diagram showing an embodiment of the invention;

Fig. 2 is a circuit diagram for explaining an example in which an automatic clearing circuit is applied to an electronic desk top computer; and

Figs. 3, 4, 5, 6 and 7 show circuits for various parts shown in Fig. 1, respectively.

Prior to the detailed explanation of the invention, reference will be made to Fig. 2 showing an example in which an automatic clearing circuit is applied to an electronic desk top computer using a PLA and has already been proposed by the present inventors.

The PLA realizes the system control in a digital system with a simplified circuitry, thereby providing the reduction of cost due to the decrease in the number of parts used. The system control by PLA is also called microprogram control. In Fig. 2, address information designated by an address register 2 is applied to a fixed memory circuit 3 in which a microprogram is stored. An X register 4 is designated by an output of the fixed memory circuit 3, for example, an output R_2, and an AND gate AG_4 is thereby enabled to set information ADD from an adder into the X register 4. On the other hand, address information A_1 to A_8 for the next step (next address information) is applied to the address register 2 for subsequent operation. Such a digital system includes various memory circuits whose stored contents must be cleared after the switching-on of power and before a desired arithmetic operation. For example, there are X register 4, Y register 5, Z register (not shown), M register (not shown), conditional flip-flop 6 for storing a type of arithmetic calculation, and address register 2. The present inventors proposed to clear meaningless stored contents of these memory circuits by applying, at the switching-on of power, an output Q_{11} or clearing signal of a flip-flop circuit 1 in one stable condition to the memory circuits. The flip-flop 6 is reset by applying the clearing signal through an OR gate OG'_{10} to a set input R_{16} of the flip-flop 6, the stored contents of the X and Y registers 4 and 5 constructed by shift registers are cleared by applying the clearing signal to AND gates AG_1 and AG_3 of the respective feedback loops to cut off these loops, and the address register 2 constructed by flip-flops is applied with the clearing signal commonly to the respective digits. Thus, the initial values of the memory circuits are set.

The shown flip-flop circuit 1 comprising a depletion type load MISFET M_3 and an enhancement type load MISFET M_1 is rendered stable such that a drive MISFET M_2 first turns on since the gate voltage of the MISFET M_2 first reaches its threshold level at the switching-on of power. Alternatively, the operation similar to the above-described operation may be achieved by making the threshold voltage of the drive MISFET M_2 smaller than that of a MISFET M_4.

However, the above-described clearing method in accordance with which the clearing signal is automatically generated and directly applied to the memory circuits whose contents are to be cleared at the switching-on of power is disadvantageous in that signal lines for applying signals are necessary, thus resulting in the complexity of wiring.

These drawbacks are eliminated by an information processing system of the invention systematically controlled by a PLA, wherein the initialization of a predetermined memory circuit after the switching-on of power is made by setting the contents of the memory circuit to an initial value by means of a signal generated automatically or manually.

Fig. 1 is a circuit diagram showing an example of main parts of an embodiment of the invention which is applied to an automatic clearing operation of electronic desk top computer.

In the figure, reference number 1 designates an initial value setting signal generating flip-flop circuit which comprises MISFET's M_1, M_2, ... M_5. With the load MISFET's M_1 and M_3 constructed in enhancement and depletion types respectively, at the switching-on of power the drive MISFET M_2 always reaches its threshold gate voltage earlier than the drive MISFET M_4 cross-coupled with the MISFET M_2, so that the MISFET M_2 is first turned on thereby rendering the flip-flop circuit 1 stable. The MISFET M_5 is provided for resetting the flip-flop circuit 1, and this MISFET M_5 is turned on by a key input signal (K_1, K_2, ... K_n) first entered after the switching-on of power so that the output of the flip-flop circuit 1 is inverted. It should be appreciated that the initial value setting flip-flop circuit 1 is not limited to the illustrated example and may use any circuit which comes to its one stable condition at the switching-on of power. For example, a circuit as shown in Fig. 6 may be used.

Reference numeral 2 designates an address register which comprises latch circuits F_1, F_2, F_4, ... F_{128}. Each of the latch

circuits F_1, F_2, F_4, ... F_{128} is constructed by a MOS circuit shown in Fig. 5. The address register 2 designates an address of control information (or microprogram) stored in a fixed memory circuit 3. The fixed memory circuit 3 is constructed by a read-only memory (ROM) comprising MISFET's, as shown in Fig. 3. For example, symbols *a*, *b*, *c* and *d* in Fig. 1 correspond to MISFET's M_{R8}, M_{R19}, M_{R7} and M_{R18} in Fig. 3 respectively.

Latch circuits LT_1, LT_2, ... LT_{16} with construction similar to the latch circuits F_1, F_2, ... F_{128} are provided for temporarily storing the output information (R_1, R_2, μ_0, μ_1, ... μ_5, A_1, A_2, ... A_8) from the fixed memory circuit 3.

Reference numerals 4 and 5 designate respectively X and Y shift registers each of which comprises forty eight series-connected MOS circuits shown in Fig. 4. Numeral 6 designates a usual set-reset type flip-flop which may be constructed by a MOS circuit as shown in Fig. 7. Numeral 7 designates a gate circuit for forcibly setting a special digit of the address register 2 to a constant value in accordance with the output signal Q_{11} of the initial value setting signal generating flip-flop 1. The gate circuit 7 comprises OR gates OG_1, OG_2, ... OG_6.

In operation of the system shown in Fig. 1, the output Q_{11} or clearing signal of the flip-flop circuit 1 which comes to its one stable condition or takes one stable value at the switching-on of power is applied through the OR gates OG_1, OG_2, ... OG_6 of the gate circuit 7 to the digits F_4, F_{128} of the address register 2 except two lower digits F_1 and F_2. The respective initial values of six upper digits F_4, ... F_{128} of the address register 2 are thus fixed. When the digits F_4 ... F_{128} are held, for example, at "1", the address register 2 designates one of the addresses 252 to 255 since the values at which the two lower digits F_1 and F_2 become stable are not defined. Therefore, the contents of a predetermined memory circuit can be cleared by repeatedly designating the addresses 252 to 255 in which the programs are stored for clearing the predetermined memory circuits until the release of a clearing signal.

The clearing operation is carried out in the following manner. For example, when it is desired to clear all the stored contents of the Y register 5 to "O", the address register 2 designates the address 252 whose information in turn is entered into the fixed memory circuit or ROM 3. The output R_1 of the fixed memory circuit 3 is applied to the AND gate AG_1 forming a feedback loop of the Y register 5, thereby cutting off the feedback loop. Similarly, for the clearing of the flip-flop 6, the address register 2 designates the address to derive the output μ_0 from the fixed memory circuit 3 which output in turn is applied to the reset input R_{16} of the flip-flop 6.

With respect to the X register 4 whose output is supplied to display means, when it is desired to display numeral "O" at the lowest digit and to display no numeral at or enter a zero suppression code (for example, 12) to the other digits, the address register 2 designates the address 254 to derive the output signal R_2 from the fixed memory circuit 3 for enabling the AND gate AG_4, while a control signal is applied to an adder (not shown) which in turn forms a zero suppression code (for example, 12). The information from the adder is applied through the AND gate AG_4 to all digits except the lowest digit to set the zero suppression code information therein, and the "O" information from the adder is entered to the lowest digit. Similarly, the other register such as Z register (not shown) may be cleared by means of the address 255.

Operation of the repeated designation of the addresses 252 to 255 is accomplished by a program loop. The program loop comprises the address lines W252 to W255; the first group of coupling elements a,b,c,d ... which are coupled between the address lines and the true outputs of the flip-flops F_4 and F_{128} except for the flip-flops F_1 and F_2; the second group of the coupling elements selectively coupled between the address lines and true or inverse outputs of the flip-flops F_1 and F_2; the third group of the coupling elements selectively coupled between the address lines and the control output lines A1 to A8; and the feedback connections for coupling the flip-flops LT_9 to LT_{16} with the flip-flops F_1 to F_{128}.

In such a program loop, when the digit flip-flops F_4 to F_{128} are held at "1" by the circuit 1, all of the outputs thereof become "1". These outputs will not select any one of the address lines W252 to W255 because the coupling elements (a,b,c,d, ...) of the first group receiving the true outputs of the flip-flops F_4 to F_{128} which are coupled to each of the address lines W252 to W255 with the same pattern of the coupling. In contrast with the flip-flops F_4 to F_{128} controlled by the circuit 1, the flip-flops F_1 and F_2 connected to only the feedback connections will select any one of the address lines W252 to W255 because of the different coupling pattern of coupling elements in each address line.

Assuming that in a first period the outputs of the flip-flops F_1 and F_2 are "1" and "O", respectively, and that the flip-flops F_4 to F_{128} are held at "1" by the circuit 1, the address line W253 is selected in accordance with the position of the coupling elements in the second group so that the control output lines A1 and A2 are respectively applied with "O" and "1" in accordance with the position of the coupling elements in the third

group. In a second period succeeding the first period, the output signals "O" and "1" are applied to the flip-flops A1 and A2, respectively, through the flip-flops LT_{16} and LT_{15} and the feedback connections, so as to select the next address line W254. Similarly, in a third period, the address line W255 is selected in response to the output signals of the output control lines A1 and A2 corresponding to the address line W254 selected in the preceding period. Thus, in so far as the flip-flops F_4 to T_{128} are held at "1" by the circuit 1, the address lines W252 to W255 are selected in that order, and such a selection is repeated.

The address next to the address 255 or the next address (output information of A_1, A_2, ... A_8), as shown in a matrix form of ROM's in the block 3 of Fig. 1, indicates the address O which is an actual process starting address in the information processing system. However, in the case where the program step of the address 255 is designated, the output of the initial value setting signal generating flip-flop circuit 1 forcibly fixes the contents of the address register 2 to the address 252 through the gate circuit 7 as long as that output is in the level of "1". Thus, the program steps of the initial value setting microprogram are again and successively carried out for the addresses 252, 253, 254 and 255 to repeat the setting of the respective memory circuits to their initial values.

Next, when a key input signal from a key which is first depressed is applied to the reset input R_{11} of the flip-flop circuit 1 through the OR gate OG_7, the flip-flop circuit 1 is inverted so that the clearing signal is released. With the clearing signal released, address information designating the fixed memory circuit 3 is entered to the address register 2. As a result, the program loop for the clearing operation is released from the address 255 and a jump takes place to a program address, i.e. address O for a predetermined system control in accordance with the next address information or output information (A_1, A_2, ... A_8).

As described in the foregoing, the invention utilizes the clearing operation for system control based on PLA, instead of the direct application of a clearing signal to memory circuits. Therefore, any special signal line for supplying to each memory circuit can be omitted and simplification of wiring can be achieved. Further, since the initialization of the memory circuit is carried out by the microprogram, the initial value can be easily and arbitrarily modified by merely changing the pattern of microprogram storing ROM's in accordance with the user's requirements.

It should be appreciated that the invention is not limited to the above-described embodiment and may include various modifications. For example, in the case where a clearing signal is generated in a manual manner, a predetermined digit of the address register may be fixed on the basis of a signal obtained by the depression of a clearing key. In the case where a clearing signal is generated in an automatic manner, any suitable circuit may be used for generating a clearing signal. The number and address of program steps for clearing memory circuits may arbitrarily determined depending upon the system. In addition to an automatic clearing operation, a method of setting an initial value as required in the system, as in the case of setting the initial value of the X register, may be employed.

The invention is widely applicable to the initial value setting manner in information processing systems such as electronic desk top computers controlled systematically by PLA.

WHAT WE CLAIM IS:–

1. An information processing system including: a programmable logic array in which a microprogram for processing information is stored; an address register for designating the addresses of program information stored in said programmable logic array; a plurality of storage devices coupled to said programable logic array and selectively receiving program information stored in said programmable logic array; and means for setting the contents of said storage devices at prescribed values upon the turn-on of said system; characterized in that said means includes: first means for generating a first prescribed signal upon the turn-on of said system; second means, coupled to said first means and said address register, for coupling said first prescribed signal to a plurality of selected bit positions of said address register corresponding to a plurality of selected addresses of said programmable logic array, and wherein said plurality of selected addresses of said programmable logic array have been programmed to store said prescribed values for setting the contents of said storage devices; and third means, coupled to said address register, for selectively addressing individual ones of the bit positions of said address register, and thereby causing the contents of the individual ones of said selected addresses of said programmable logic array to be coupled to respective ones of said plurality of storage devices.

2. An information processing system according to claim 1, wherein the programmable logic array includes: a plurality of control output lines for supplying control signals to said storage devices thereover; a plurality of address lines to which address signal for designating the addresses of matrix positions in said array are applied; and a

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group. In a second period succeeding the first period, the output signals "O" and "1" are applied to the flip-flops A1 and A2, respectively, through the flip-flops LT_{16} and LT_{15} and the feedback connections, so as to select the next address line W254. Similarly, in a third period, the address line W255 is selected in response to the output signals of the output control lines A1 and A2 corresponding to the address line W254 selected in the preceding period. Thus, in so far as the flip-flops F_4 to T_{128} are held at "1" by the circuit 1, the address lines W252 to W255 are selected in that order, and such a selection is repeated.

The address next to the address 255 or the next address (output information of A_1, A_2, ... A_8), as shown in a matrix form of ROM's in the block 3 of Fig. 1, indicates the address O which is an actual process starting address in the information processing system. However, in the case where the program step of the address 255 is designated, the output of the initial value setting signal generating flip-flop circuit 1 forcibly fixes the contents of the address register 2 to the address 252 through the gate circuit 7 as long as that output is in the level of "1". Thus, the program steps of the initial value setting microprogram are again and successively carried out for the addresses 252, 253, 254 and 255 to repeat the setting of the respective memory circuits to their initial values.

Next, when a key input signal from a key which is first depressed is applied to the reset input R_{11} of the flip-flop circuit 1 through the OR gate OG_7, the flip-flop circuit 1 is inverted so that the clearing signal is released. With the clearing signal released, address information designating the fixed memory circuit 3 is entered to the address register 2. As a result, the program loop for the clearing operation is released from the address 255 and a jump takes place to a program address, i.e. address O for a predetermined system control in accordance with the next address information or output information (A_1, A_2, ... A_8).

As described in the foregoing, the invention utilizes the clearing operation for system control based on PLA, instead of the direct application of a clearing signal to memory circuits. Therefore, any special signal line for supplying to each memory circuit can be omitted and simplification of wiring can be achieved. Further, since the initialization of the memory circuit is carried out by the microprogram, the initial value can be easily and arbitrarily modified by merely changing the pattern of microprogram storing ROM's in accordance with the user's requirements.

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1. An information processing system including: a programmable logic array in which a microprogram for processing information is stored; an address register for designating the addresses of program information stored in said programmable logic array; a plurality of storage devices coupled to said programable logic array and selectively receiving program information stored in said programmable logic array; and means for setting the contents of said storage devices at prescribed values upon the turn-on of said system; characterized in that said means includes: first means for generating a first prescribed signal upon the turn-on of said system; second means, coupled to said first means and said address register, for coupling said first prescribed signal to a plurality of selected bit positions of said address register corresponding to a plurality of selected addresses of said programmable logic array, and wherein said plurality of selected addresses of said programmable logic array have been programmed to store said prescribed values for setting the contents of said storage devices; and third means, coupled to said address register, for selectively addressing individual ones of the bit positions of said address register, and thereby causing the contents of the individual ones of said selected addresses of said programmable logic array to be coupled to respective ones of said plurality of storage devices.

2. An information processing system according to claim 1, wherein the programmable logic array includes: a plurality of control output lines for supplying control signals to said storage devices thereover; a plurality of address lines to which address signal for designating the addresses of matrix positions in said array are applied; and a

matrix of coupling elements selectively connected to said address lines and said control output lines and providing prescribed control signals on selected control output lines in response to the receipt of address signals on selected address lines.

3. An information processing system according to claim 2, wherein the programmable logic array further includes a program loop for providing the address of any one or of several of the program steps of the microprogram setting the prescribed values or initial states of the storage devices.

4. An information processing system according to any one of the preceding claims wherein the first means comprises a flip-flop which is held in one of its stable states upon the turn-on of said system.

5. An information processing system according to claim 4, wherein the flip-flop is set into the other of its stable states by the input signal first brought about after the turn-off said system.

6. An information processing system according to any one of the preceding claims 1 to 4, wherein the programmable logic array includes a read-only memory.

7. An information processing system constructed and arranged to operate substantially as herein described with reference to Fig. 1 and Figs. 3 to 7 of the accompanying drawings.

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The following amendments were allowed under Section 29 on 24 September 1979:

Page 5, *delete* line 23 *insert* turn-on of said system.

THE PATENT OFFICE
16 October 1979

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