CLAIMS

1. A manufacturing method of a semiconductor structure, comprising:

providing a substrate;

forming a plurality of laminated structures arranged at intervals on the substrate, wherein each of the laminated structures comprises a first conductive layer, an insulating layer, and a second conductive layer that are stacked sequentially, and at least one of the first conductive layer and the second conductive layer is a bismuth layer;

forming a channel layer covering the laminated structures, and a dielectric layer covering the channel layer; and

forming word lines (WLs) extending along a first direction, wherein the WL comprises a plurality of contact parts and a connecting part connecting adjacent contact parts, the contact part surrounds and is in contact with a side surface of the dielectric layer, and the contact part is opposite to at least a part of the insulating layer.

2. The manufacturing method of a semiconductor structure according to claim 1, wherein a material of the channel layer comprises molybdenum sulfide.

3. The manufacturing method of a semiconductor structure according to claim 1, wherein the forming a channel layer covering the laminated structures, and a dielectric layer covering the channel layer comprises:

depositing the channel layer on the laminated structures and the substrate, wherein the channel layer covers top surfaces and side surfaces of the laminated structures, and a top surface of the substrate; and

depositing the dielectric layer on the channel layer.

4. The manufacturing method of a semiconductor structure according to claim 3, before the forming WLs extending along a first direction, wherein the WL comprises a plurality of contact parts and a connecting part connecting adjacent contact parts, the contact part surrounds and is in contact with a side surface of the dielectric layer, and the contact part is opposite to at least a part of the insulating layer, the manufacturing method further comprises:

filling a first support layer between the laminated structures covered by the channel layer and the dielectric layer, wherein a surface of the first support layer away from the substrate is higher than that of the first conductive layer away from the substrate, and is lower than a surface of the insulating layer away from the substrate.

5. The manufacturing method of a semiconductor structure according to claim 4, wherein the filling a first support layer between the laminated structures covered by the channel layer and the dielectric layer, wherein a surface of the first support layer away from the substrate is higher than that of the first conductive layer away from the substrate, and is lower than a surface of the insulating layer away from the substrate comprises:

forming a first initial support layer on the dielectric layer, wherein the first initial support layer is filled between the laminated structures covered by the channel layer and the dielectric layer, and the first initial support layer covers a top surface of the dielectric layer; and

removing a part of the first initial support layer, and taking the retained first initial support layer as the first support layer.

6. The manufacturing method of a semiconductor structure according to claim 4, wherein the forming WLs extending along a first direction, wherein the WL comprises a plurality of contact parts and a connecting part connecting adjacent contact parts, the contact part surrounds and is in contact with a side surface of the dielectric layer, and the contact part is

opposite to at least a part of the insulating layer comprises:

forming an initial WL layer covering the first support layer and the dielectric layer;

removing a part of the initial WL layer located on the first support layer along the first direction, such that the initial WL layer is divided, to form a plurality of intermediate WL layers arranged at intervals; and

removing the intermediate WL layer on a top surface of the dielectric layer, and a part of the intermediate WL layer away from the substrate on the side surface of the dielectric layer, and taking the retained intermediate WL layers as the WLs.

7. The manufacturing method of a semiconductor structure according to claim 6, wherein the removing a part of the initial WL layer located on the first support layer along the first direction, such that the initial WL layer is divided, to form a plurality of intermediate WL layers arranged at intervals comprises:

forming a mask layer covering the initial WL layer, wherein the mask layer is filled between the laminated structures covered by the channel layer, the dielectric layer, and the initial WL layer, and the mask layer covers a top surface of the initial WL layer;

forming a first photoresist layer on the mask layer, wherein the first photoresist layer is provided with a trench extending along the first direction, and orthographic projection of the trench on the substrate and that of the initial WL layer on the side surface of the laminated structure on the substrate do not overlap;

etching the mask layer by the first photoresist layer as a mask; and

etching the initial WL layer by the etched mask layer as a mask, to form the intermediate WL layers.

8. The manufacturing method of a semiconductor structure according to claim 4, after the forming WLs extending along a first direction, wherein the WL comprises a plurality of

contact parts and a connecting part connecting adjacent contact parts, the contact part surrounds and is in contact with a side surface of the dielectric layer, and the contact part is opposite to at least a part of the insulating layer, the manufacturing method further comprises:

forming a second support layer covering the WLs, the first support layer, and the dielectric layer, wherein a surface of the second support layer away from the substrate is flat;

forming a second photoresist layer on the second support layer, wherein the second photoresist layer is provided with a plurality of openings, and the openings are directly opposite to the laminated structures;

etching the second support layer, the dielectric layer, and the channel layer by the second photoresist layer as a mask, to form a contact hole, wherein the contact hole exposes the second conductive layer; and

forming a third conductive layer in the contact hole, wherein the third conductive layer is electrically connected to the second conductive layer.

9. The manufacturing method of a semiconductor structure according to claim 8, wherein an area of an opening of the contact hole is greater than that of a bottom of the contact hole.

10. The manufacturing method of a semiconductor structure according to claim 9, wherein a plane perpendicular to the substrate is used as a cross section, a shape of a cross section of the contact hole comprises a rectangle and a trapezoid that are connected to each other, the rectangle is disposed at one side of the trapezoid close to the substrate, and a bottom edge of the rectangle coincides with an upper bottom of the trapezoid.

11. The manufacturing method of a semiconductor structure according to claim 1, wherein a plurality of bit lines (BLs) are arranged at intervals in the substrate, and the BLs extend along a second direction; and

at least one of the laminated structures is disposed on each of the BLs along the second direction, and the first conductive layer is electrically connected to the BLs.

12. The manufacturing method of a semiconductor structure according to claim 11, wherein a shallow trench isolation (STI) structure is also disposed in the substrate, and the STI structure is disposed between adjacent BLs.

13. A semiconductor structure, comprising: laminated structures, a channel layer covering side surfaces of the laminated structures, and a dielectric layer covering a side surface of the channel layer, and a gate annularly provided on the dielectric layer; wherein

each of the laminated structures comprises a first conductive layer, an insulating layer, and a second conductive layer that are stacked sequentially, one of the first conductive layer and the second conductive layer is a source, the other of the first conductive layer and the second conductive layer is a drain, and at least one of the source and the drain is a bismuth layer.

14. The semiconductor structure according to claim 13, wherein a material of the channel layer comprises molybdenum sulfide.

15. The semiconductor structure according to claim 13, wherein the semiconductor structure further comprises WLs and BLs; and

the BLs are disposed in the substrate, the laminated structures are disposed on the substrate, one of the source and the drain is electrically connected to the BL, the WL comprises gates and a connecting part connecting two adjacent gates.