

ABSTRACT

An integrated circuit semiconductor device includes a nanosheet extending above a substrate in a first horizontal direction, a gate electrode extending in a second horizontal direction while surrounding the nanosheet with a gate insulating layer therebetween, a first source/drain region on a side of the nanosheet, and a second source/drain region on another side of the nanosheet, wherein the first source/drain region includes first silicide layers provided inward from surfaces of the nanosheet, first metal layers surrounding the nanosheet from upper and lower sides of the first silicide layers, and a first nanosheet region provided between the first silicide layers, wherein the second source/drain region includes second silicide layers formed inward from the surfaces of the nanosheet, second metal layers surrounding the nanosheet from upper and lower sides of the second silicide layers, and a second nanosheet region provided between the second silicide layers.

FIG. 1