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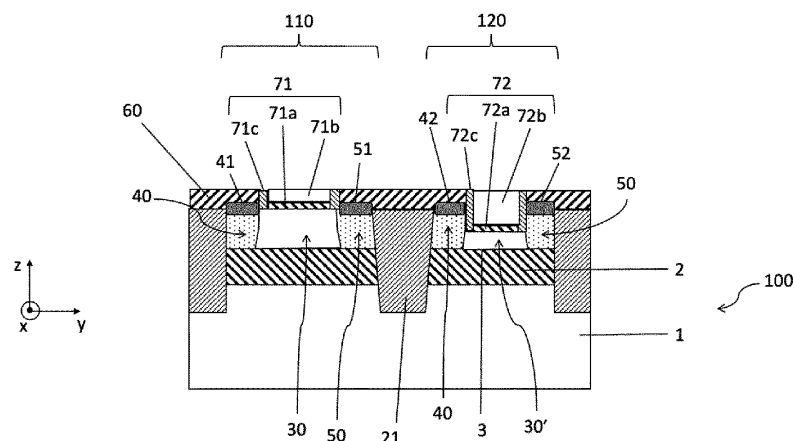
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(54) Title: METHOD FOR MANUFACTURING A SeOI INTEGRATED CIRCUIT CHIP

[Fig. 5c]



(57) Abstract: The invention relates to a method for manufacturing a semiconductor-on-insulator (SeOI) integrated circuit chip comprising the following steps: a) providing a semiconductor-on-insulator structure having a buried insulating layer which is sandwiched between a support substrate and a top semiconductor-containing layer, said top layer having a first thickness throughout the SeOI structure, b) building a plurality of field effect transistors (FET), wherein each FET is isolated from the others and comprises: - a preliminary gate above a channel region of the top layer, the FETs from a first group having a first preliminary gate length and the FETs from a second group having a second preliminary gate length smaller than the first one, - a source region and a drain region formed by n-type or p-type dopant implantation in the top layer, and extending down to the buried insulating layer, - a source electrode and a drain electrode respectively on the source region and the drain region, c) removing at least the preliminary gates of the FETs from the second group, leaving access to the channel regions of said FETs, d) thinning the top layer in channel regions of the FETs from the second group, so as to reach a second thickness, wherein the top layer in channel regions of a first group of FET has the first thickness, e) forming functional gates simultaneously on channel regions of the FETs whose preliminary gate was removed.

[Continued on next page]

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