METHOD OF FORMING A HIGH K METALLIC DIELECTRIC LAYER

BACKGROUND OF THE INVENTION

(1) Field of the Invention

The present invention relates to methods used to fabricate metal - insulator - metal capacitor structures for semiconductor integrated circuits, and more specifically to a method used to form a high dielectric constant, (high k), metallic oxide layer, for use as a dielectric layer for a capacitor structure.

(2) Description of Prior Art

Metal - Oxide - Metal, (MOM), capacitor structures are commonly used in current analog/RF circuits. The use of an insulator layer, with a high dielectric constant, (high K), would be useful in terms of providing efficient charging for the analog devices. Therefore capacitor dielectric layers, such as silicon nitride, with a dielectric constant of about 7, has been used in place of silicon oxide dielectric layers, featuring a dielectric constant of only about 3.9. For enhanced capacitor performance, metal oxide layers, with dielectric constants even larger than silicon nitride values, are now being considered for use in MOM structures. However to form reliable, (in terms of breakdown strength), metal oxide layers, such as tantalum pentoxide, (Ta_2O_5), or aluminum oxide, (Al_2O_3), temperatures greater than 400^0 C, are needed. These elevated

temperatures however, can result in degradation to existing interconnect structures, comprised of aluminum based metallurgies. The exposure of these aluminum based structures, to temperatures needed to form the metal oxide layer, can result in pre-melting, or reflowing of these structures.

This invention will describe processes used to form reliable, dense, metal oxide layers, for MOM structures, still however avoiding the exposure of the surrounding interconnect structures, metal structures other than MOM structures, to elevated temperatures. A first iteration will describe local heating of an area of a metal layer, in an oxidizing environment, accomplished via local laser ablation. The laser ablation process results in only surface heating of an underlying metal layer, allowing the desired region of metal to be oxidized, forming the desired metal oxide layer at temperatures greater than temperatures experienced by surrounding metal structures. A second iteration will describe the localized formation of the metal oxide layer, in an oxidizing environment, using energy supplied by either UV or I line exposures. Conventional photolithographic plates are used to allow specific regions of an underlying metal layer to experience the UV or I line exposure. Prior art such as Kang in U.S. Pat. No. 5,834,357, as well as Sun et al, in U.S. Pat. No. 5,930,584, describe processes used to fabricate high K dielectric layers, however these prior arts do not feature the unique processes used in this invention to achieve metal oxide layers, without exposure of surrounding metal structures to the high oxidation temperatures, used to form reliable, dense metal oxide layers, on local regions of a metal layer.

SUMMARY OF THE INVENTION

It is an object of this invention to form a high K dielectric layer, for a metal - oxide - metal, (MOM), capacitor structure, via oxidation procedures, which allows the oxidizing region to experience a higher temperature than the surrounding metal interconnect structures.

It is another object of this invention to form a high K dielectric layer, via a laser ablation procedure, performed to localized regions of an underlying metal layer, in an oxidizing ambient.

It is still another object of this invention to form a high K dielectric layer via exposure of localized regions of an underlying metal layer, to UV or I line energies, in the presence of an oxidizing environment.

In accordance with the present invention a method of fabricating a metal - oxide - metal, (MOM), capacitor structure, featuring a high K dielectric layer, formed from localized heating of an underlying metal layer, is described. A first iteration of the invention initiates with the deposition of an underlying metal layer, for subsequent use as the bottom electrode for the MOM capacitor structure, followed by a laser ablation procedure, resulting in the formation of the desired high K, metal oxide component of the MOM capacitor structure. The laser ablation procedure, performed in an oxidizing environment, allows the laser ablated surface of the underlying metal layer to reach a temperature needed for formation of a dense, metal oxide region, while surrounding metal structures, or metal structures used for non- MOM purposes, do not experience the temperature increase. A second iteration of this invention features the

subjection of localized regions of the underlying metal layer, to either UV or I line exposures. A photolithographic plate is used to allow only selective regions of the underlying metal layer to be subjected to the UV or I line exposures, performed in an oxidizing environment, thus resulting in the formation of the desired metal oxide component of the MOM capacitor structure, on an underlying metal electrode structure.

BRIEF DESCRIPTION OF THE DRAWINGS

The object and other advantages of this invention are best described in the preferred embodiment with reference to the attached drawings that include:

Figs. 1 - 8, which schematically, in cross-sectional style, describe key stages of fabrication used to form a high K dielectric layer, for a MOM capacitor structure.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The methods used to form a high K dielectric layer for a metal - oxide - metal, (MOM), capacitor structure, featuring the use of laser ablation, UV or I line exposure procedures, performed to an underlying metal electrode component of the MOM capacitor structure, in an oxidizing environment, will now be described in detail. An interlevel dielectric, (ILD), layer 1, comprised of either silicon oxide, undoped silica glass, (USG), fluorinated silica glass, (FSG), or borophosphosilicate glass, is shown schematically in Fig. 1. Metal plug structures 2, comprised of a metal chosen from a group containing tungsten, copper, or aluminum, are formed in via

holes 20. Via holes 20, can expose underlying metal interconnect structures, or via holes 20, can be dummy openings, terminating at the top surface of an underlying insulator layer. A metal layer 3, comprised of either aluminum, tantalum, or copper, shown schematically in Fig. 2, is next deposited via plasma vapor deposition, (PVD), procedures, to a thickness between about 3000 to 5000 Angstroms.

The first iteration of this invention is next detailed and described schematically in Figs. 3 - 4. An in situ, laser procedure is performed to local regions of metal layer 3, in an environment comprised of either NO, N_2O, O_2, or O_3. The laser ablation procedure results in local heating of metal layer 3, confined to a region near the top surface of metal layer 3. The localized heating, created by the laser spot, results in melting of metal layer 3, confined at the top surface, and in the presence of an oxidizing ambient, forms metallic dielectric layer 4, consuming a portion of the of metal layer 3. The laser ablation procedure is performed using excimer or YAG laser, at a power between about 0.1 to 10 watts. The temperature reached, at the surface of metal layer 3, during the laser ablation procedure is between about 1000 to 2000^o C, while the surrounding device regions are not influenced by the surface heating laser ablation procedure, and therefore remain at temperatures below 400^o C. Metallic dielectric layer, or high K layer 4, is comprised of either Ta_2O_5, Al_2O_3, or CuO_2, at a thickness between about 200 to 400 Angstroms, and with a dielectric constant between about 22 to 35. The thickness of metal layer 3, after formation of high K layer 4, is now decreased to between about 2500 to 4500 Angstroms. This is schematically shown in Fig. 3. An overlying metal layer 5, again comprised

of either aluminum, tantalum or copper, is next deposited via PVD procedures, to a thickness between about 3000 to 5000 Angstroms. This is schematically shown in Fig. 4. Conventional photolithographic and RIE procedures, using Cl_2 or SF_6, as an etchant for the metal layers, while either BF_3, or CF_4/CHF_3 is used as an etchant for the high K layer, are employed to define metal - oxide - metal, capacitor structure 6, schematically shown in Fig. 4.

A second iteration of this invention, featuring formation of the desired high K layer, via use of UV or I line exposure, in an oxidizing ambient, is next addresses, and schematically described in Figs. 5 - 8. Fig. 5, shows metal plug structures 2a, and metal plug structure 2b, in via holes 20, where via holes 20, were formed in interlevel dielectric layer 1. Metal layer 13, chosen from a group that includes titanium, tantalum, aluminum, or copper, is deposited via PVD procedures, to a thickness between about 2500 to 4500 Angstroms. A photolithographic plate 15, comprised of quartz, with a chromium pattern 16, is then situated, overlying metal layer 13. Opening 24, or the non- chromium, clear region of photolithographic plate 15, will subsequently define the region of metal layer 13, to be converted to the desired high K layer. This is schematically shown in Fig. 5.

Exposure of metal layer 13, to a UV or to a I line, exposure conditions, in an ambient comprised of either O_2 or O_3, create high K layer 18, in regions of metal layer 13, directly underlying opening 24, in photolithographic plate 15. The oxygen or ozone, flowing in space 7, in combination with the energy supplied by the UV or I line exposure, are sufficient to oxidize a top portion of exposed metal layer 13. This is accomplished using a UV exposure at an energy

between about 1 to 100 millijoules, while the exposure energy for the I line procedure is also between about 1 to 100 millijoules. The oxygen or ozone flow, in the space located between the photolithographic plate and the substrate, is maintained between about 10 to 1000 sccm. The temperature reached at the top surface of exposed metal layer 13, is between about 250 to 1000^{o} C, forming high K layer 18, at a thickness between about 200 to 300 Angstroms, and reducing the thickness of the portion of metal layer 13, located underlying high K layer 18, to between about 2000 to 4000 Angstroms. The dielectric constant of high K layer 18, comprised of either TiO_2, Al_2O_3, Ta_2O_5, or CuO_2, is between about 22 to 35. The result of selectively forming high K layer 18, in only a portion of metal layer 13, is schematically shown in Fig. 6. Again, as was the case for the first iteration of this invention, the localized exposure of only a portion of the top surface of a metal layer, restricts the increase in temperature to only the exposed area, maintaining lower temperatures for the bulk of the device.

An overlying metal layer 19, comprised of either titanium, tantalum, aluminum, or copper, is next deposited, via PVD procedures, to a thickness between about 2500 to 4500 Angstroms, overlying high K layer 18, and metal layer 13. Photoresist shapes 30, shown schematically in Fig. 7, are then formed on the regions of metal layer 19, for purposes of defining the metal - oxide - metal, capacitor structure, as well as defining a metal interconnect structure. Anisotropic RIE procedures, using Cl_2 or SF_6 as an etchant for metal layer 19, and for metal layer 13, and using either BF_3, or CF_4/CHF_3 as an etchant for high K layer 18, are used to create capacitor structure 31, comprised of metal layer 19, high K layer 18, and metal layer 13, overlying, and contacting metal plug structures 2a. This is schematically shown in Fig. 8. The same RIE

procedure results in the definition of metal interconnect structure 32, comprised of metal layer 19, and metal layer 13, communicating with active device regions, such as underlying metal interconnect structures, (not shown in the drawings), via metal plug structure 2b. After definition of these structures, photoresist shapes 30, are removed via plasma oxygen ashing and careful wet cleans. If desired underlying metal layer 13, as well as overlying metal layer 19, can be comprised of titanium, with a titanium nitride barrier layer, underlying metal layer 13, and with another titanium nitride barrier layer, located overlying metal layer 19.

While this invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit or scope of the invention.

What is claimed is:

1. A method of forming a metal - oxide - metal, capacitor structure, on a semiconductor substrate, comprising the steps of:

depositing a first metal layer on an underlying dielectric layer;

performing a laser ablation oxidation procedure at a power of about to 0.1 watts to a top portion of said first metal layer to form a capacitor dielectric layer on a bottom portion of said first metal layer, featuring specific process conditions allowing a higher temperature, between about 1000 to 2000^{o} C to be reached at the top surface of said first metal layer when compared to the temperature reached at other regions of said semiconductor substrate allowing said capacitor dielectric layer, between about 100 to 400 Angstroms, to be grown on the higher temperature top surface of said first metal layer;

depositing a second metal layer on said capacitor dielectric layer; and

patterning of said second metal layer, of said capacitor dielectric layer, and of said bottom portion of said first metal layer, to form said metal - oxide - metal, capacitor structure,

wherein said oxidation procedure is a UV or I line exposure, performed to a portion of said first metal layer, at an energy between about 1 to 100 millijoules, resulting in a tempertaure at the top surface of said first metal layer, between about 250 to 1000ºC.

2. A method of fabricating a high dielectric constant, (high K), layer, for a metal - oxide - metal, capacitor structure, via exposure of a region of an underlying metal layer, to a UV, or to an I line procedure, performed in an oxidizing ambient, comprising the steps of:

depositing said underlying metal layer;

performing said UV, or I line exposure, in said oxidizing ambient, to a region of said underlying metal layer, exposed through clear regions of a photolithographic plate, creating said high K layer, in a top portion of said underlying metal layer:

depositing an overlying metal layer on said high K layer; and

patterning of said overlying metal layer, of said high K layer, and of unoxidized, bottom portion of said underlying metal layer, forming said metal - oxide - metal, capacitor structure.

3. The method of claim 2, wherein said underlying metal layer is chosen from a group that includes, titanium, tantalum, aluminum, or copper, obtained via plasma vapor deposition, at a thickness between about 3000 to 5000 Angstroms.

4. The method of claim 2, wherein said UV, or said I line procedure, is performed at an energy between about 1 to 100 millijoules.

5. The method of claim 2, wherein said oxidizing ambient is chosen from a group that includes, O_2, O_3, NO, or N_2O.

6. The method of claim 2, wherein said high K layer is a metal oxide layer, chosen from a group that includes, TiO_2, Ta_2O_5, Al_2O_3, or CuO_2, at a thickness between about 100 to 400 Angstroms.

7. The method of claim 2, wherein said high K layer has a dielectric constant between about 22 to 35.

8. The method of claim 2, wherein said overlying metal layer is chosen from a group that includes aluminum, tantalum, titanium, or copper, obtained via plasma vapor deposition procedures, at a thickness between about 2500 to 4500 Angstroms.

9. The method of claim 2, wherein said metal - oxide - metal, capacitor structure is patterned via an anisotropic RIE procedure, using Cl_2 or SF_6, as an etchant for said overlying metal layer, and for said underlying metal layer, while either BF_3, or CF_4/CHF_3 is used as an etchant for said high K layer.