

DESCRIPTION

MANUFACTURING METHOD OF WIRING CIRCUIT BOARD, AND WIRING CIRCUIT BOARD

5

Technical Field

The present invention relates to a manufacturing method of wiring circuit board having a ceramic substrate, and a wiring circuit
10 board.

Background Art

Hitherto, a wiring circuit board having a ceramic substrate is manufactured by a method
15 comprising a step of applying a photosensitive conductor paste on the surface of a ceramic substrate made from a ceramic green sheet, and a step of processing the applied photosensitive conductor layer by photolithography and forming a
20 circuit pattern. The processing by photolithography consists of exposure and development by using a photo mask.

In such wiring circuit board, recently, a wiring circuit pattern having a fine line of 40 μm
25 or less is required in order to realize a high

density.

The invention presents a manufacturing method of a wiring circuit board for achieving a wiring circuit pattern of such fine line, and a wiring
5 circuit board.

Summary of the Invention

A manufacturing method of wiring circuit board of the invention comprises:

- 10 (a) a step of fabricating a ceramic substrate,
- (b) a step of polishing the surface of the ceramic substrate to surface roughness Ra of 0.5 μm or less,
- (c) a step of forming a photosensitive
15 conductor layer on the surface of the ceramic substrate, and
- (d) a step of processing the photosensitive conductor layer by photolithography, and forming a specified wiring pattern.

20 A circuit board of the invention comprises a ceramic substrate having surface roughness Ra of about 0.5 μm or less, and a wiring pattern formed on the surface of the ceramic substrate by photolithography.

25 Herein, supposing the roughness curve to be $y =$

f (x), the extracting length of the roughness curve in the center line direction to be L, the central axis of the extracting portion to be X-axis, and the direction vertical to the X-axis to be Y-axis, Ra is the value calculated in the formula:

$$Ra = (1/L) \int_0^L |f(x)| dx \quad (1)$$

In this constitution, a wiring pattern having a fine line of line width of 40 μ m or less is stably obtained on the ceramic substrate, and a circuit board of high density and high precision is obtained.

Brief Description of the Drawings

Fig. 1 is an explanatory diagram showing the manufacturing process of a manufacturing method of wiring circuit board in an embodiment of the invention.

Fig. 2 shows an example of roughness curve on the surface of a ceramic substrate in the manufacturing method of wiring circuit board in the embodiment of the invention.

Fig. 3 is a sectional view of a wiring circuit board in an embodiment of the invention.

Best Mode for Carrying Out the Invention

As a result of repeated studies and experiments, since the ceramic substrate is fabricated by sintering ceramic particles, it is found out that
5 the surface of the ceramic substrate has fine asperities, and that these asperities are disturbing minimization of line width of wiring pattern. Accordingly, in order to form a wiring pattern of a fine line width on the surface of
10 ceramic substrate, it is found important to define the degree of surface roughness of the ceramic substrate, important to polish to have a smaller surface roughness, and important to polish so that Ra as the degree of surface roughness may be 0.5
15 μm or less. As a result, the present invention is completed.

The manufacturing method of wiring circuit board of the invention comprises:

- (a) a step of fabricating a ceramic substrate,
- 20 (b) a step of polishing the surface of the ceramic substrate to surface roughness Ra of 0.5 μm or less,
- (c) a step of forming a photosensitive conductor layer on the surface of the ceramic
25 substrate, and

(d) a step of processing the photosensitive conductor layer by photolithography, and forming a specified wiring pattern.

The circuit board of the invention comprises a
5 ceramic substrate having surface roughness Ra of about 0.5 μm or less, and a wiring pattern formed on the surface of the ceramic substrate by photolithography.

Herein, supposing the roughness curve to be $y =$
10 $f(x)$, the extracting length of the roughness curve in the center line direction to be L, the central axis of the extracting portion to be X-axis, and the direction vertical to the X-axis to be Y-axis, Ra is calculated in the following
15 formula 1.

$$Ra = (1/L) \int_0^L |f(x)| dx \quad (1)$$

In this constitution, a wiring pattern having a fine line of line width of 40 μm or less is stably obtained without defect on the ceramic substrate,
20 and a circuit board of high density and high precision is obtained.

More preferably, the following constitution is required.

The step of forming the photosensitive
25 conductor layer includes a step of applying a

photosensitive conductor paste on the surface of the ceramic substrate, and a step of drying the photosensitive conductor paste.

The photolithography process includes a step of
5 exposing the photosensitive conductor layer through a photo mask, and a step of developing the exposed photosensitive conductor layer and removing the unexposed region.

The surface of the ceramic substrate is
10 polished by using a powder abrasive having a mean particle size in a range of about 0.1 μm to about 20 μm .

The wiring pattern has a fine line with a line width of about 40 μm or less.

15 The ceramic substrate is manufactured in the process of baking a ceramic green sheet having ceramic powder and binder.

The ceramic substrate is a sinter of a ceramic green sheet having ceramic powder and binder.

20 The wiring pattern obtained by the photolithography is a pattern of photosensitive conductor layer formed by exposing and developing the photosensitive conductor layer through a photo mask, by placing the photosensitive conductor
25 layer on the surface of the ceramic substrate.

That is, in the manufacturing method of the wiring circuit board for obtaining a wiring circuit on a ceramic substrate, by applying a photo-sensitive conductor paste on the surface of a ceramic substrate, printing a wiring circuit pattern on this applied layer, and exposing and developing, it is characterized by polishing the surface of the ceramic substrate so that the roughness Ra may be 0.5 μm or less before applying the paste.

An embodiment of the invention is specifically described below.

Fig. 1 shows the manufacturing process of a manufacturing method of a wiring circuit board in an embodiment in the invention.

In Fig. 1, a ceramic substrate 2 is manufactured in the same method as in the prior art, and its example is described below.

Ceramic powder, binder resin, plasticizer, and solvent are kneaded, and a slurry is prepared. Herein, the ceramic powder is a mixture of about 45 to about 60 wt.% of inorganic powder with mean particle size of about 0.5 to about 1.5 μm , and about 40 to about 55 wt.% of alumina powder with mean particle size of about 1.0 to about 2.0 μm .

The inorganic powder is a compound powder containing CaO , Al_2O_3 , SiO_2 , B_2O_3 , PbO , etc. Examples of binder resin include polyvinyl butyral resin, methacrylic acid resin, and other resin materials. As the plasticizer, any ordinary plasticizer may be used such as dibutyl phthalate. As the solvent, toluene, methyl ethyl ketone, or the like may be used.

By the doctor blade method or the like, from this slurry, a ceramic green sheet 1 of about 0.1 to about 0.3 mm in thickness is fabricated. This ceramic green sheet 1 is cut to a vertical length of 100 to 250 mm and a lateral length of 100 to 250 mm. As required, an internal circuit is placed on the surface of this ceramic green sheet 1. This ceramic green sheet 1 is laminated in multiple layers, pressed, and baked for 5 to 15 minutes at temperature of 880 to 950 °C. Thus, a ceramic substrate 2 is fabricated. The surface roughness R_a of thus fabricated ceramic substrate 2 is about 2.5 to about 5.0 μm .

Next, the surface 2b of the obtained ceramic substrate 2 is polished until the surface roughness R_a becomes 0.5 μm or less. Herein, the surface roughness R_a is measured and calculated as

follows. First, the roughness curve of the surface of the ceramic substrate is measured. A portion of measuring length L is extracted from the roughness curve in the direction of its center line, and the center line of the extracted portion is supposed to be X-axis, the direction of the vertical multiplication (the direction vertical to the X-axis) to be Y-axis, and the roughness curve to be $y = f(x)$, the surface roughness R_a is calculated in formula 1 above.

The polishing method of the surface of ceramic surface is not particularly limited, but the following method is an example. Using fine particle abrasive and grinding device, the surface is polished to surface roughness R_a of $0.5 \mu\text{m}$ or less. As the abrasive, fine particles of Al_2O_3 , SiC or the like may be used. The mean particle size of the abrasive is preferred to be about 0.5 to about $10 \mu\text{m}$. As the grinding device, lapping device or polishing device may be used.

On the polished ceramic substrate 2a, a photosensitive conductor paste 3 is applied. As the method of this application, an ordinary application method is employed. For example, the spin coat method, roll transfer method, or screen

printing method may be employed. In particular, the screen printing method is preferred. The photosensitive conductor paste is not particularly limited, but, for example, Ag compound photosensitive conductor paste, Au compound photosensitive conductor paste, or Cu compound photosensitive conductor paste may be used. The applied paste is dried at temperature of about 80 to about 100°C. Thus, a photosensitive conductor layer 3a is placed on the surface of the ceramic substrate 2a.

In succession, the photosensitive conductor layer 3a is processed by photolithography. Ultraviolet rays (UV rays) are passed through a photo mask 4 having a specified wiring circuit pattern to expose the photosensitive conductor layer 3a. At this time, the wavelength of ultraviolet rays is preferred to be about 350 to about 450 nm, and the exposure dose is preferred to be about 400 to about 1200 mJ.

The exposed photosensitive conductor layer 3a is developed. As the developing device, for example, an ordinary spray type developing device is used. The developing solution is sprayed over the exposed surface of the photosensitive

conductor layer 3a, and by this spray, the unexposed portion of the photosensitive conductor layer is dissolved and removed. Thus, the photosensitive conductor layer 3a is developed, and a wiring circuit pattern 3b is formed. At this time, the spray pressure is preferred to be about 0.2 to 0.8 kg/cm². As the developing solution, for example, an aqueous solution of sodium carbonate of about 0.4 to about 1.0% is used.

The ceramic substrate 2 having the developed wiring pattern 3b is baked for about 3 to 7 minutes at temperature of about 750 to 850 °C (preferably 780 to 820 °C). Thus, a wiring circuit board 5 having the wiring circuit pattern 3b is fabricated.

Concerning the surface roughness of the ceramic substrate before application of the photosensitive conductor paste 3, the surface roughness Ra of the ceramic substrate 2a is preferred to be about 0.5 μm or less. If the surface roughness Ra exceeds about 0.5 μm, it is not possible to form stably the wiring circuit pattern having a fine line of 40 μm or less.

Exemplary Embodiments

By presenting exemplary embodiments and comparative examples, the invention is further described below. It must be noted, however, that the invention is not limited to the illustrated
5 embodiments alone.

According to the aforesaid manufacturing method of ceramic green sheet, a ceramic green sheet 1 was fabricated. From this ceramic green sheet 1, a glass ceramic substrate 2 of Al_2O_3 - SiO_2 - B_2O_3 - PbO
10 system was fabricated.

The surface of the ceramic substrate 2 was polished by a grinding device (lapping device 9B-5L-IV or polishing device 9B-5P-IV, Speedfam) together with abrasive WA-#2000 or Polypla 700
15 (Fujimi Abrasive Industries, mean particle size 1.0 to 7.0 μm).

By this polishing, a first ceramic substrate 2a was obtained. The surface roughness Ra of this first ceramic substrate 2a was 0.5 μm .

20 On the other hand, using various different abrasives, the ceramic substrate 2 fabricated in the same manner was polished, and a second ceramic substrate 2a having surface roughness Ra of 0.38 was obtained. Similar, a third ceramic substrate
25 2a having surface roughness Ra of 0.25 was

obtained.

On the surface of these polished ceramic substrates 2a, photosensitive conductor paste 3 (Ag/Pt photosensitive conductor paste K3714, Du Pont) was applied by screen printing, and dried at temperature of 80 °C. Thus, a photosensitive conductor layer 3a was obtained.

In succession, ultraviolet rays (UV rays) of wavelength of 365 nm and exposure dose of 720 mJ were passed through a photo mask 4 having a wiring circuit pattern of specified shape to expose the photosensitive conductor layer. This photo mask 4 is a photo mask for test having a wiring pattern forming various line widths and line intervals and designed for measuring formable line widths and line intervals. Next, using a developing machine SL-400 (Shinwa Industrial), a developing solution (0.4% aqueous solution of sodium carbonate) was sprayed at a spray pressure of about 0.6 kg/cm² on the exposed surface of the photosensitive conductor layer 3a. By this spraying, the unexposed portion of the photosensitive conductor layer was dissolved and removed.

Thus developed wiring pattern was baked for 5 minutes at temperature of 855°C. In this process,

a wiring pattern 3b having a specified shape was formed on the surface of first ceramic substrate, second ceramic substrate and third ceramic substrate.

5 As a result, a wiring pattern of fine line having a line width of about 10 μm was obtained on the first ceramic substrate. Further, in the pattern of line width of about 10 μm or more, a fine line width was obtained.

10 On the second ceramic substrate, a wiring pattern of fine line having a line width of about 7 μm was obtained, and also in the pattern of line width of about 7 μm or more, a fine line width was obtained.

15 On the third ceramic substrate, a wiring pattern of fine line having a line width of about 5 μm was obtained, and also in the pattern of line width of about 5 μm or more, a fine line width was obtained.

20 These fine lines are fine lines having a continuous and constant width. In these wiring patterns, there was no defect such as shorting between fine lines or disconnection.

On the other hand, using the first ceramic
25 substrate 2a, second ceramic substrate 2a, and

third ceramic substrate 2a, wiring patterns were formed by varying the exposure dose, spray pressure, concentration of developing solution, other exposure conditions, developing conditions, and baking conditions. The exposure dose was changed in a range from about 400 mJ to about 1200 mJ. The spray pressure was changed in a range from about 0.2 kg/cm² to about 0.8 kg/cm². The aqueous solution of sodium carbonate as developing solution was changed in the concentration in a range from about 0.4% to about 1.0%. The baking condition of the developed ceramic substrate was changed in temperature in a range from about 780°C to about 820°C, and in the time from about 3 minutes to about 7 minutes. The photosensitive conductor paste 3 was same as the paste 3 above.

In all of thus obtained ceramic substrates forming wiring patterns, excellent effects having the same wiring pattern as above were obtained.

That is, a stable and fine line width was obtained regardless of exposure dose, spray pressure, concentration of developing solution, other exposure conditions, developing conditions, and baking conditions. Moreover, the wiring patterns obtained by such method were free from

any defect in the fine line width.

(Comparative Example)

Comparative examples are described below.

5 Using the same ceramic substrate 2 as the ceramic substrate used in the exemplary embodiments, the surface of the ceramic substrate 2 was polished to surface roughness Ra of 2.0 μm . The surface of other ceramic substrate 2 was
10 polished to surface roughness Ra of 1.1 μm . The surface of a different ceramic substrate 2 was polished to surface roughness of 0.7 μm .

 Thus, a fourth comparative ceramic substrate 2a having surface roughness Ra of 2.0 μm , a fifth
15 comparative ceramic substrate 2a having surface roughness Ra of 1.1 μm , and a sixth comparative ceramic substrate 2a having surface roughness Ra of 0.7 μm were prepared.

 Using the fourth comparative ceramic substrate
20 2a, fifth comparative ceramic substrate 2a and sixth comparative ceramic substrate 2a, wiring patterns 3b were formed in the same process as in the exemplary embodiments.

 As a result, on the fourth comparative ceramic
25 substrate 2a, a wiring pattern of fine line having

a line width of about 50 μm were obtained, but in the pattern of line width of about 50 μm or less, fine line having a constant width was not obtained. In the pattern of line width of about 50 μm or less, shorting, disconnection or other defect was noted.

On the fifth comparative ceramic substrate 2a, a wiring pattern of fine line having a line width of about 45 μm were obtained, but in the pattern of line width of about 45 μm or less, fine line having a constant width was not obtained. In the pattern of line width of about 45 μm or less, shorting, disconnection or other defect was noted.

On the sixth comparative ceramic substrate 2a, a wiring pattern of fine line having a line width of about 30 μm were obtained, but in the pattern of line width of about 30 μm or less, fine line having a constant width was not obtained. In the pattern of line width of about 30 μm or less, shorting, disconnection or other defect was noted.

Next, using the fourth comparative ceramic substrate 2a, fifth comparative ceramic substrate 2a and sixth comparative ceramic substrate 2a, same as in the exemplary embodiments, wiring patterns were formed by varying the exposure dose,

spray pressure, concentration of developing solution, other exposure conditions, developing conditions, and baking conditions.

As a result, by using the fourth comparative ceramic substrate 2a and fifth comparative ceramic substrate 2a, fine line having a constant line width of 40 μm or less was not obtained. In the case of the sixth comparative ceramic substrate 2a, in about 30% of substrates, fine line having a constant line width of 40 μm or less was not obtained depending on the developing conditions, exposure conditions and baking conditions.

As a result of these exemplary embodiments and comparative examples, by polishing the surface of ceramic substrate to surface roughness Ra of about 0.5 μm or less, it was found that a wiring pattern of fine line having a line width of about 40 μm or less is obtained, and moreover that a wiring pattern of such fine line is obtained stably.

Industrial Applicability

According to the manufacturing method of wiring circuit board of the invention, a wiring pattern of fine line having a line width of about 40 μm or

less can be formed on a ceramic substrate, and a wiring pattern of such fine line can be formed stably. As a result, a circuit board of high density and high precision is obtained.



CLAIMS

1. A manufacturing method of wiring circuit board comprising the steps of:

(a) fabricating a ceramic substrate,

5 (b) polishing a surface of said ceramic substrate to surface roughness R_a of $0.5 \mu\text{m}$ or less,

wherein supposing a roughness curve to be $y = f(x)$, an extracting length of the roughness curve in a center line direction to be L , a
10 central axis of an extracting portion to be X-axis, and a direction vertical to a X-axis to be Y-axis, R_a is a value calculated in a formula:

$$(1/L) \int_0^L |f(x)| dx$$

15 (c) forming a photosensitive conductor layer on the surface of said ceramic substrate, and

(d) processing said photosensitive conductor layer by photolithography, and forming a specified wiring pattern.

20

2. The manufacturing method of wiring circuit board of claim 1,

wherein at said step (c),

the step of forming said photosensitive
25 conductor layer includes



a step of applying a photosensitive conductor paste on the surface of said ceramic substrate, and

a step of drying said photosensitive conductor
5 paste.

3. The manufacturing method of wiring circuit board of claim 1,

wherein at said step (d),

10 the photolithography process includes

a step of exposing said photosensitive conductor layer through a photo mask, and

a step of developing said exposed photosensitive conductor layer and removing the
15 unexposed region.

4. The manufacturing method of wiring circuit board of claim 1,

wherein at said step (c),

20 the step of forming said photosensitive conductor layer includes

a step of applying a photosensitive conductor paste on the surface of said ceramic substrate, and

25 a step of drying said photosensitive conductor



paste, and

at said step (d),

the photolithography process includes

a step of exposing said photosensitive
5 conductor layer through a photo mask, and

a step of developing said exposed
photosensitive conductor layer and removing the
unexposed region.

10 5. The manufacturing method of wiring circuit
board of claim 1,

wherein at said step (b),

the surface of said ceramic substrate is
polished by using a powder abrasive having a mean
15 particle size in a range of about 0.1 μm to about
20 μm .

6. The manufacturing method of wiring circuit
board of claim 1,

20 wherein at said step (d) the wiring pattern has
a fine line with a line width of about 40 μm or
less.

7. The manufacturing method of wiring circuit
25 board of claim 1,



wherein at said step (a),

the ceramic substrate is manufactured in the process of baking a ceramic green sheet having ceramic powder and binder.

5

8. The manufacturing method of wiring circuit board of claim 1,

wherein said step (a) includes

a step of fabricating said ceramic substrate,

10 a step of fabricating a plurality of green sheets,

a step of placing internal circuits on the surface of each green sheet of said plurality of green sheets, and

15 a step of laminating, pressing and baking each green sheet having the individual internal circuit.

9. A wiring circuit board comprising:

a ceramic substrate having surface roughness R_a
20 of about $0.5 \mu\text{m}$ or less, in which supposing the roughness curve to be $y = f(x)$, the extracting length of the roughness curve in the center line direction to be L , the central axis of the extracting portion to be X-axis, and the direction
25 vertical to the X-axis to be Y-axis, R_a is the



value calculated in the formula: $(1/L) \int_0^L |f(x)| dx$, and
a wiring pattern formed on the surface of said
ceramic substrate by photolithography.

5 10. The wiring circuit board of claim 9,
 wherein said wiring pattern has a fine line of
 line width of 40 μ m or less.

 11. The wiring circuit board of claim 9,
10 wherein said ceramic substrate is a sinter of a
 ceramic green sheet having ceramic powder and
 binder.

 12. The wiring circuit board of claim 9,
15 wherein said wiring pattern obtained by
 photolithography is a pattern of a photosensitive
 conductor layer formed by exposing and developing
 said photosensitive conductor layer through a
 photo mask, using said photosensitive conductor
20 layer placed on the surface of said ceramic
 substrate.

 13. The wiring circuit board of claim 9,
 wherein said ceramic substrate is a sinter of
25 a laminated body of a plurality of green sheets,



and

each green sheet of said plurality of green sheets has an individual internal circuit on the surface.