



PATENT SPECIFICATION

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COMPLETE SPECIFICATION

DRAWINGS ATTACHED

Electronic Switching

We, RADIO CORPORATION OF AMERICA, a corporation organized under the laws of the State of Delaware, United States of America, of 30, Rockefeller Plaza, City and State of New York, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to synchronous detector circuits.

In synchronous detector circuits it is desirable to permit current flow in either direction through a switch when the switch is closed. Circuits have heretofore been proposed wherein a junction transistor is used as a bidirectionally conductive switching element with the desired signal information applied in series with the emitter-collector electrodes of the transistor and a switching voltage applied to the base electrode. One problem which has been encountered in such circuits is the contamination of the desired signal information by the switching voltage. The contamination includes a direct current (d-c) component developed across the base-emitter junction and an alternating current (a-c) component caused by switching currents flowing through the signal input and/or output circuits. Another problem encountered in switching circuits using junction transistors is that the range of desired signal amplitude for which the device exhibits linear characteristics is limited to a very small voltage.

The object of this invention is to provide improved synchronous detector circuits and according to the present invention there is provided a synchronous detector circuit comprising an insulated gate field-effect transistor having source, gate and drain

electrodes, a switching signal input circuit coupled between said gate and source electrodes, a rectifier connected between said gate and source electrodes and poled to provide a low impedance path for signals of a polarity tending to decrease the source to drain path resistance of said transistor, and a controlled circuit including a source of modulated wave energy to be detected and a load impedance element connected between said source and drain electrodes.

Where the switching signal circuit is capacitively coupled to the transistor and the rectifier is connected between the gate and source electrodes, the conduction of the rectifier charges the coupling capacitor to a voltage which maintains the transistor cut-off except during the interval of maximum switching signal voltage in the turn-on direction.

The invention will now be described with reference to the accompanying drawings, in which:

FIGURE 1 is a diagrammatic view of an insulated gate field-effect transistor suitable for use in circuits embodying the invention;

FIGURE 2 is a cross-sectional view taken along section line 2-2 of FIGURE 1;

FIGURE 3 is a graph showing a family of drain current versus source-to-drain voltage curves for various values of gate-to-source voltages for the transistor of FIGURES 1 and 2;

FIGURE 4 is a schematic circuit diagram of a balanced synchronous detector circuit embodying the invention;

FIGURES 5a, 5b and 5c are graphs of voltage waveforms on the same time base, useful in explaining the operation of the synchronous detector circuit of FIGURE 4;

FIGURE 6 is a schematic circuit diagram

[Price 4s. 6d.]

of another balanced synchronous detector circuit embodying the invention;

FIGURES 7a, 7b, 7c and 7d are graphs of voltage waveforms useful in explaining the operation of the synchronous detector circuit of FIGURE 6;

FIGURE 8 is a schematic circuit diagram of a single-ended synchronous detector circuit embodying the invention, with the switching voltage referenced with respect to ground;

FIGURE 9 is a schematic circuit diagram of a single-ended synchronous detector circuit embodying the invention, with the signals containing the desired modulation information referenced with respect to ground;

FIGURE 10 is a schematic circuit diagram of a sub-carrier wave synchronous detector circuit embodying the invention, for FM stereophonic receivers; and

FIGURES 11a, 11b and 11c are graphs of voltage waveforms useful in explaining the operation of the detector circuit of FIGURE 10.

FIGURE 1 shows an insulated gate field-effect transistor 10 which may be used with circuits embodying the invention and which includes a body 12 of semi-conductor material. The body 12 may be either a single crystal or polycrystalline and may be of any of the semiconductor materials used to prepare transistors in the semiconductor art. For example, the body 12 may be nearly intrinsic silicon, such as for example, lightly doped P-type silicon of 100 ohm cm. material.

In the manufacture of a device shown in FIGURE 1, heavily doped silicon dioxide is deposited over the surface of the silicon body 12. The silicon dioxide is doped with N-type impurities. By means of a photo-resist and acid etching, or other suitable technique, the silicon dioxide is removed where the gate electrode is to be formed, and around the outer edges of the silicon wafer as viewed on FIGURE 1. The deposited silicon dioxide is left over those areas where the source-drain regions are to be formed.

The body 12 is then heated in a suitable atmosphere such as in water vapour so that exposed silicon areas are oxidized to form grown silicon dioxide layers indicated by the stippled areas of FIGURE 1. During the heating process, impurities from the deposited silicon dioxide layer diffuse into the silicon body 12 to form the source and drain regions. FIGURE 2, which is a cross-sectional view taken along section line 2-2 of FIGURE 1, shows the source-drain regions labelled S and D respectively.

By means of another photo-resist and acid etching or like step, the deposited silicon dioxide over part of the source-drain

diffused regions are removed. Electrodes are formed for the source, drain and gate regions by evaporation of a conductive material by means of an evaporation mask. The conductive materials evaporated are either chromium or gold, with chromium being preferred, but other suitable electrically conductive material may be used.

The finished wafer is shown in FIGURE 1, in which the stippled area between the outside boundary and the first more darkly stippled zone is grown silicon dioxide. The white area 16 is the metal electrode corresponding to the source electrode. Dark zones 14 and 18 are deposited silicon dioxide zones overlying the diffused source region, and the dark zone 20 is a deposited silicon dioxide zone overlying the diffused drain region. White areas 22 and 24 are the metallic electrodes which correspond to the gate and drain electrodes respectively. The stippled zone 28 is a layer of a grown silicon dioxide on a portion of which the gate electrode 22 is placed and which insulates the gate electrode 22 from the substrate silicon body 12 and from the source and drain electrodes as shown in FIGURE 2. The input resistance of the device at low frequencies is of the order of 10^{14} ohms.

The layer of grown silicon dioxide 28 on which the gate electrode 22 is mounted, overlies an inversion layer or channel C of controllable conductivity connected the source and drain regions. The gate electrode 22 is displaced symmetrically between the source region S and the drain region D. If desired, the gate electrode 22 may be displaced towards the source region S and may overlap the deposited silicon dioxide layer 18.

It should be noted that electrodes D and S interchangeably operate as the drain and the source electrodes as a function of the polarity of the bias potential applied therebetween; i.e., the electrode to which a positive bias potential is applied (relative to the bias potential applied to the other electrode) operates as a drain electrode. The conduction of current through the channel C is by majority current carriers, in the present case electrons. If the device has an N-type substrate, and P-type source and drain regions, the majority current carriers are holes, and the electrode to which the negative terminal of a supply source is applied operates as the drain electrode.

The channel C, i.e., the source-to-drain current path, has controllable conductivity as shown by FIGURE 3. The conductivity of the channel C is a function of the amplitude and polarity of the gate-to-source bias voltage applied. FIGURE 3 is a family of curves 29-41 illustrating the linear portion below the knee of the drain current versus drain voltage characteristic of the insulated

gate field-effect transistor shown in FIGURE 1 connected in a common source configuration.

In order to more easily explain the conditions for obtaining the curves shown in FIGURE 3, one of the two electrodes will always be referred to as the drain electrode regardless of the polarity of the bias voltage applied thereto, and the other electrode will be referred to as the source electrode. The curves 29-41 shown in the first quadrant in FIGURE 3 were obtained by applying a bias potential to the drain electrode which is positive with respect to the potential of the source electrode, and by biasing the gate electrode with respect to the source electrode by a voltage having a magnitude as indicated by the voltage of E_g (gate voltage) corresponding to each of the curves 29-41. The portion of the curves 29-41 corresponding to the third quadrant were obtained by reversing the polarity of the bias voltage applied between the source and drain electrodes, i.e., by applying a bias potential to the drain electrode which is negative with respect to the potential of the source electrode.

It should be noted that the drain current versus drain voltage characteristics shown in FIGURE 3 is substantially linear over a substantial range of drain voltages as compared to a bipolar or junction transistor. With a gate-to-source voltage corresponding to the curve 29, substantially no source-to-drain current flows, while a gate-to-source voltage corresponding to the curve 41 permits source-to-drain current as a linear function of applied source-to-drain voltage.

A feature of an insulated gate field-effect transistor is that it can be manufactured so that the zero gate bias voltage characteristic is at any one of the curves shown in FIGURE 3. In FIGURE 3, for example, the curve 41 corresponds to the zero bias voltage curve, as indicated by the notation $E_g = 0$. The location of the zero bias curve is established during the manufacture of the transistor, e.g., by controlling the time and/or temperature of the step of the process when the silicon dioxide layer 28 shown in FIGURES 1 and 2 is grown. The longer the transistor is baked and the higher the temperature, in a dry oxygen atmosphere, the larger the drain current will be for a given amount of drain voltage at zero bias between the source and gate electrodes. Hence, if desired, the curve 29 could be made to correspond to the zero gate bias condition, with the curves 30-41 corresponding to progressively more positive gate voltages.

Reference is now made to FIGURE 4 which is a schematic circuit diagram of a balanced synchronous detector circuit employing a pair of insulated gate field-effect

transistors 43 and 44 which may be similar to the transistor described with reference to FIGURES 1 and 2. The transistor 43 has a source electrode 45, a drain electrode 46, and a gate electrode 47, and the transistor 44 has a source electrode 48, a drain electrode 49, and a gate electrode 50.

Switching signals from a source, not shown, are coupled through a transformer 51 having a centertapped secondary winding 52. The opposite ends of the secondary winding 52 are coupled to the gate electrodes 47 and 50 through the coupling capacitors 53 and 54 respectively. The centertap of the secondary winding 52 is connected to the source electrodes 45 and 48 which are at ground potential.

A first rectifier 55 is connected between the gate electrode 47 and the source electrode 45 of the transistor 43 and a second rectifier 56 is connected between the gate electrode 50 and the source electrode 48 of the transistor 44. The poling of the rectifiers 55 and 56 is such that they are respectively rendered conductive for signal excursions tending to drive the respective gate electrodes 47 and 50 positive relative to ground, which is the polarity direction tending to increase the source-drain current in the transistors 43 and 44.

Signal modulated waves from a source (not shown) are coupled to a transformer 60 which has a centertapped secondary winding 61. The secondary winding 61 is connected between the drain electrodes 46 and 49 respectively, and the centre-tap is connected to a utilization or load circuit 62 having an internal resistance represented by a resistor 63. The capacitor 64 which is connected between the centertap of the secondary winding 61 and ground serves as a storage capacitor. It is not necessary to have a completed direct current path between the source and drain electrodes of the transistors 43 and 44, and hence signals may be capacitively coupled to the load circuit 62.

The circuit of FIGURE 4 may be used, by way of example, as a subcarrier detector for stereophonic FM receivers. Such a subcarrier wave is a double-sideband amplitude-modulated suppressed carrier wave at 38 Kc/s, which is transmitted together with a 19 Kc/s (half carrier frequency) pilot signal for use in demodulation.

The subcarrier sidebands are applied to the primary winding of the transformer 60, and the pilot signal which has been doubled in frequency by suitable circuitry, as is known in the art, is applied to the primary winding of the transformer 51.

The frequency doubled pilot signal will be referred to as the switching or sampling signal, and is shown in the graphs of FIGURE 5a. The solid line waveform 65 is

intended to represent the sinusoidal switching waveform as measured between the gate electrode 47 and ground. The dashed line waveform 66 is intended to represent the sinusoidal wave as measured between the gate electrode 50 and ground. As the switching signal drives the gate electrode 47 positive, the diode 55 conducts charging the capacitor 53 to a voltage which builds up to a value approximating the peak level of the switching voltage 65. The diode 55 conducts only at the peaks of the switching signal as indicated by the "X"'s 67. During the interval between switching signal positive voltage peaks, the charge on the capacitor 53 is of a polarity to hold the gate 47 negative, and is of sufficient amplitude to maintain the transistor 43 cutoff. The transistor 44 operates in a manner similar to the transistor 43 but is rendered conductive at the peaks represented by the "O"'s 68 shown in FIGURE 5a.

FIGURE 5b is a graph showing the sideband envelope of the signals applied to the drain electrodes 46 and 49. The "X"'s 69 and "O"'s 70 on the waveform indicate the times when the source-to-drain resistance of the transistors 43 and 44 respectively is very low. During the remainder of each cycle the transistor will completely cutoff by the high negative part of the switching signal. It will be noted that the sideband envelope is sampled at a 76 Kc/s sampling rate due to the push-pull sampling technique. The storage capacitor 64 is charged to the instantaneous sideband voltage at the times indicated by the "X"'s and "O"'s of FIGURE 5b. The output voltage across capacitor 64 is a many step approximation of the modulating signal as shown in FIGURE 5c. The lowest "spurious" output frequency, being 76 Kc/s, is easily removed by a simple low-pass filter, since the amplitude of this spurious output frequency is always smaller than the desired audio output signal.

The product detector circuit of FIGURE 4 provides excellent operational characteristics in that a modulated signal is efficiently demodulated without contamination in a relatively simple circuit. No direct voltage polarizing supply is required, and hence d-c stability problems associated with supply voltage drift, device aging, and the like are not encountered. Furthermore, the impedance between the gate electrode and the source or drain electrodes of the transistors is so high that substantially no current from the switching signal source flows in the input or output circuit to contaminate the desired signal. Still further, since no rectifying junction exists between the gate and source or drain electrodes, as there is in junction transistors, there is no undesirable

temperature responsive offset voltage which would otherwise appear across the output circuit and contaminate the desired signal. Another advantage of the described circuit is that linear operation is maintained over a range of relatively large signal voltages applied between the source and drain electrodes as compared to junction transistor circuits.

The circuit shown in FIGURE 4 operates as a peak or narrow phase angle sampling detector. With modification, the circuit can function as an average detector employing 180° sampling as shown in FIGURE 6. In the circuit of FIGURE 6 the switching signal is applied through a transformer 80 to the gate electrodes of a pair of transistors 81 and 82. A rectifier 83 is connected between the gate and source electrodes of the transistor 81, and a rectifier 84 is connected between the gate and source electrodes of the transistor 82. A pair of current limiting resistors 85 and 86 respectively connect the gate electrodes of the transistors 81 and 82 to the opposite ends of the centertapped secondary winding of the transformer 80.

The signal modulated waves, from a source not shown, are applied through a transformer 90 the secondary winding of which is connected between the drain electrodes of the transistors 81 and 82. The drain current of the transistors 81 and 82 is derived from a centretap on the secondary winding of the transformer 90, and passes through a low-pass filter 91 to remove higher order components from the demodulated signal.

The action of the resistors 85 and 86 and the diodes 83 and 84 causes the gate electrodes of the transistors 81 and 82 to be clamped at ground potential for half of each input cycle and then go heavily negative for the other half cycle. This results in the voltage waveform at the gate electrodes of transistors 81 and 82 respectively shown in the graphs of FIGURES 7a and 7b. The rectification of the positive portion of the voltage waveform ensures that the variation in transconductance (gm) caused by the sinusoidally varying gate voltage will not add distortion to the demodulated output signal.

The drain current of the transistors 81 and 82 as measured between the centretap on the secondary winding of the transformer 90 and ground, is shown in the graph of FIGURE 7c. The drain current of the transistor 81 is represented as half cycles denoted by "X" and the drain current of the transistor 82 is shown as those half cycles denoted by "O". A low-pass filter 92 removes the high frequency components and provides the original pure modulating information which is shown in FIGURE 130

7d. It will be noted that the sampling occurs at twice the switching voltage rate, and the transistors 81 and 82 sequentially sample for 180° of the switching voltage cycle. Considered from an overall standpoint, the detector of FIGURE 6 affords full 360° sampling and provides high performance characterized by good signal-to-noise ratio (noise immunity) and freedom from distortion and intermodulation effects. In addition, the advantages with respect to d-c stability and lack of desired signal contamination are also present in the circuit of FIGURE 6.

The circuits shown in FIGURES 4 and 6 can also be used in the "single-ended" form as shown in FIGURE 8. In the circuit of FIGURE 8 the switching signals from a source, not shown, are coupled through a transformer 100 and a coupling capacitor 101 between the gate and source electrodes of the transistor 102. A diode 103 is directly coupled between the gate and source electrode of the transistor 102. The diode 103 is poled for conduction when the polarity excursion of the switching signal is in a direction to turn-on the transistor 102.

Signal modulated waves, from a source not shown, are coupled through a transformer 104, the secondary winding of which is connected in series with a low-pass filter 105 between the collector of the transistor 102 and ground.

Due to the action of the capacitor 101 and the rectifier 103, the circuit of FIGURE 8 operates as a single-ended peak or narrow angle synchronous detector. Where the detector circuit is used for demodulating an FM subcarrier wave, sampling occurs at a 38 Kc/s rate since the transistor 102 is rendered conductive once for each cycle of the switching signal.

FIGURE 9 shows a modification of the circuit of FIGURE 8 wherein the signal modulated waves are coupled between the source electrode of the transistor 110 and ground, and the demodulated signal waves are derived from a low-pass filter 111 connected to the drain electrode of the transistor 110. Otherwise the circuit is similar to that shown in FIGURE 8 and operates as a single-ended peak or narrow angle synchronous detector circuit.

The circuit shown in FIGURE 10 is a subcarrier wave detector for FM stereophonic receivers. A received 19 Kc/s pilot wave is separated from the remainder of the composite FM signal and applied without doubling to the primary winding of transformer 120 having a centretapped secondary winding 121. The opposite ends of the secondary winding 121 are coupled respectively through capacitors 122 and 123 to the gate electrodes of a pair of transistors

124 and 125. A rectifier 126 is coupled between the gate and source electrodes of transistor 124 and the rectifier 127 is coupled between the gate and source electrodes of the transistor 125. The centretap of the secondary winding 121 and the source electrodes of the transistors 124 and 125 are grounded.

The subcarrier sideband energy representative of the difference between the stereophonic signals to be reproduced is coupled to the primary winding of a transformer 128. One terminal of the secondary winding of the transformer 128 is coupled in common to the drain electrode of the transistors 124 and 125, and the other terminal of the secondary winding is coupled to storage capacitor 129 across which the output signal is derived.

The subcarrier sideband energy applied through the transformer 128 is represented by the graph shown in FIGURE 11a. The 19 Kc/s switching signal as measured between the gate electrode of the transistor 124 and ground is shown by the curve 130 of FIGURE 11b, and the curve 131 represents the switching waveform as measured between the gate of the transistor 125 and ground. Since the 19 Kc/s pilot signal is fed in push-pull relation to the gates of the transistor 124 and 125, and the 38 Kc/s sideband signal is applied in parallel to the drains, the sideband envelope is sampled at a 38 Kc/s rate, and the samples as stored by the capacitor 129, result in the waveform shown in FIGURE 11c. With a detector of the type shown in FIGURE 10, it is unnecessary to derive a stable source of 38 Kc/s subcarrier from the 19 Kc/s pilot signal to provide the desired 38 Kc/s sampling rate.

Although the circuits of the various figures have been described in connection with an insulated-gate field-effect transistor having a P-type semiconductor substrate, other types of insulated gate field-effect transistors may be used. For example, a complementary conductivity type device having an N-type semiconductor substrate may be used.

WHAT WE CLAIM IS:

1. A synchronous detector circuit comprising an insulated gate field-effect transistor having source, gate and drain electrodes, a switching signal input circuit coupled between said gate and source electrodes, a rectifier connected between said gate and source electrodes and poled to provide a low impedance path for signals of a polarity tending to decrease the source to drain path resistance of said transistor, and a controlled circuit including a source of modulated wave energy to be detected and a load impedance element connected between said source and drain electrodes.



7d. It will be noted that the sampling occurs at twice the switching voltage rate, and the transistors 81 and 82 sequentially sample for 180° of the switching voltage cycle. Considered from an overall standpoint, the detector of FIGURE 6 affords full 360° sampling and provides high performance characterized by good signal-to-noise ratio (noise immunity) and freedom from distortion and intermodulation effects. In addition, the advantages with respect to d-c stability and lack of desired signal contamination are also present in the circuit of FIGURE 6.

The circuits shown in FIGURES 4 and 6 can also be used in the "single-ended" form as shown in FIGURE 8. In the circuit of FIGURE 8 the switching signals from a source, not shown, are coupled through a transformer 100 and a coupling capacitor 101 between the gate and source electrodes of the transformer 102. A diode 103 is directly coupled between the gate and source electrode of the transistor 102. The diode 103 is poled for conduction when the polarity excursion of the switching signal is in a direction to turn-on the transistor 102.

Signal modulated waves, from a source not shown, are coupled through a transformer 104, the secondary winding of which is connected in series with a low-pass filter 105 between the collector of the transistor 102 and ground.

Due to the action of the capacitor 101 and the rectifier 103, the circuit of FIGURE 8 operates as a single-ended peak or narrow angle synchronous detector. Where the detector circuit is used for demodulating an FM subcarrier wave, sampling occurs at a 38 Kc/s rate since the transistor 102 is rendered conductive once for each cycle of the switching signal.

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124 and 125. A rectifier 126 is coupled between the gate and source electrodes of transistor 124 and the rectifier 127 is coupled between the gate and source electrodes of the transistor 125. The centretap of the secondary winding 121 and the source electrodes of the transistors 124 and 125 are grounded.

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WHAT WE CLAIM IS:

1. A synchronous detector circuit comprising an insulated gate field-effect transistor having source, gate and drain electrodes, a switching signal input circuit coupled between said gate and source electrodes, a rectifier connected between said gate and source electrodes and poled to provide a low impedance path for signals of a polarity tending to decrease the source to drain path resistance of said transistor, and a controlled circuit including a source of modulated wave energy to be detected and a load impedance element connected between said source and drain electrodes.



2. A synchronous detector circuit according to Claim 1, wherein said input circuit includes a resistor coupling said input circuit to the point of connection of said rectifier to said gate electrode.
3. A synchronous detector circuit according to Claim 1, wherein a low-pass filter is connected in series with said controlled circuit.
- 10 4. A synchronous detector circuit according to Claim 1, comprising a further insulated gate field-effect transistor and wherein said switching signal input circuit is connected in push-pull relation between the gate electrodes of said transistors, and said controlled circuit is connected in push-pull relation between the collector of electrodes of said transistors.
5. A synchronous detector circuit substantially as herein described with reference 20 to any one of Figures 4, 6, 8, 9 and 10 of the accompanying drawings.

A. M. & WM. CLARK,
Chartered Patent Agents,
5, Stone Buildings,
Lincoln's Inn,
London, W.C.2.

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