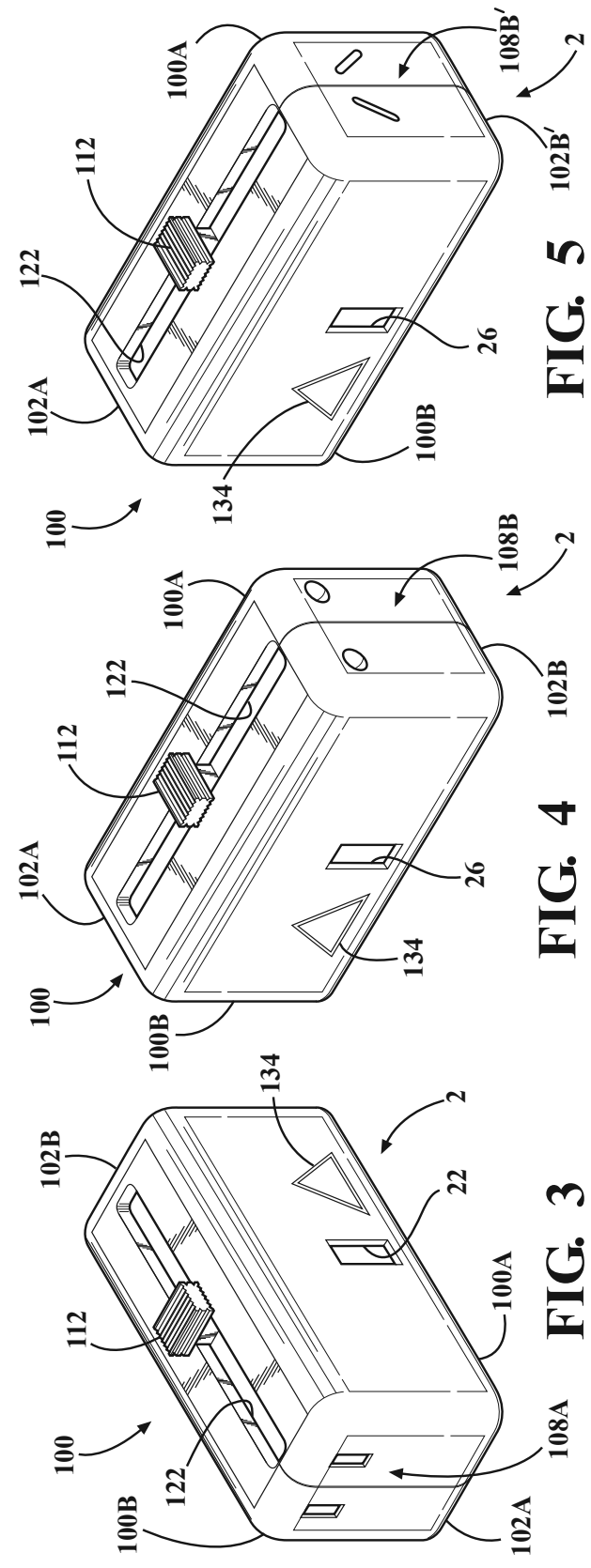
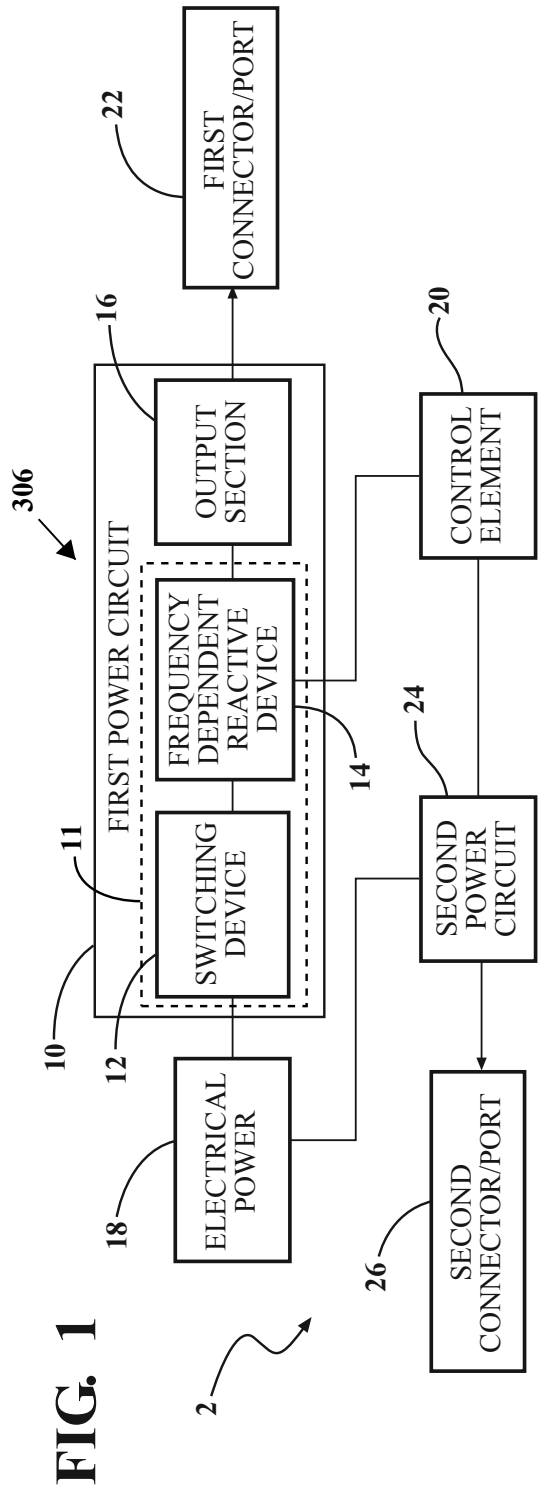




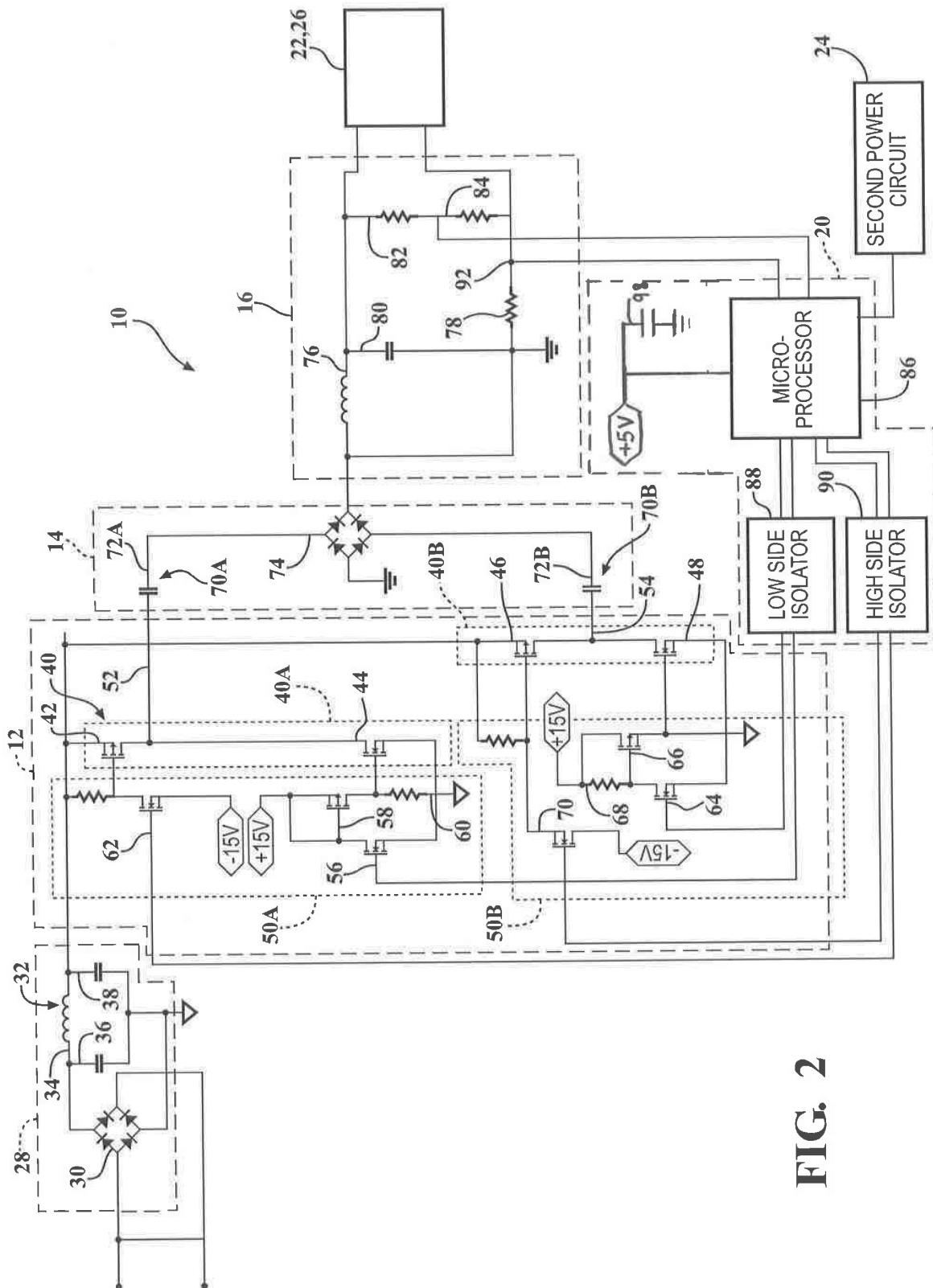


FIG. 2

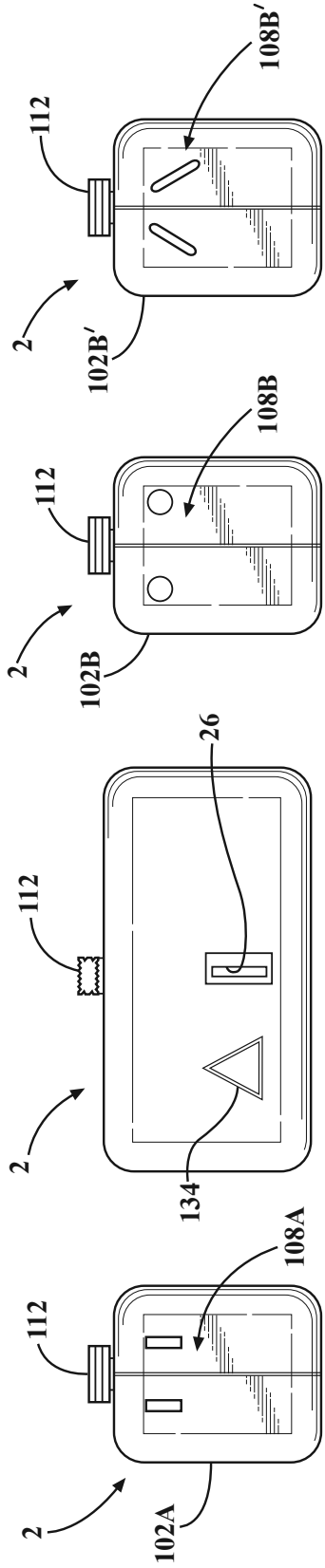


FIG. 6

FIG. 7

FIG. 8

FIG. 9

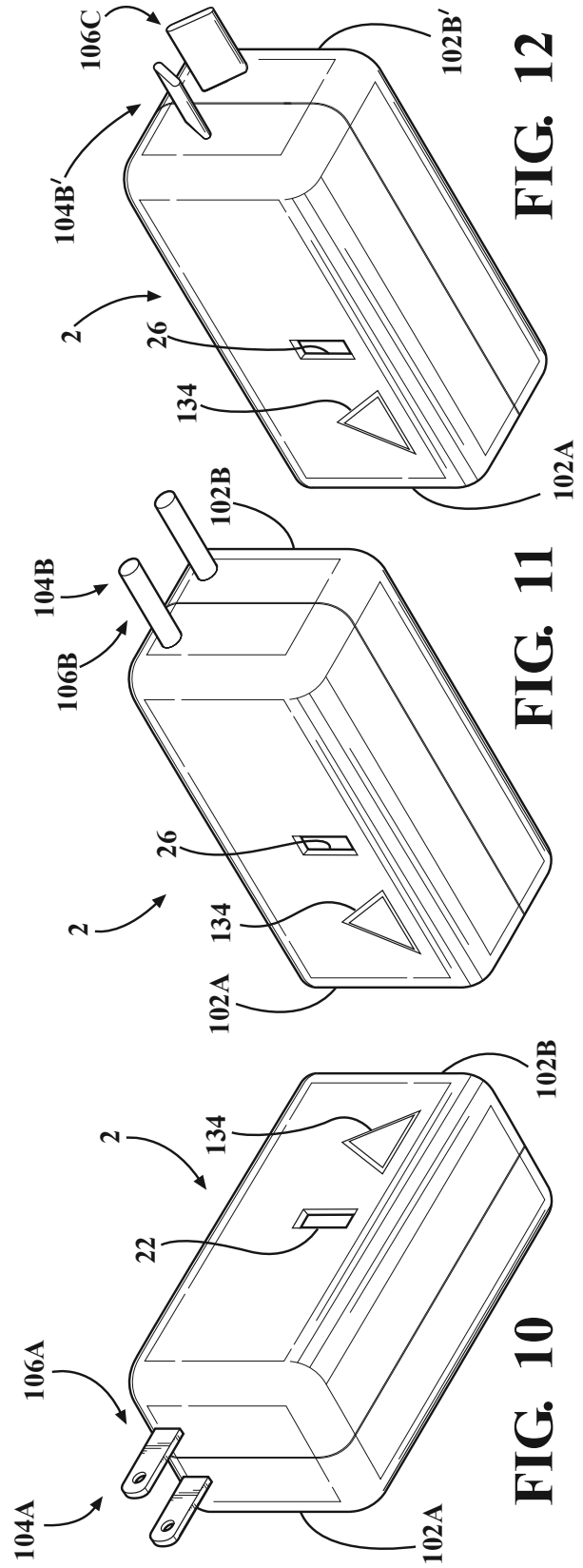


FIG. 10

FIG. 11

FIG. 12

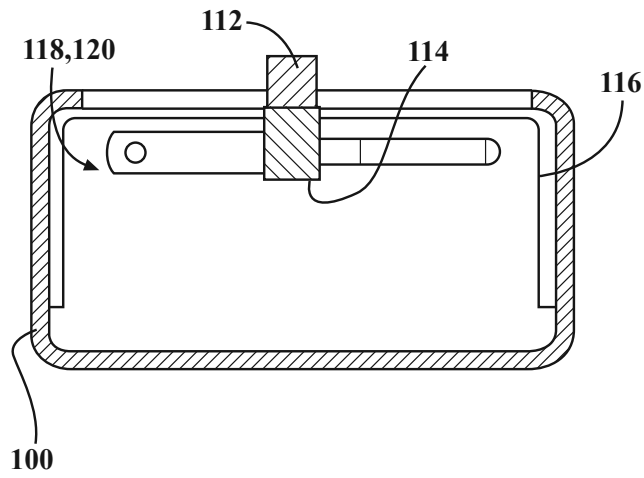


FIG. 13

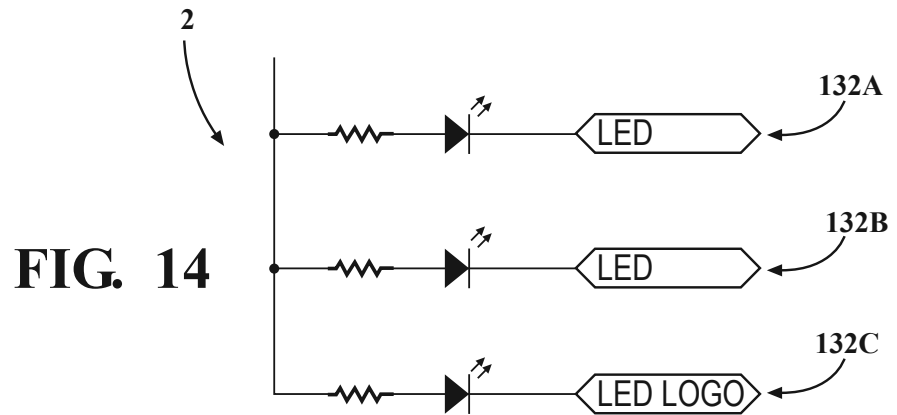


FIG. 14

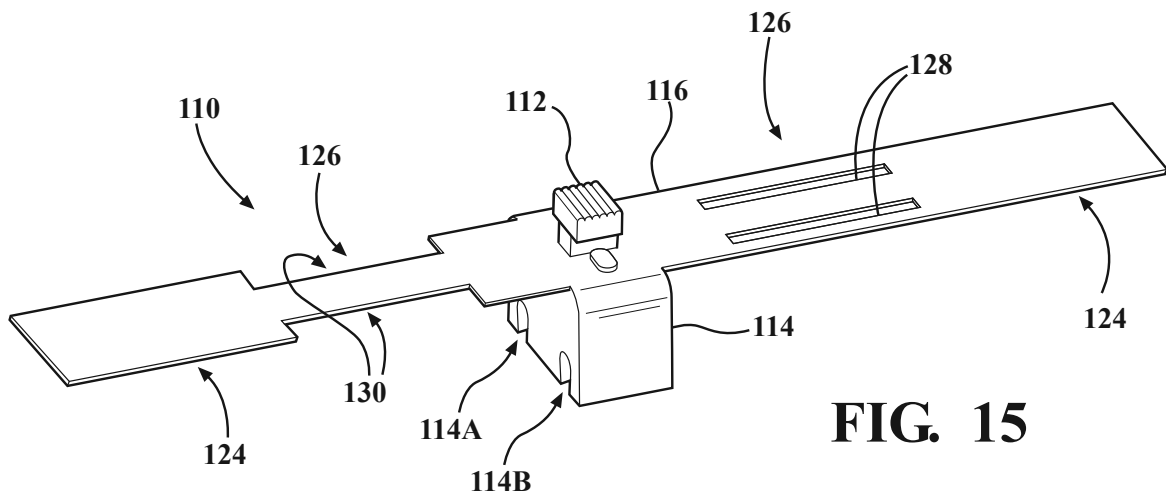
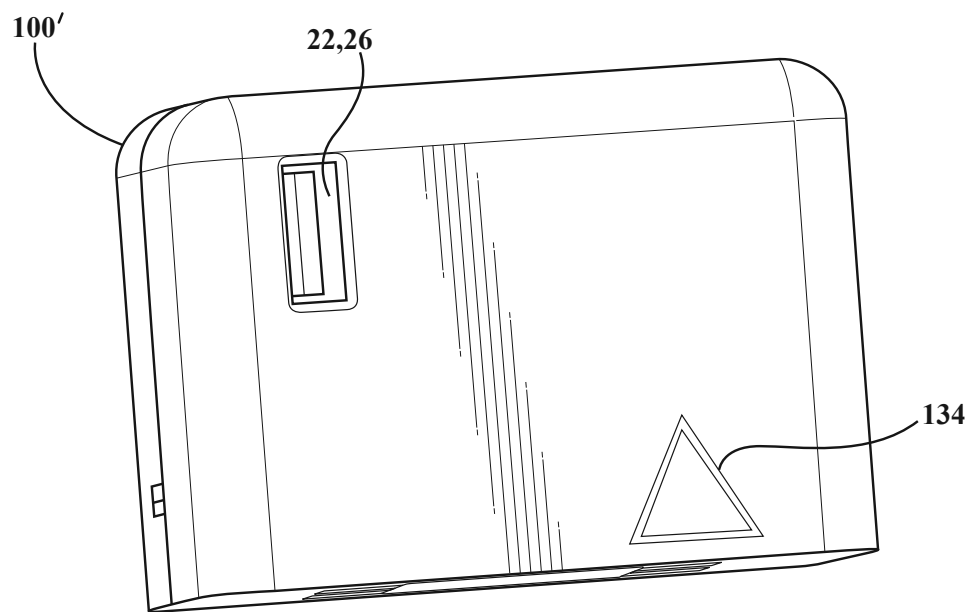
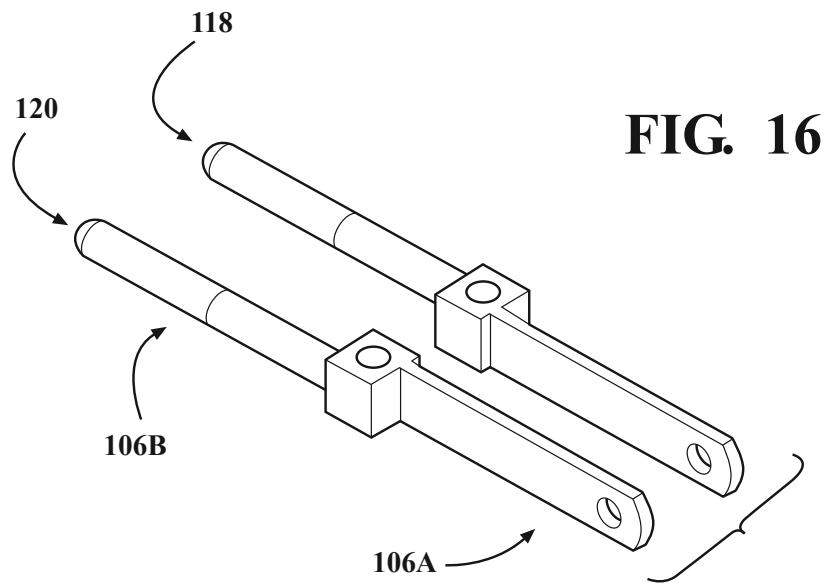
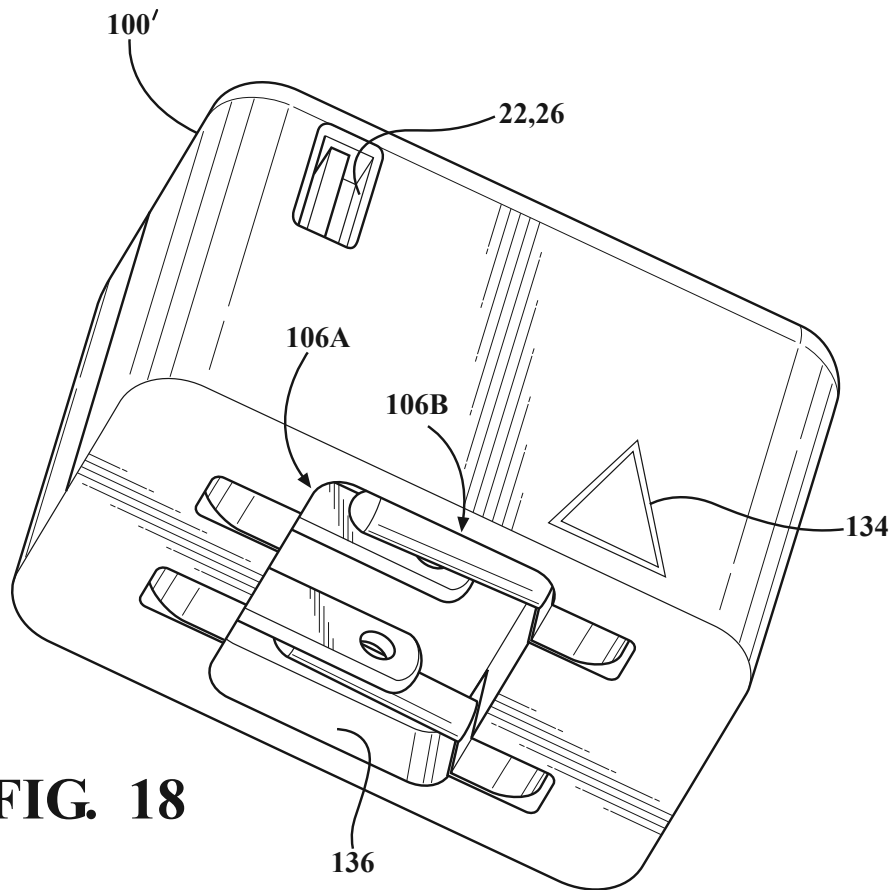


FIG. 15



**FIG. 18**

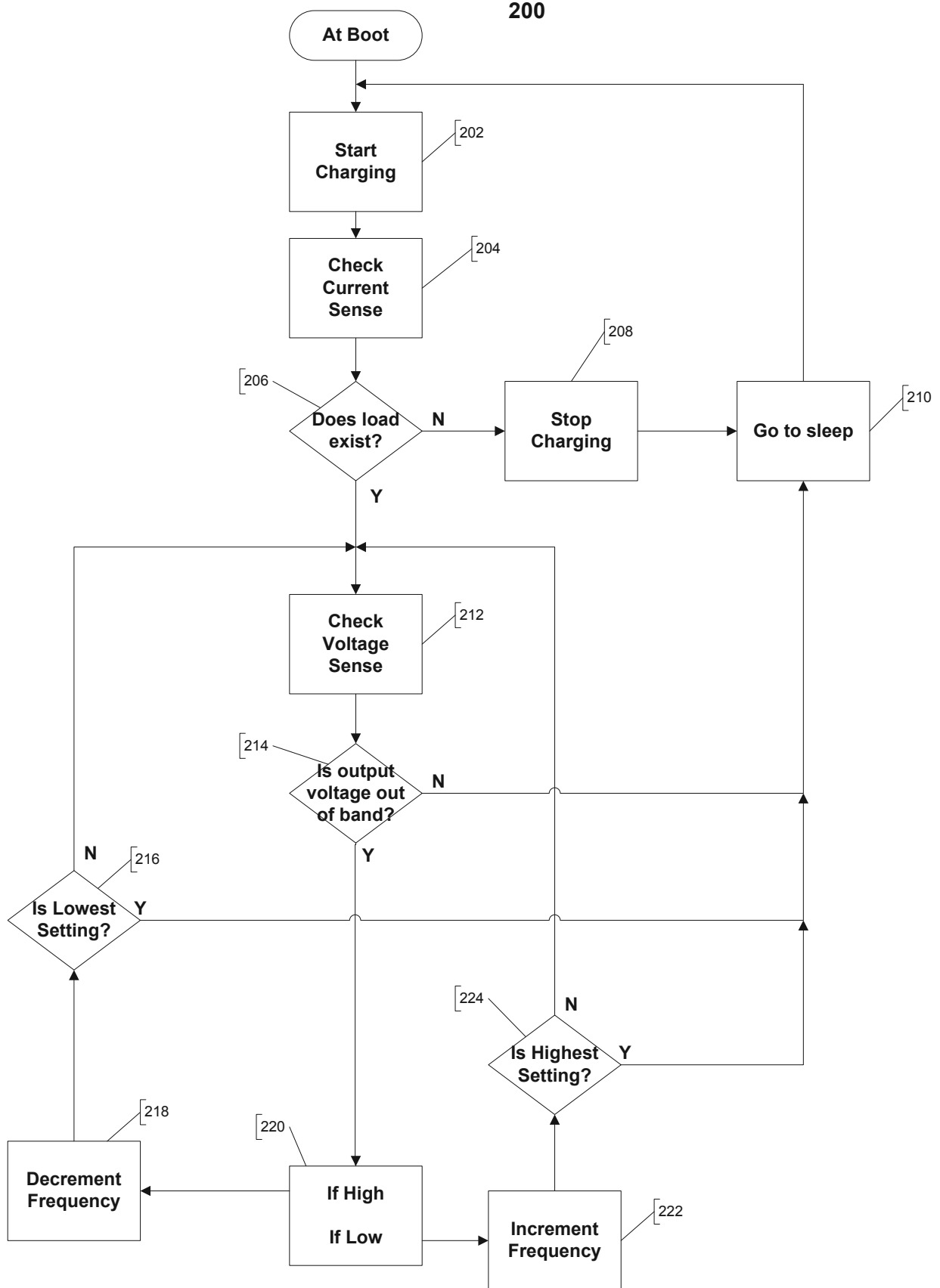


Figure 19

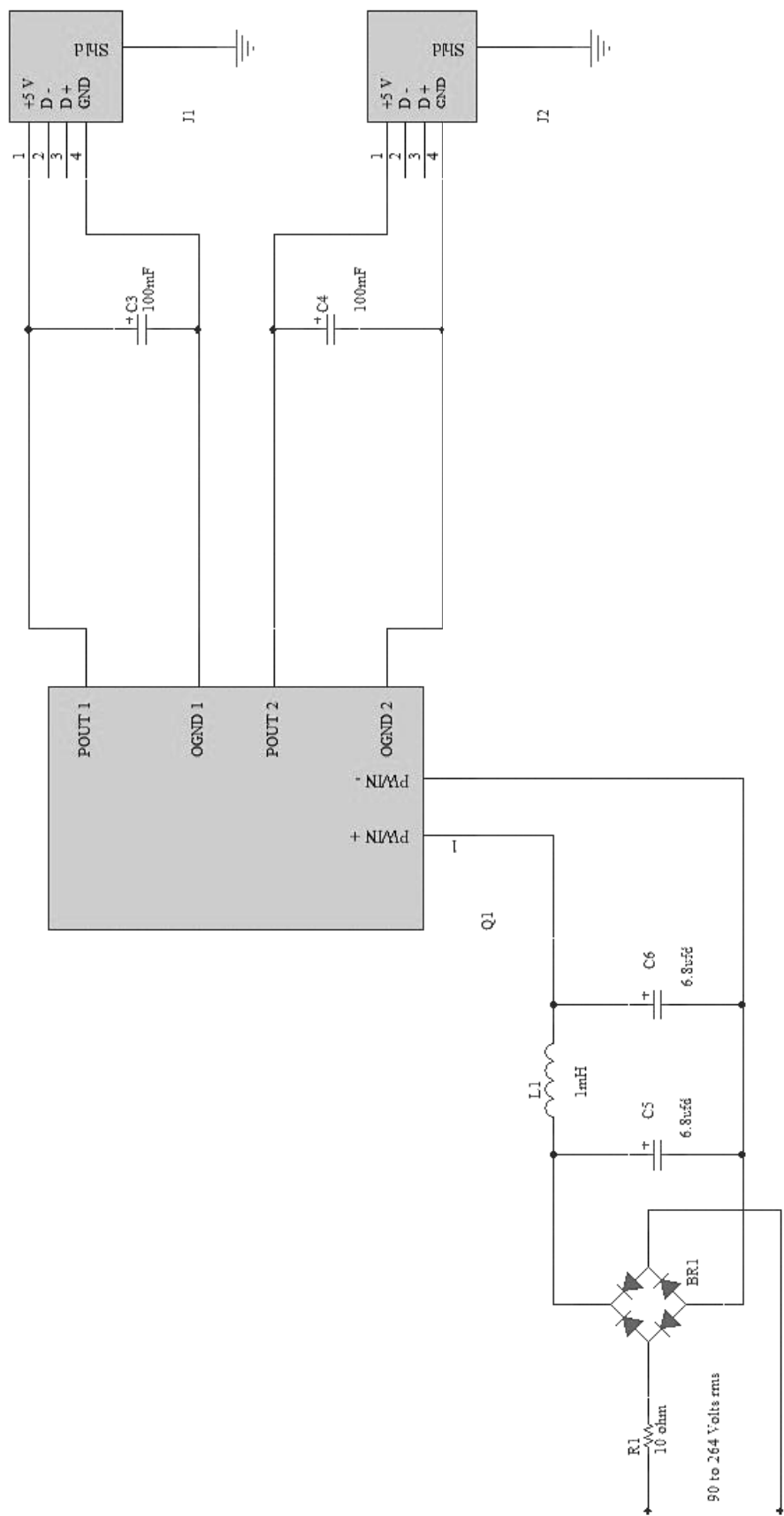


FIG. 20

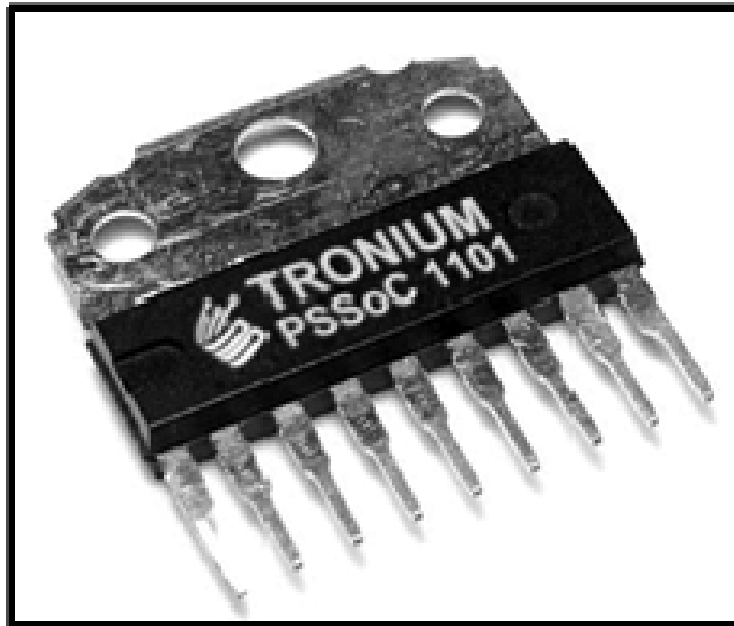


FIG. 21

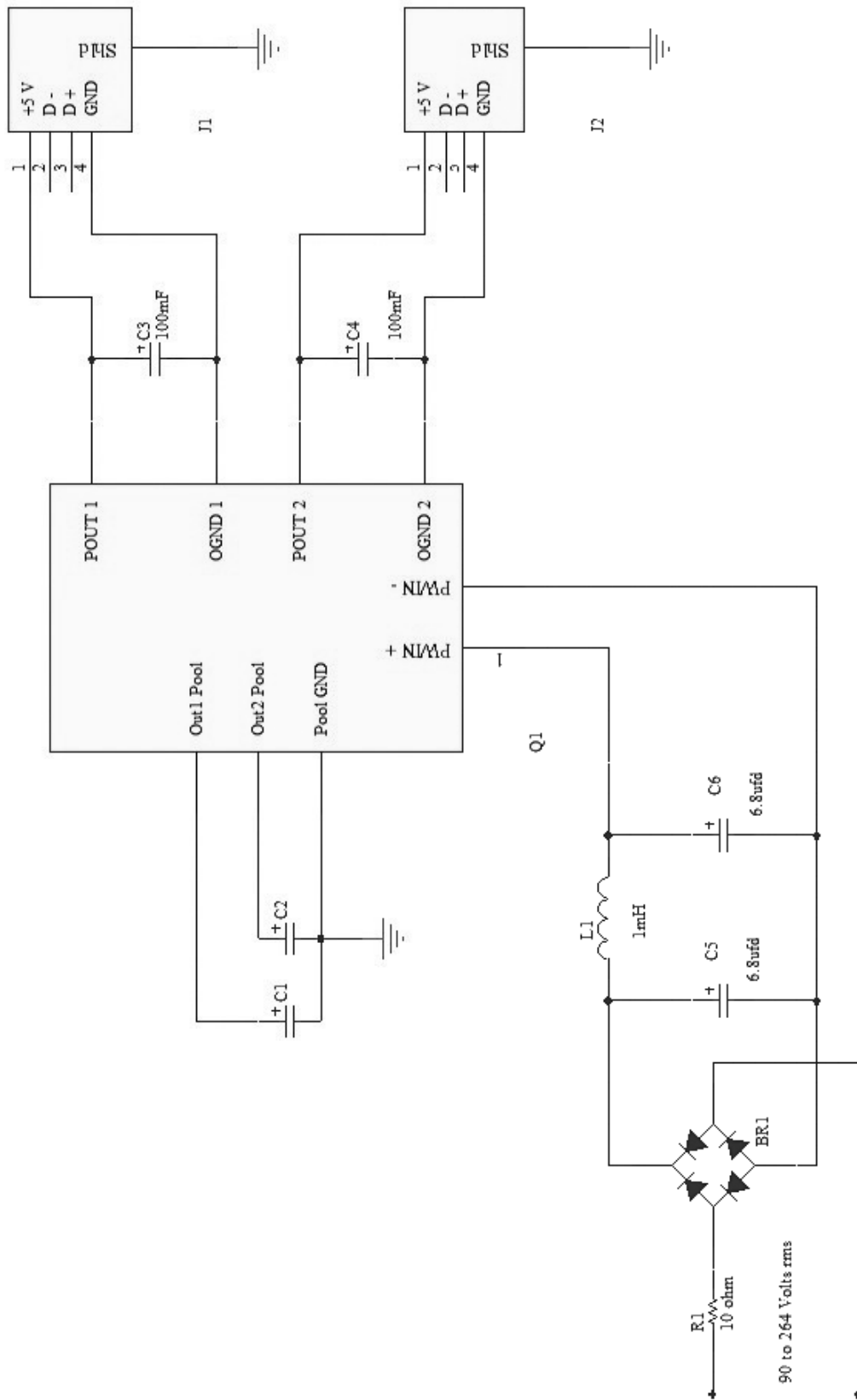


FIG. 22

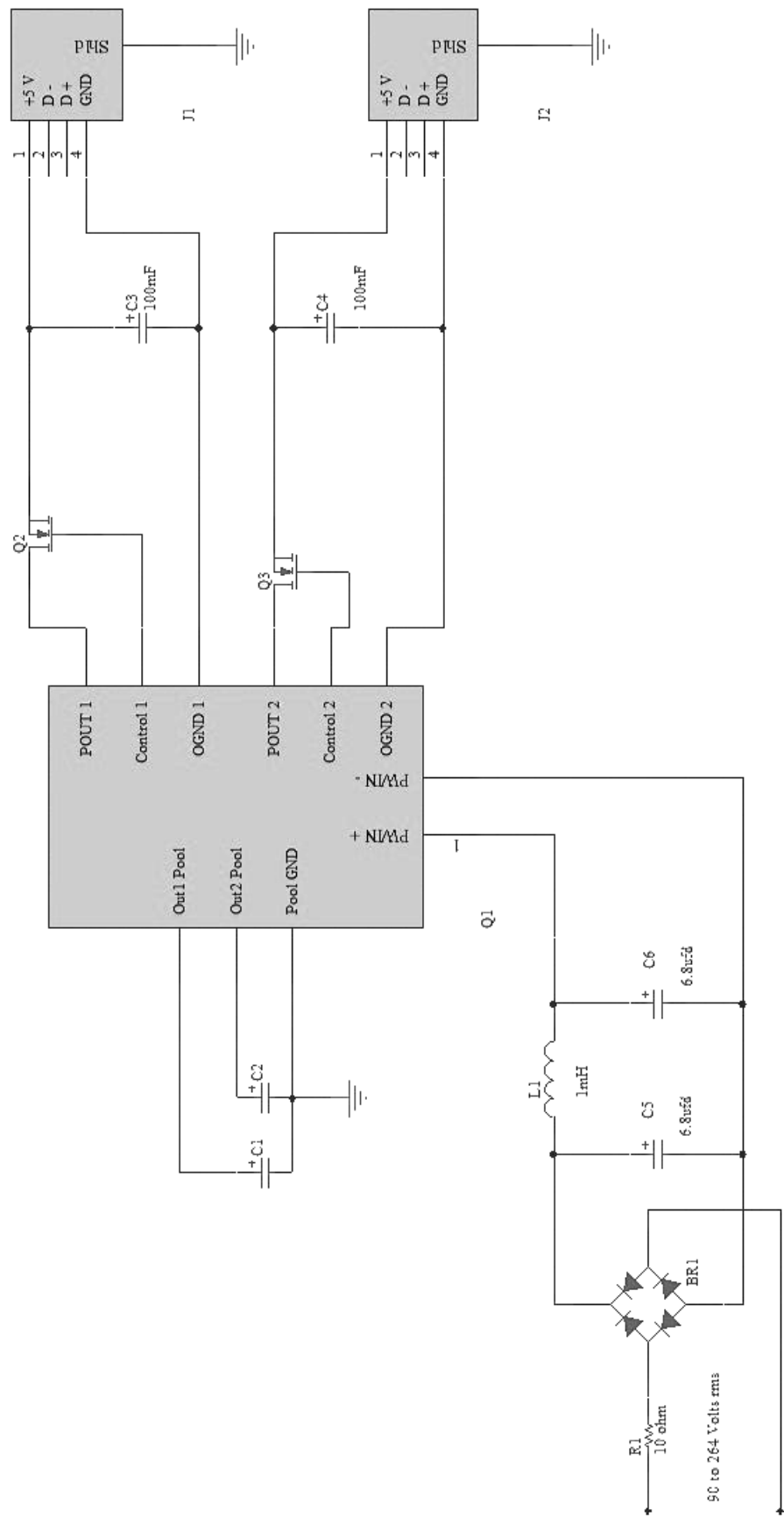


FIG. 23

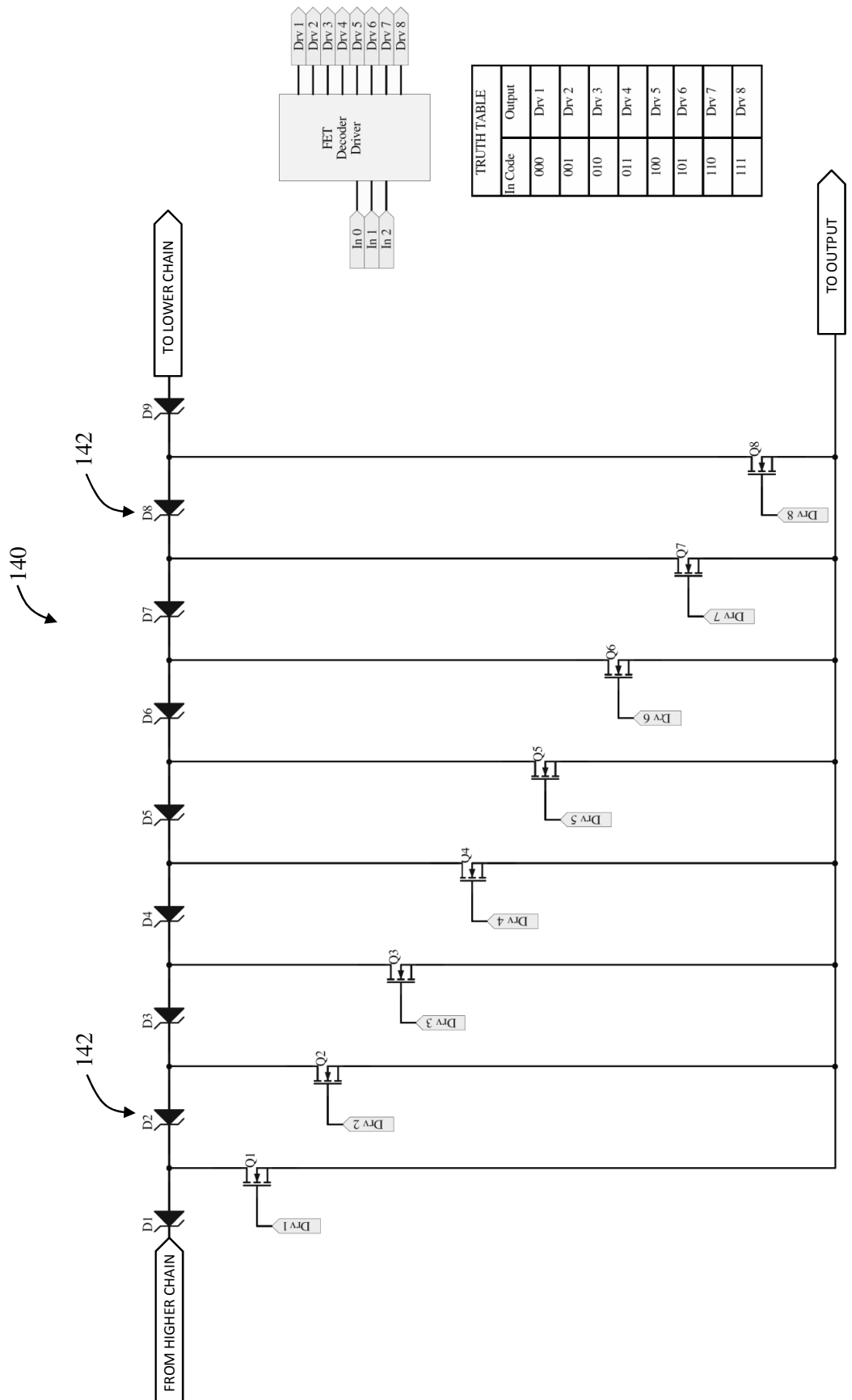


FIG. 24

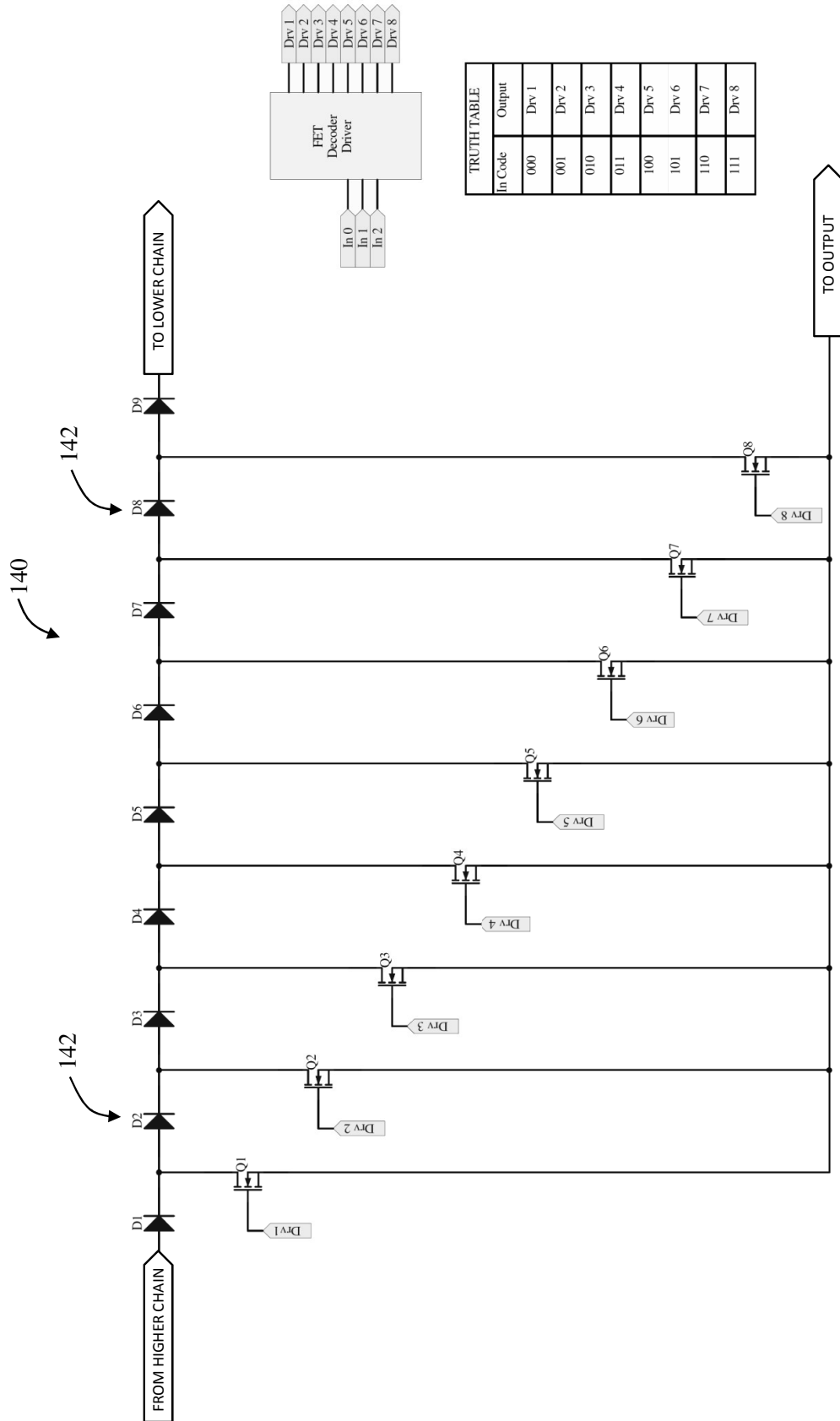


FIG. 25

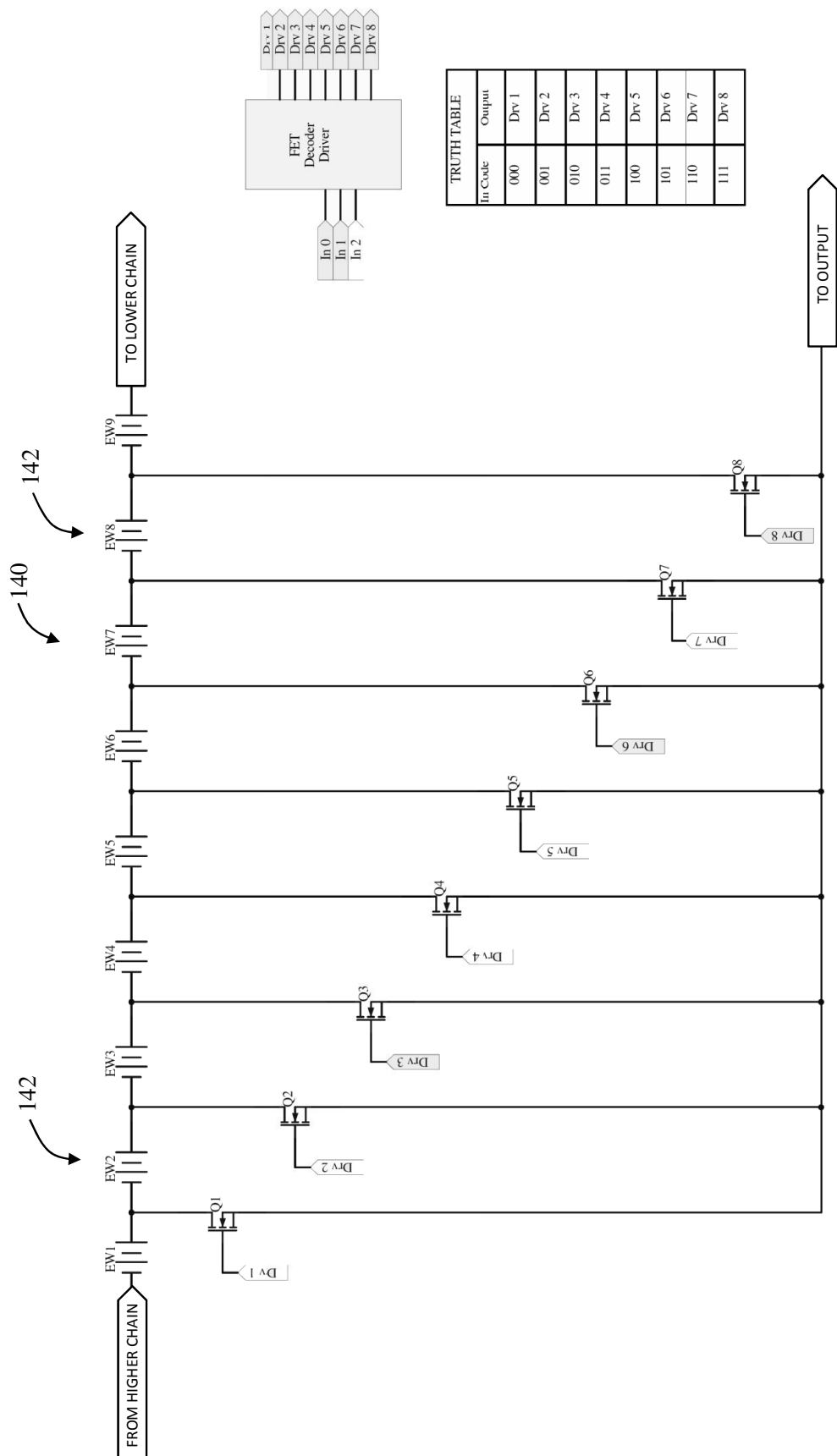
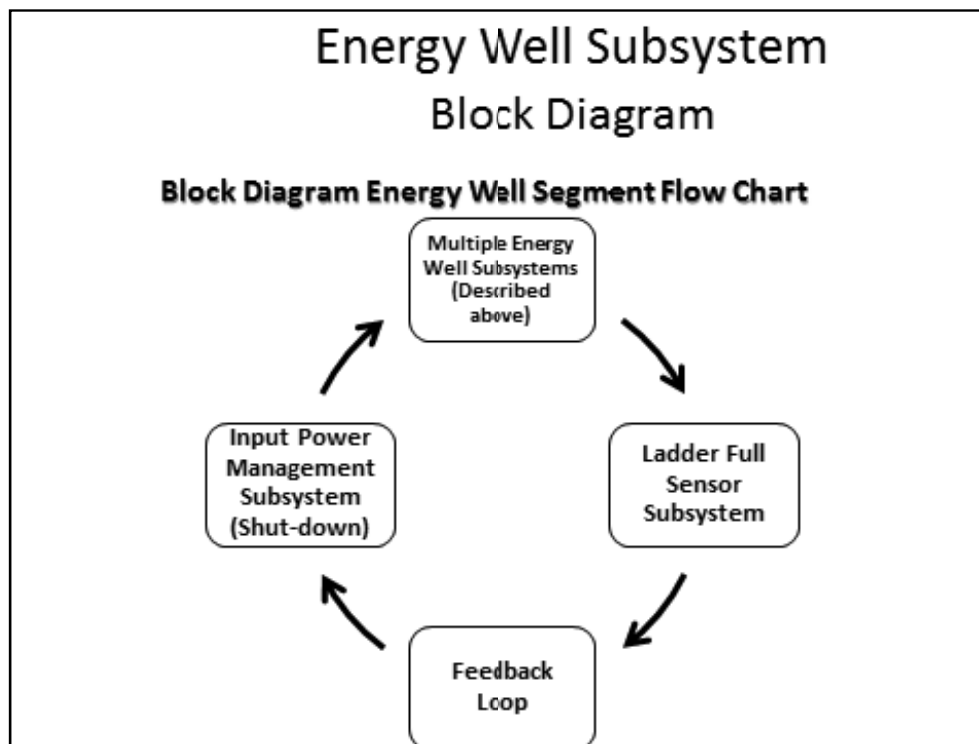
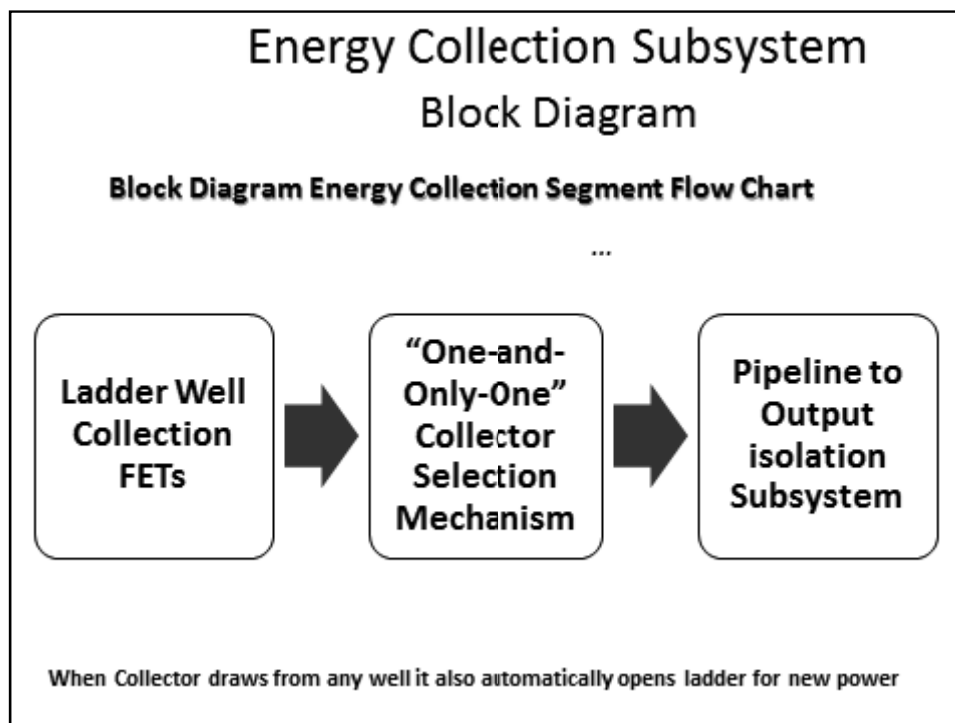


FIG. 26

**FIG. 27****FIG. 28**

Output Isolation Subsystem Schematic

Total isolation between input power & each of the outputs required

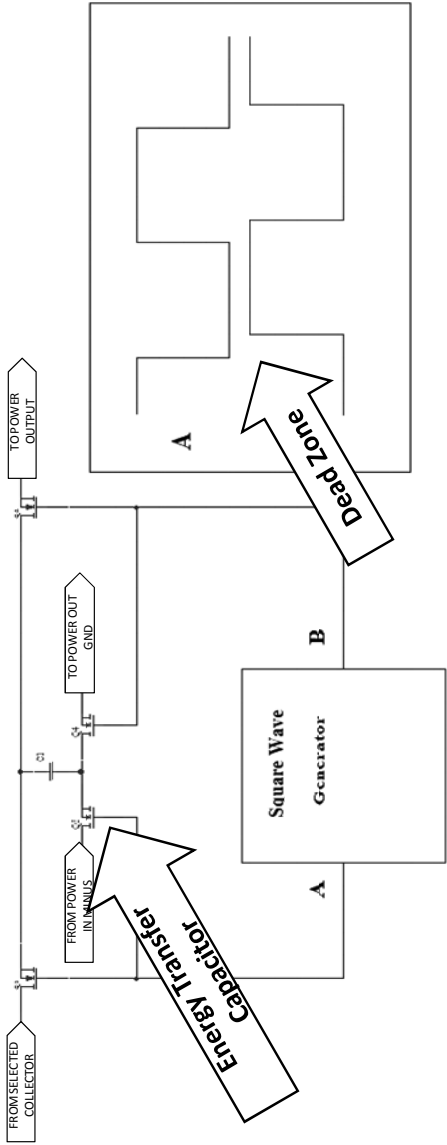


FIG. 29

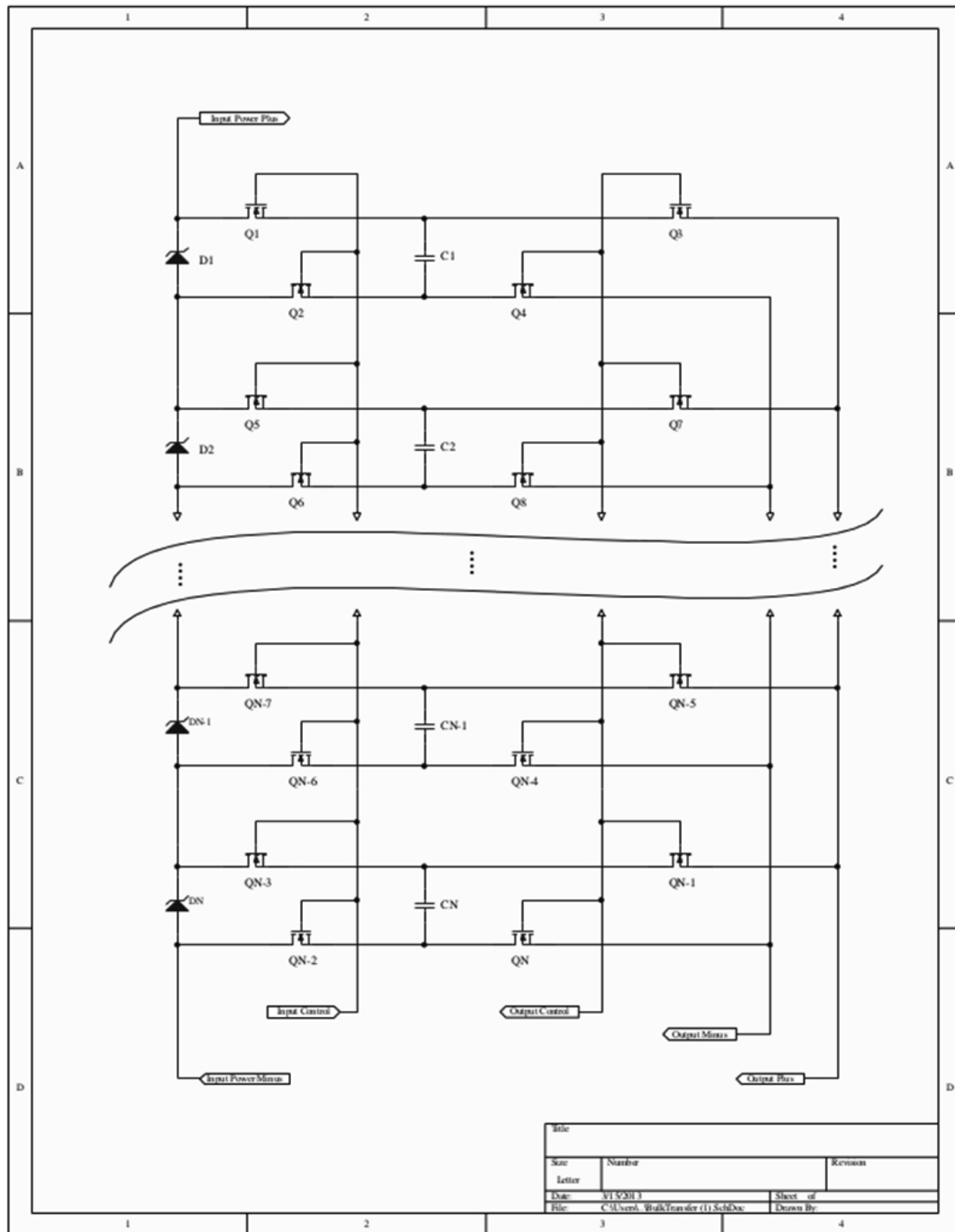


FIG. 30

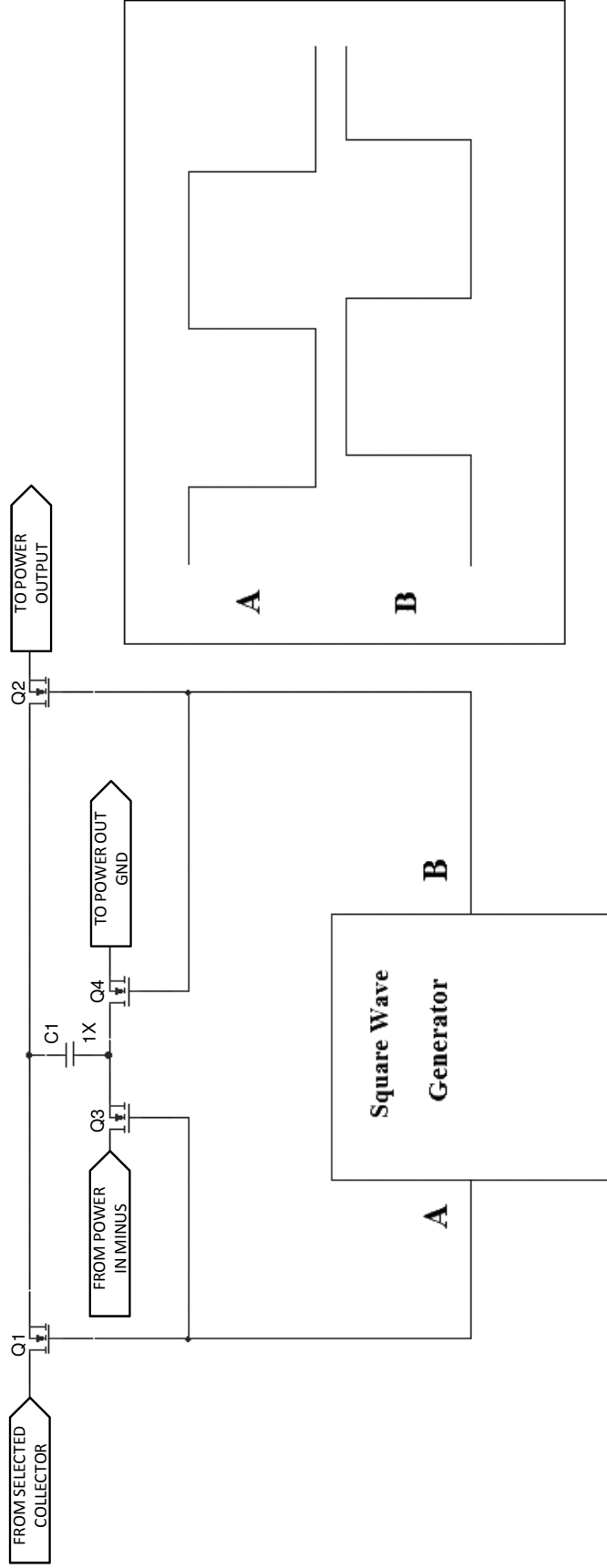


FIG. 31a

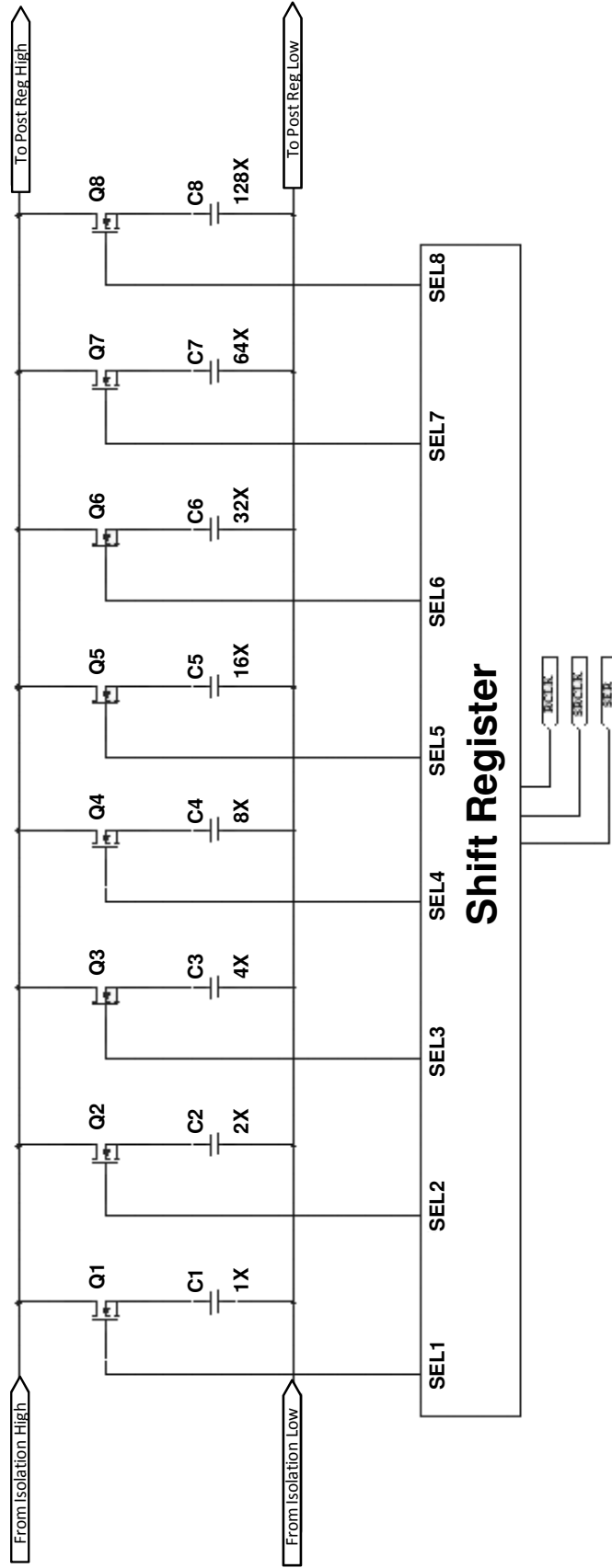


FIG. 31b

FUNCTION TABLE

INPUTS			FUNCTION
SER	SRCLK	RCLK	
L	↑	X	First stage of the shift register goes low. Other stages store the data of previous stage, respectively.
H	↑	X	First stage of the shift register goes high. Other stages store the data of previous stage, respectively.
X	X	↑	Shift-register data is stored in the storage register.

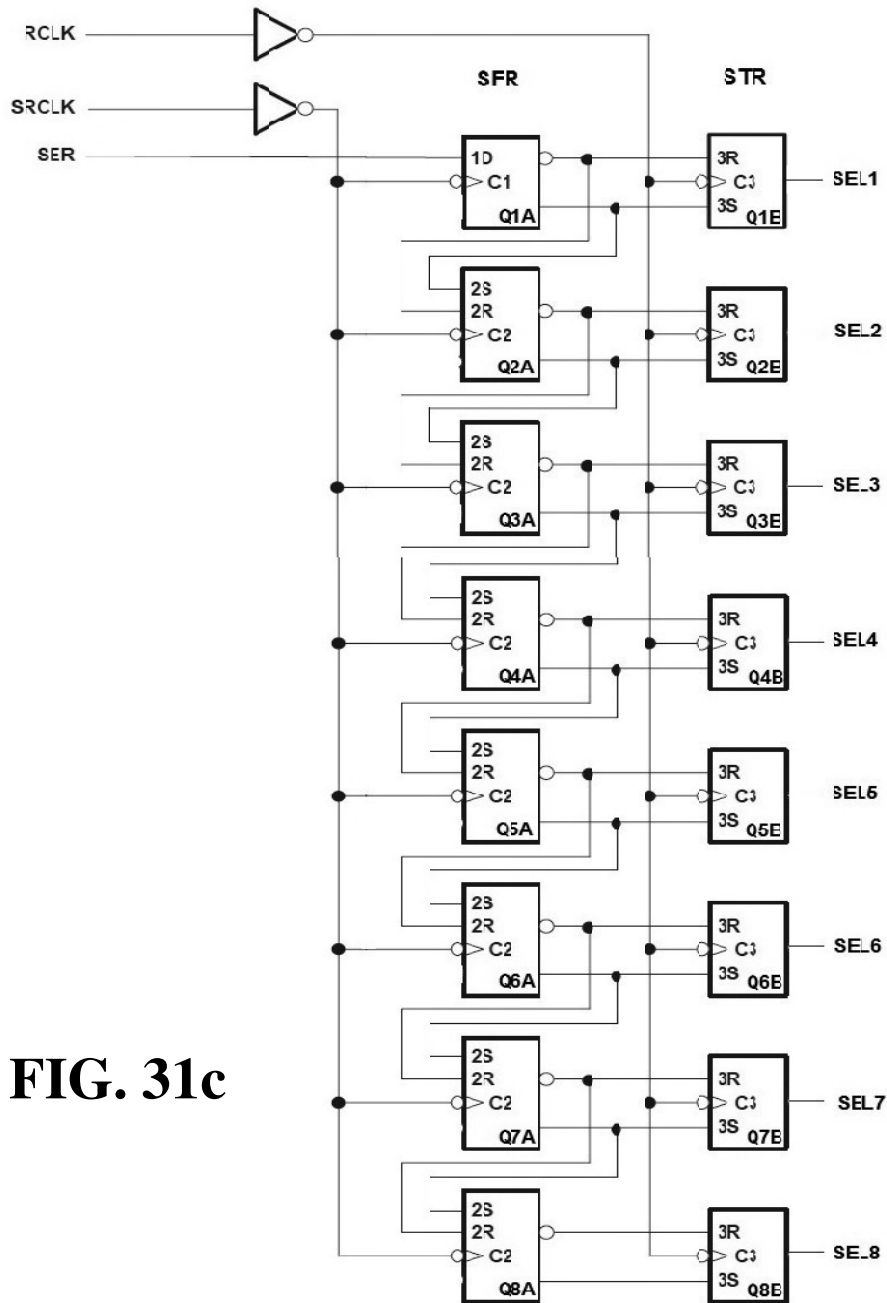
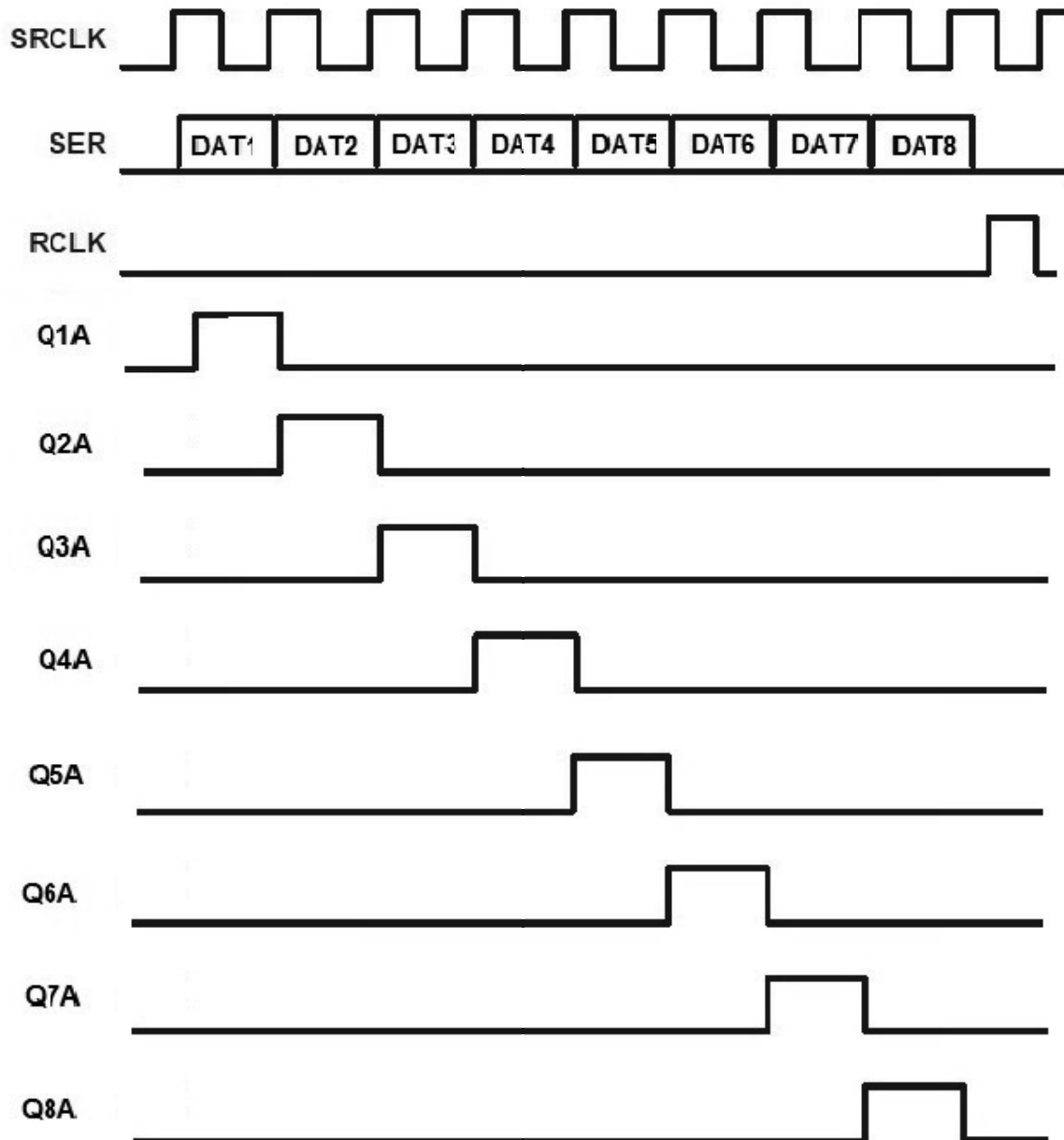
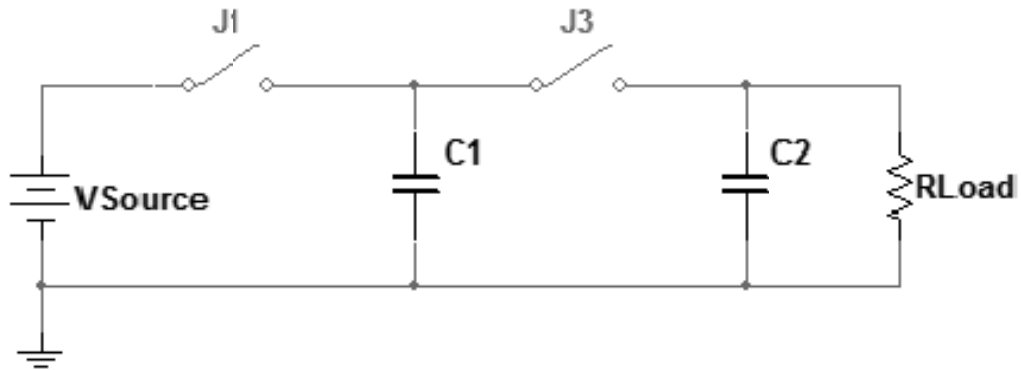
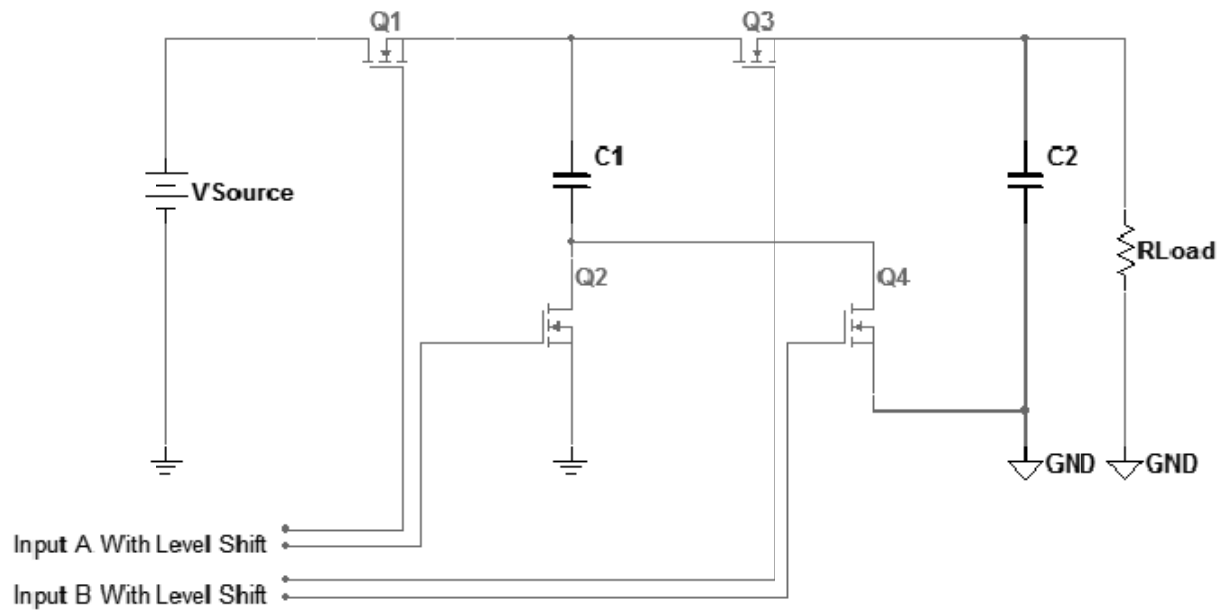


FIG. 31c

SHIFT REGISTER

timing diagram

**FIG. 31d**

**FIG. 32a****FIG. 32b**

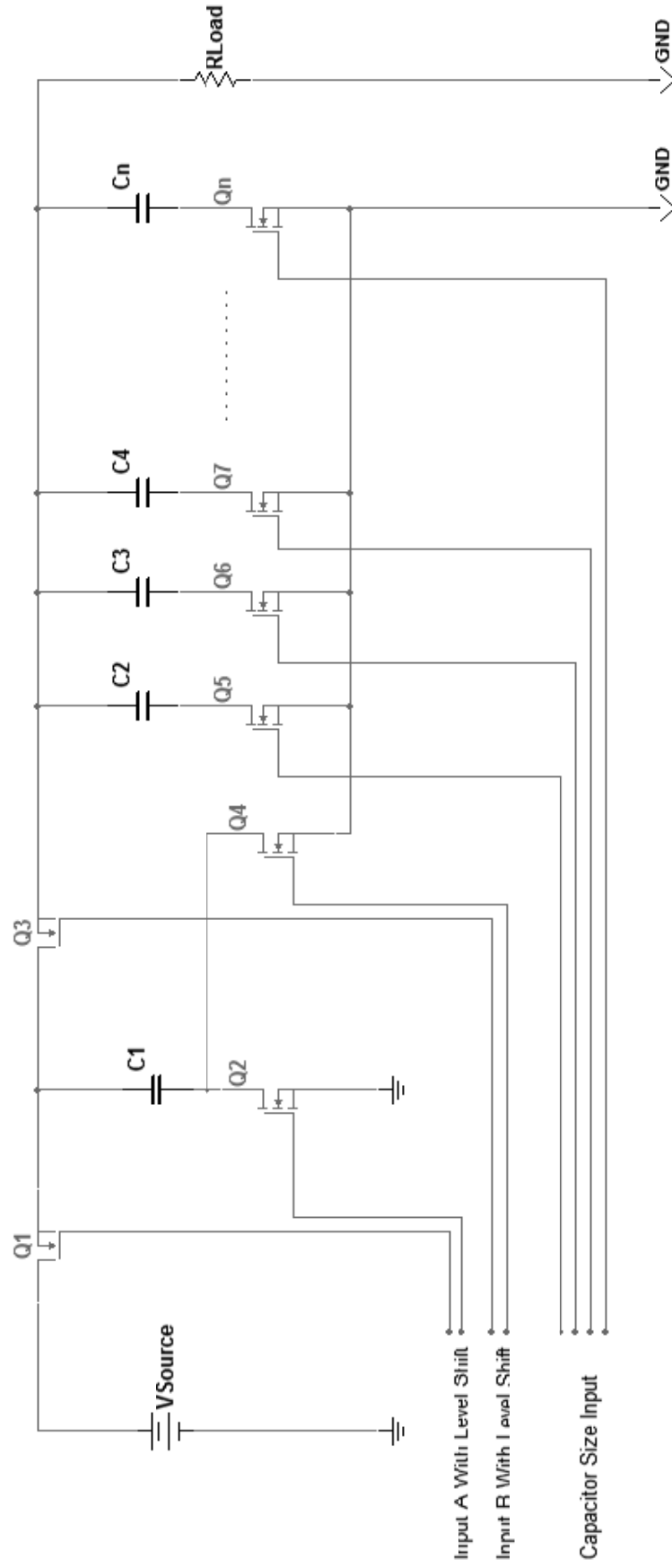


FIG. 32c

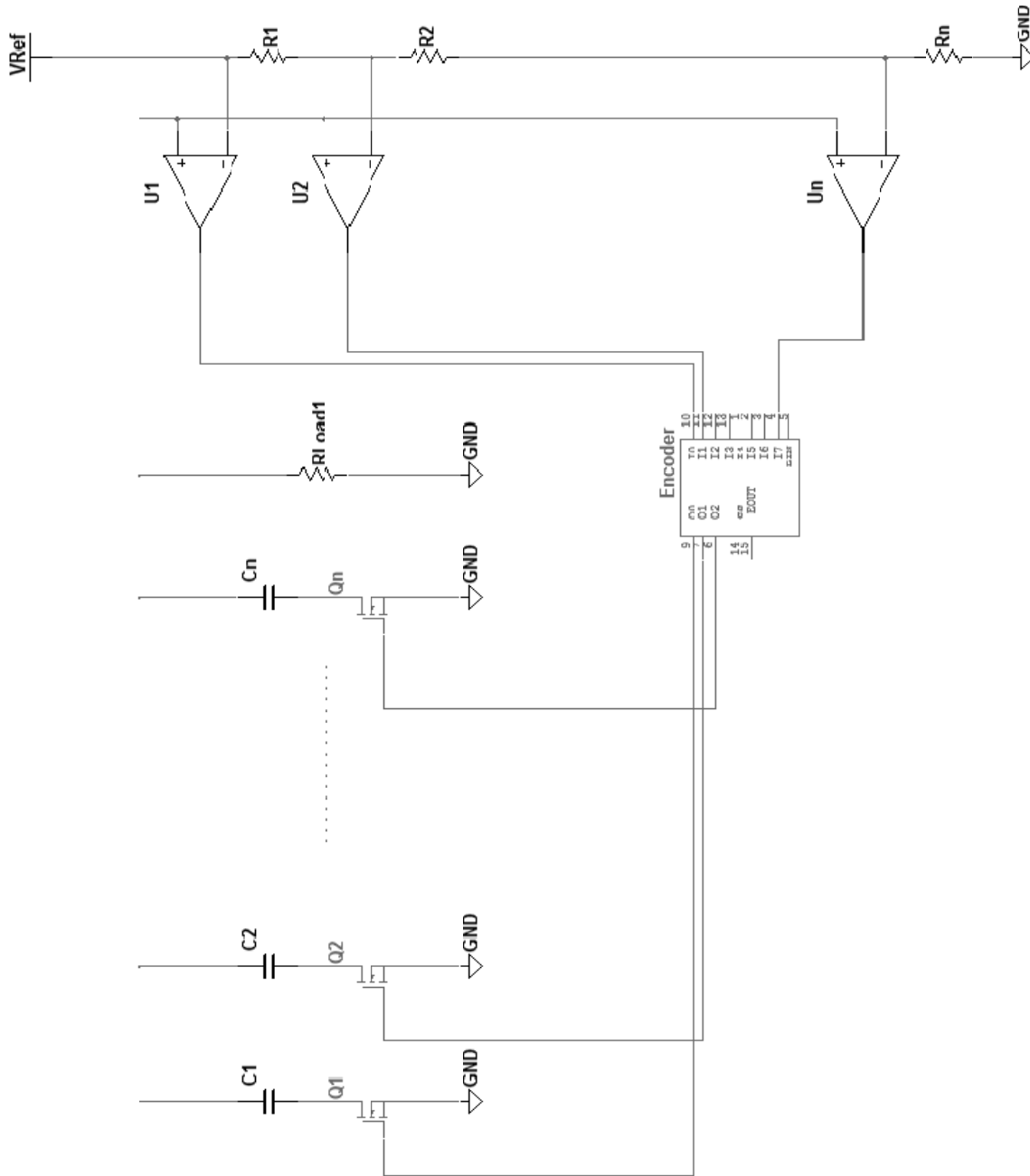


FIG. 32d

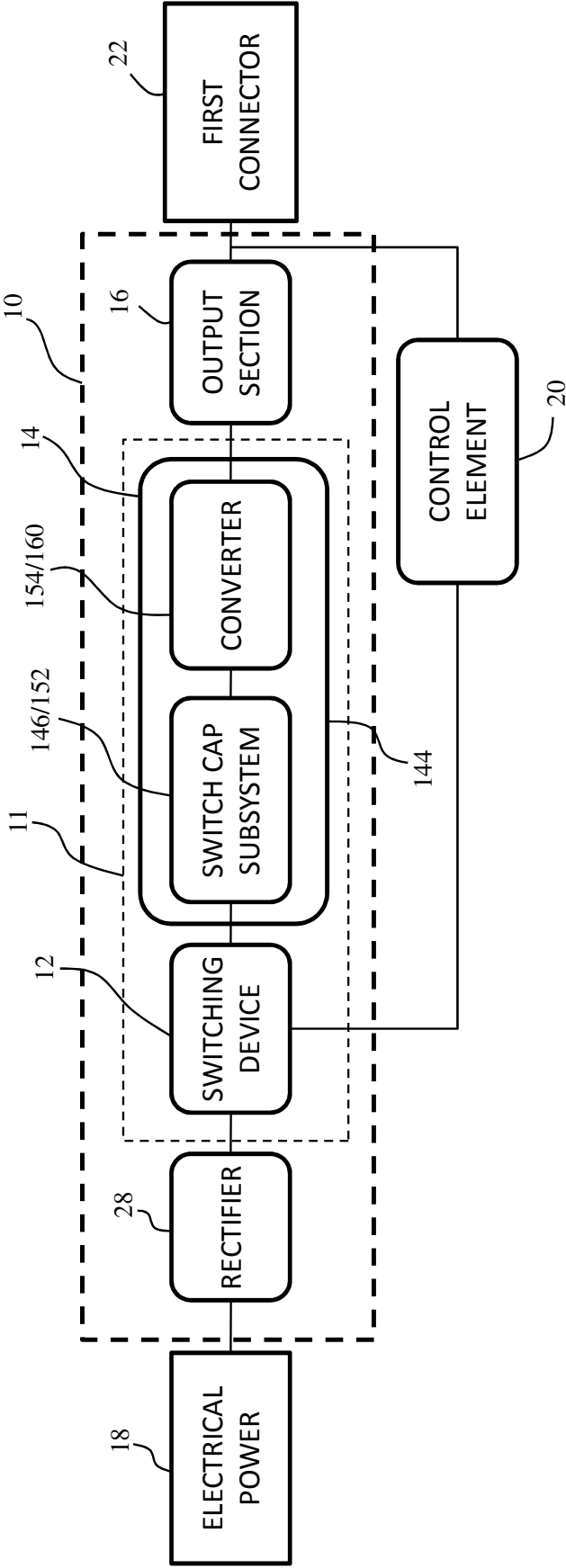


FIG. 33

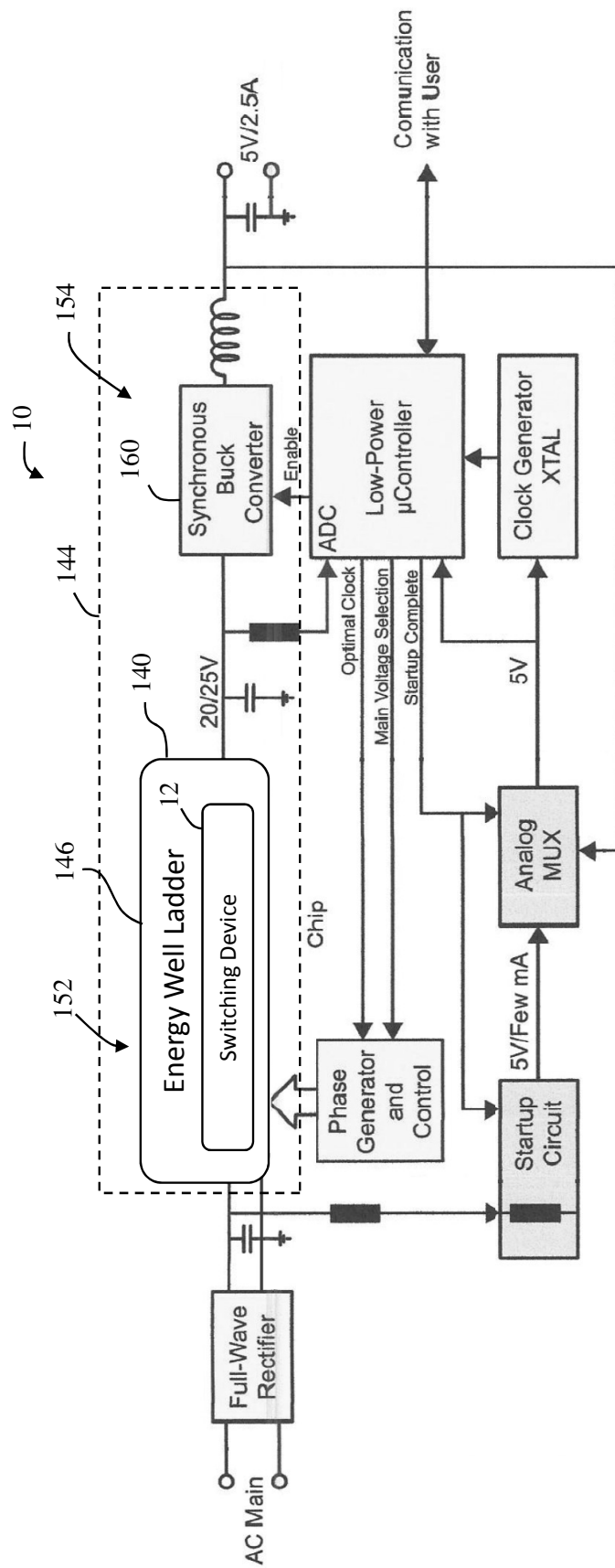
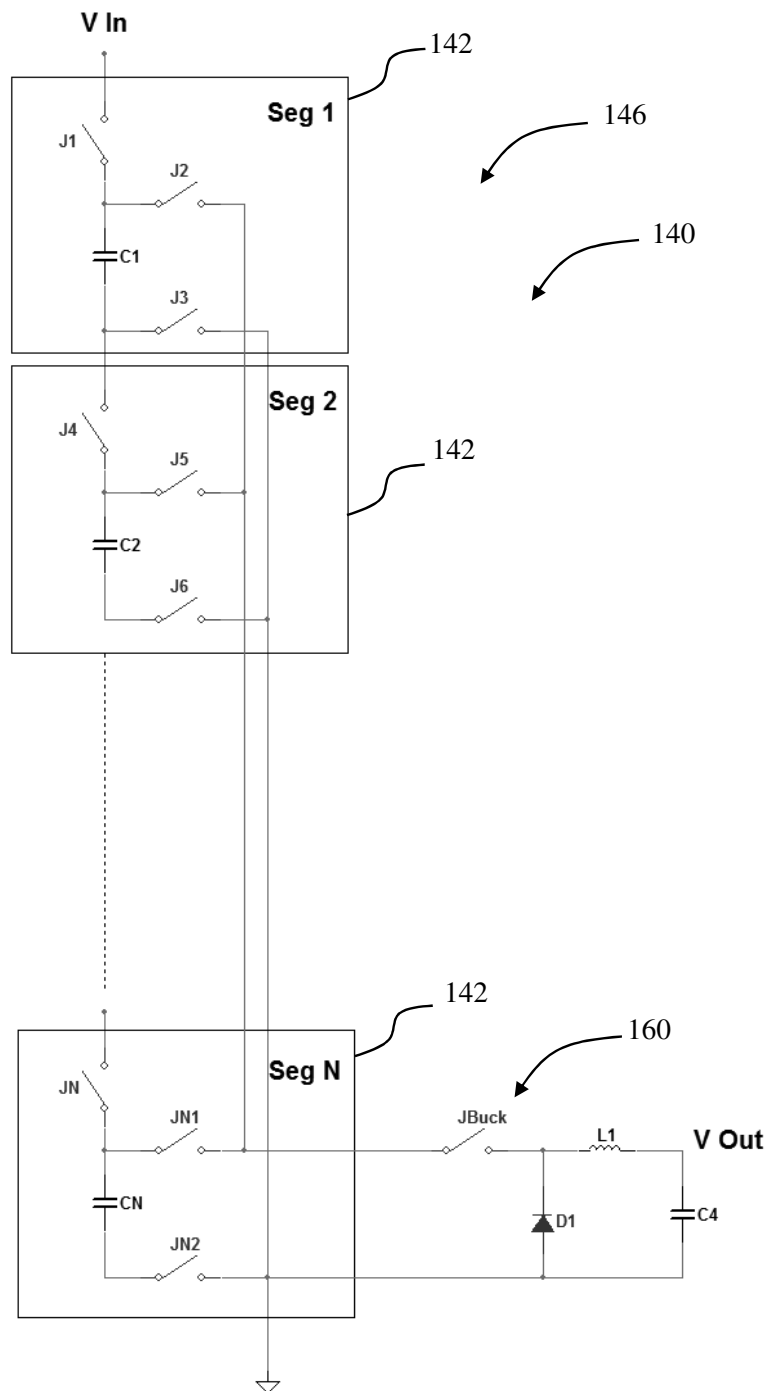


FIG. 34a



Switched N-Capacitor Ladder with Buck Output

FIG. 34b

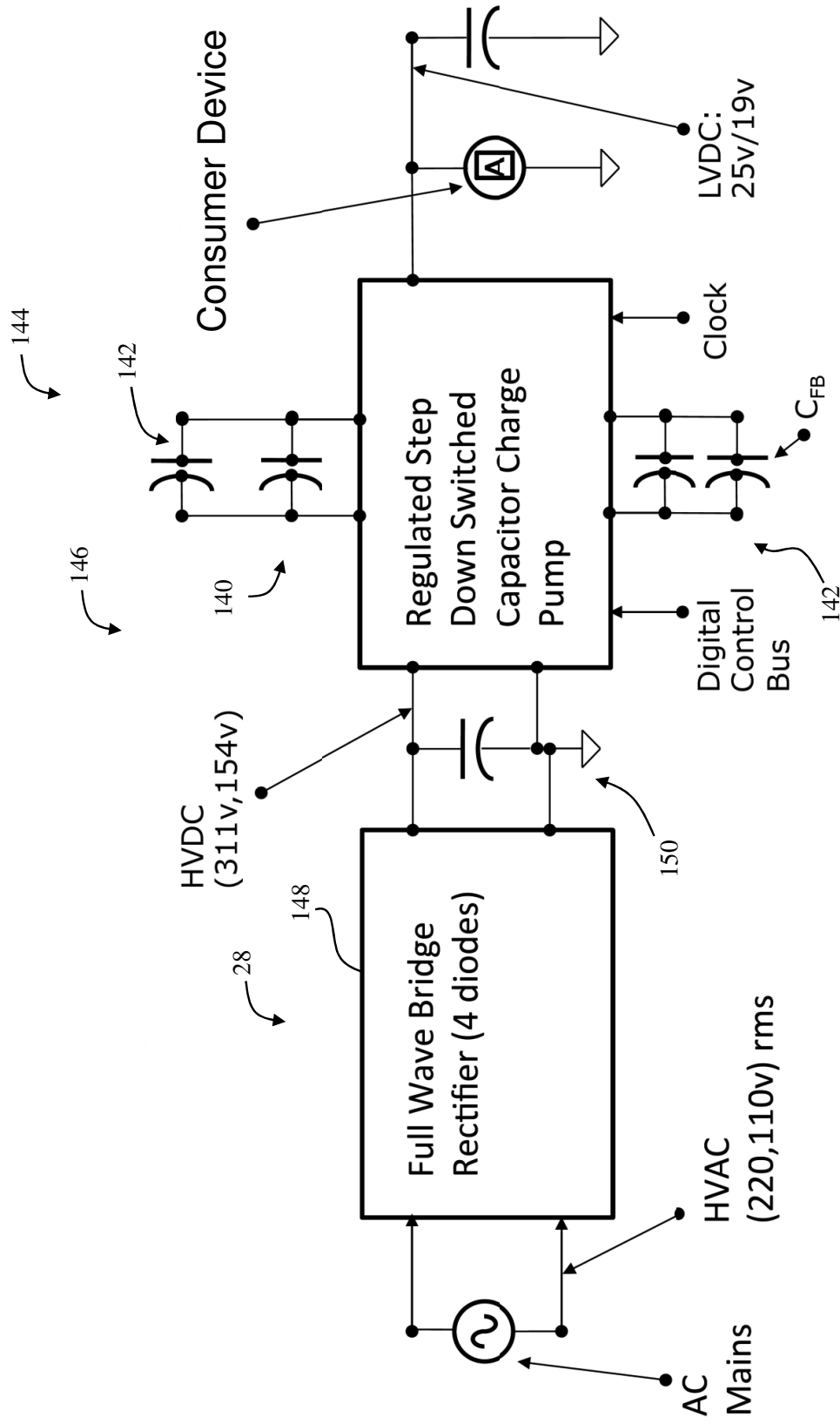
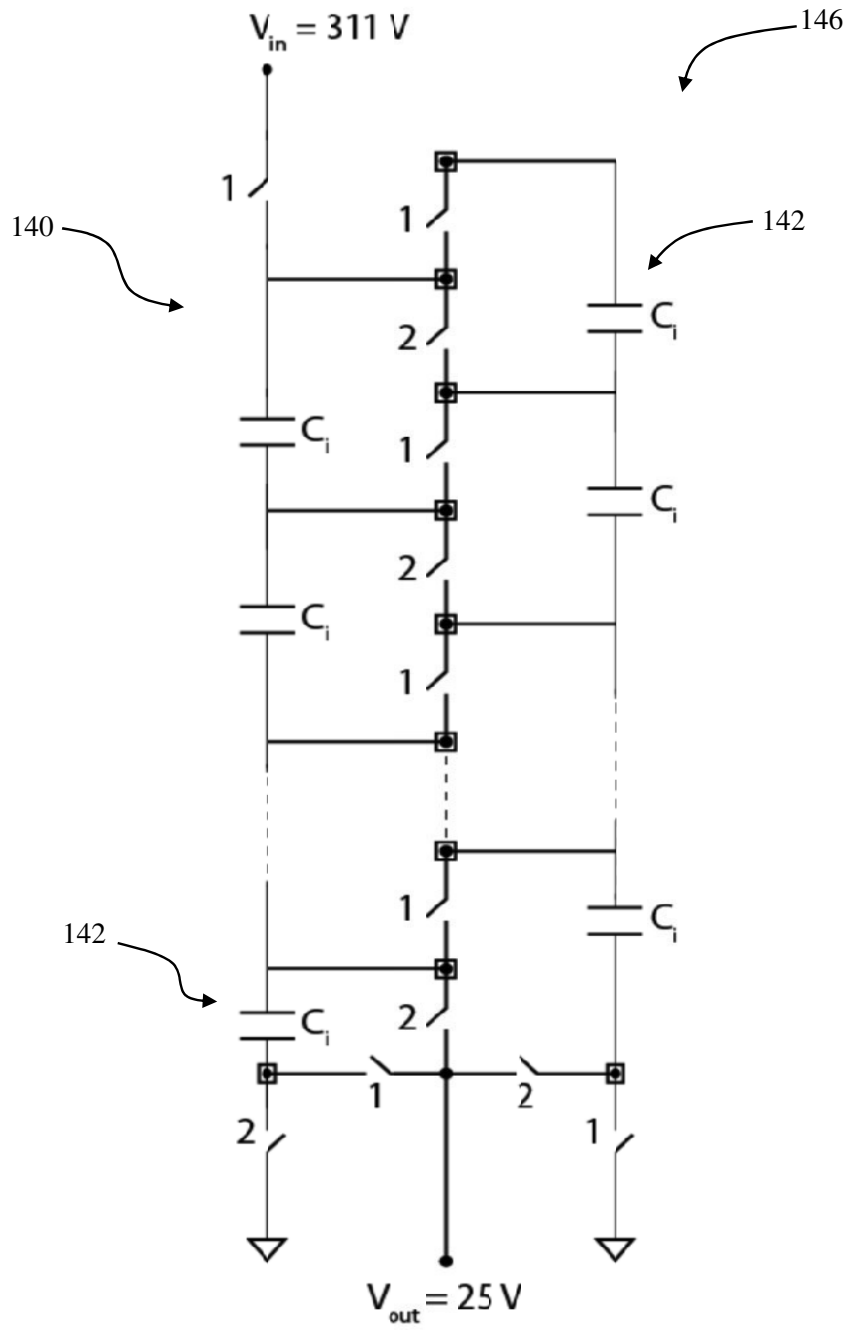


FIG. 35

**FIG. 36**

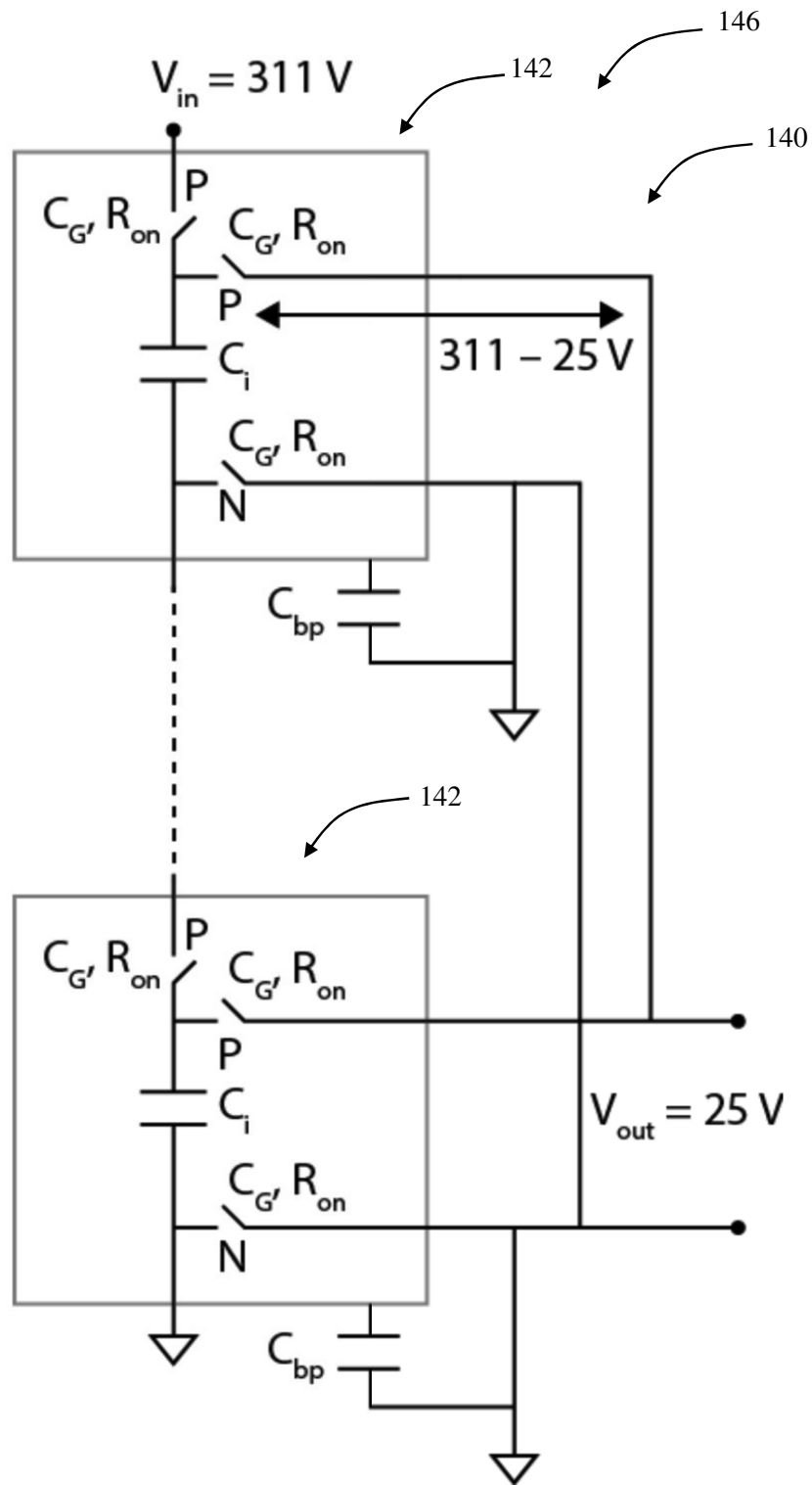


FIG. 37

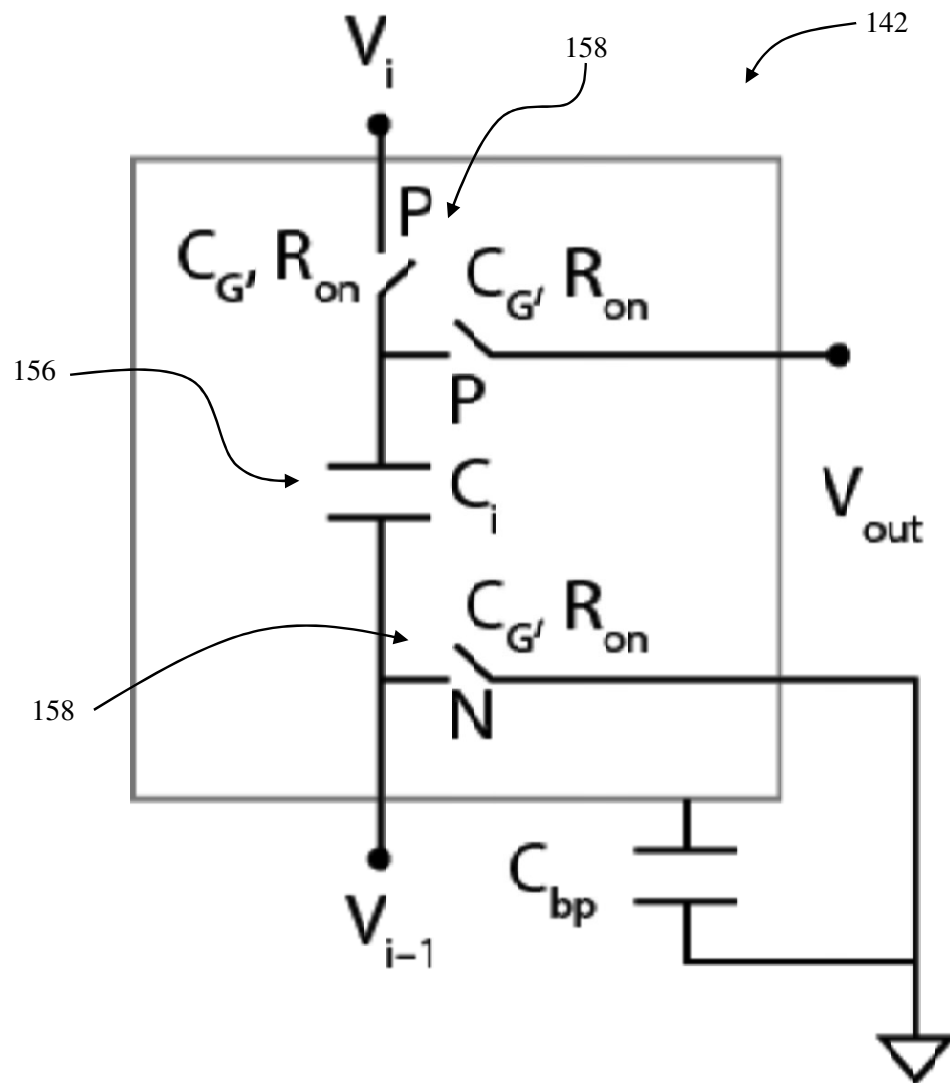


FIG. 38

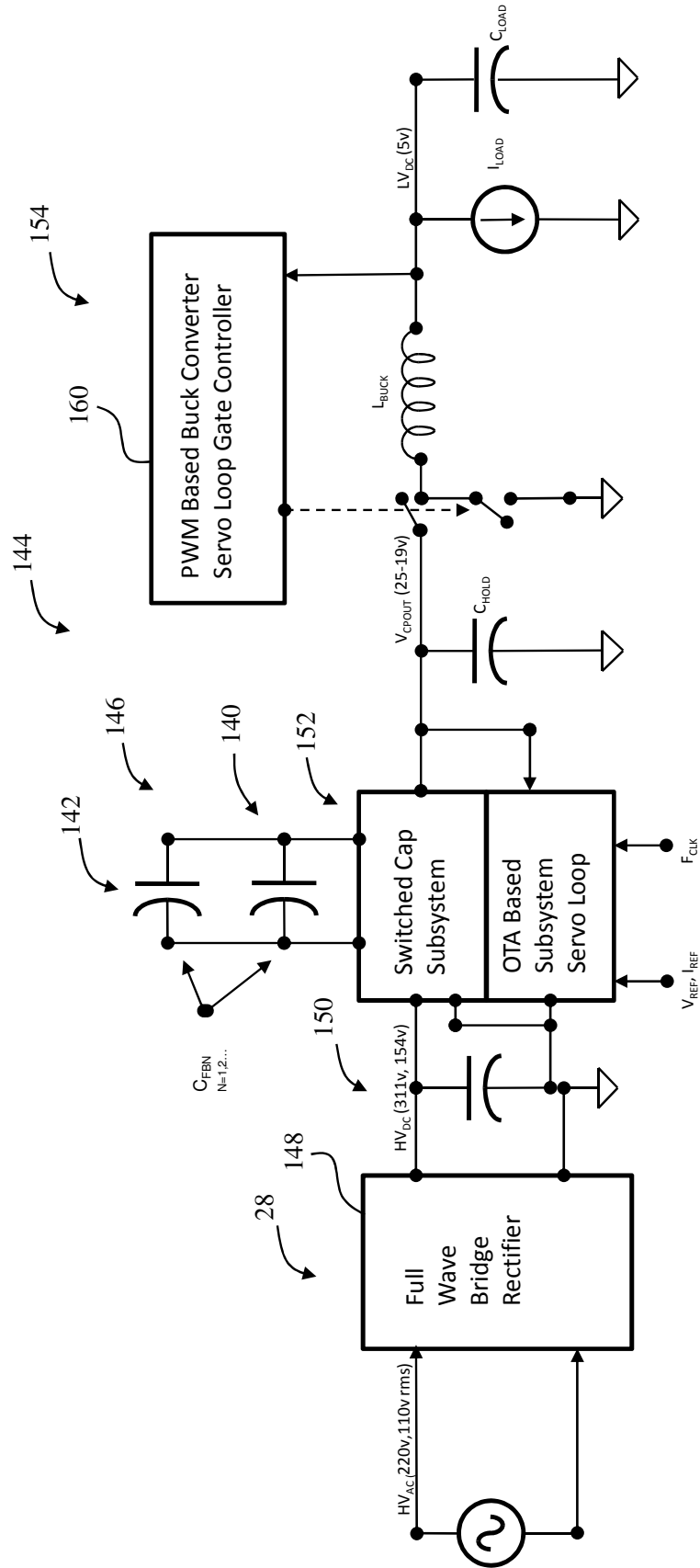


FIG. 39

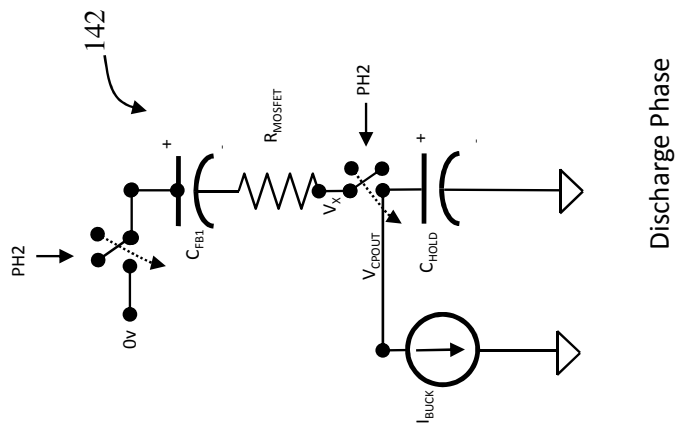


FIG. 41

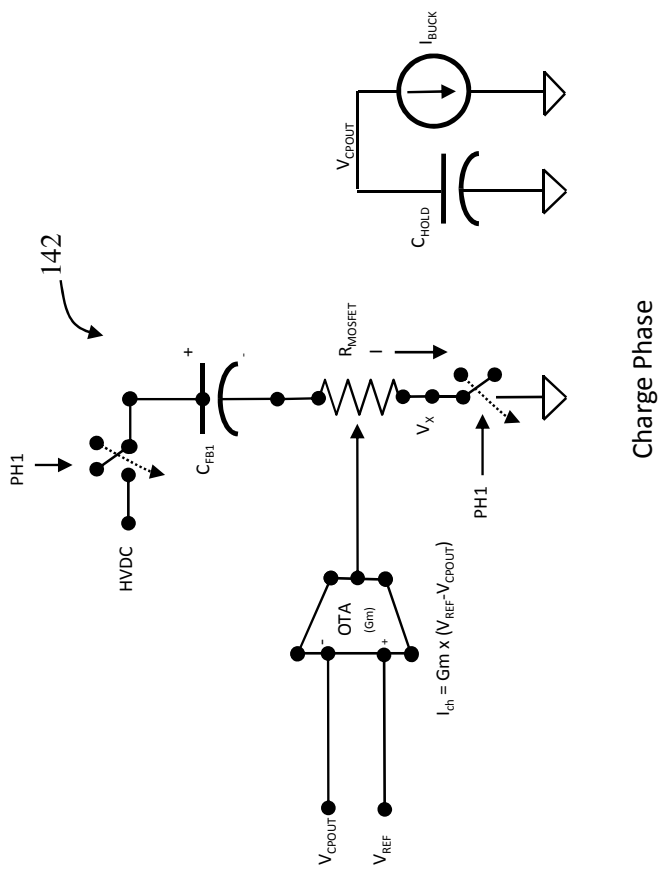
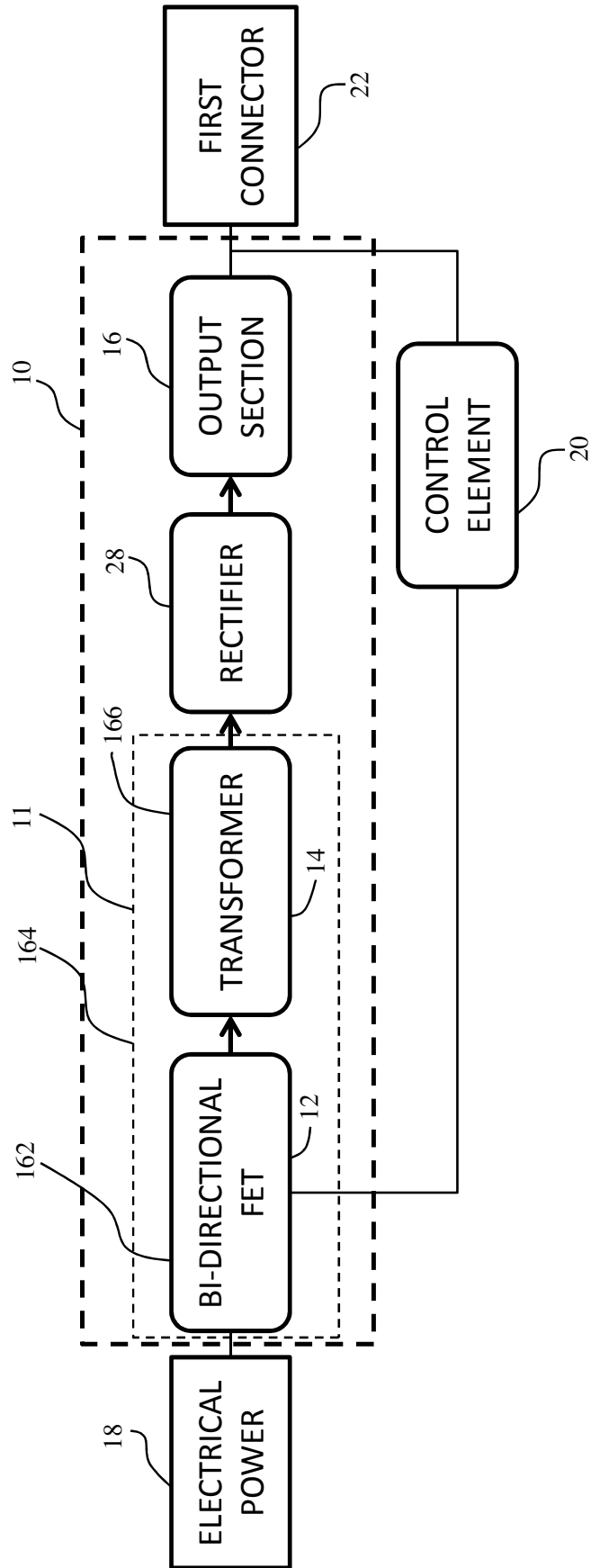
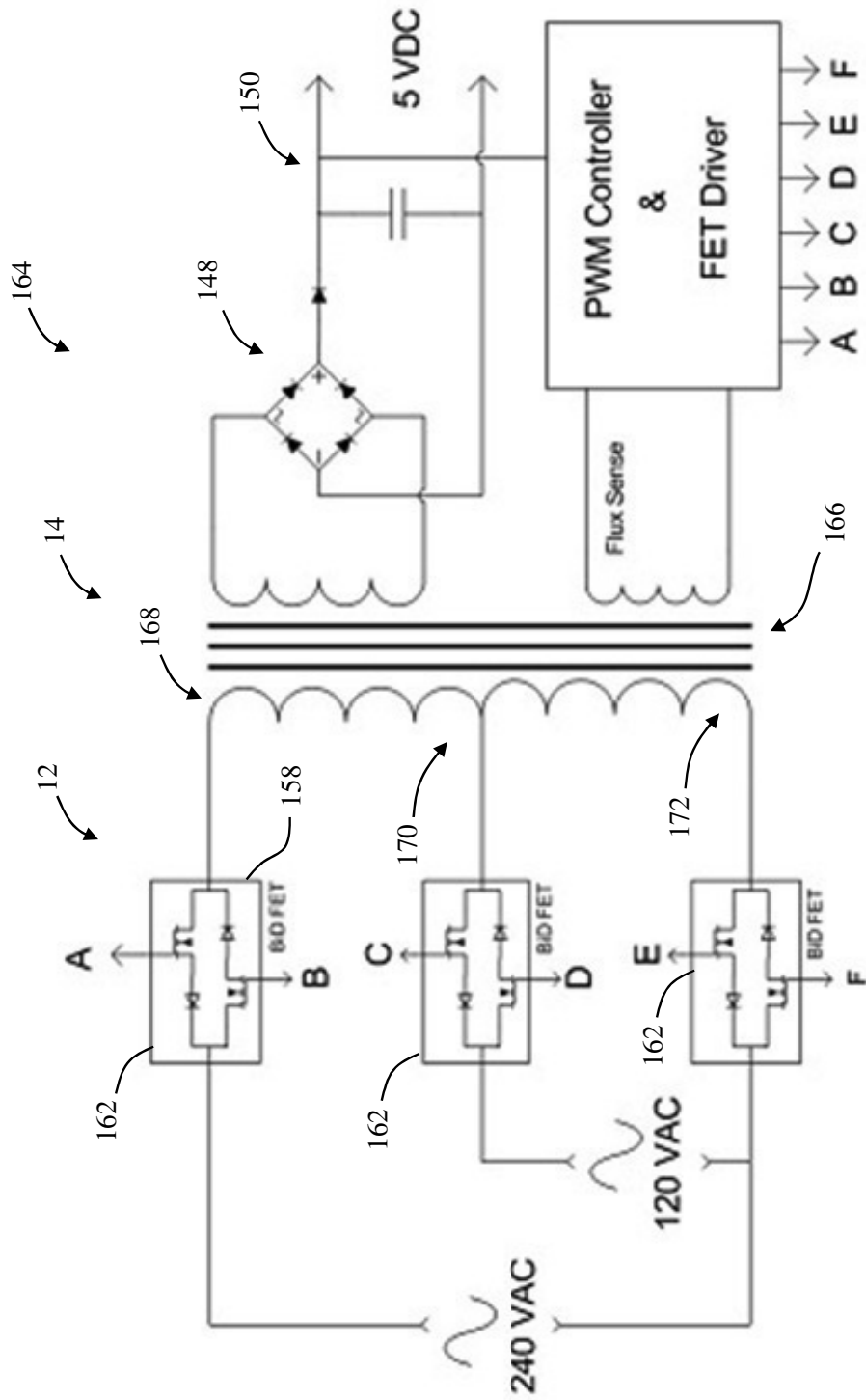


FIG. 40

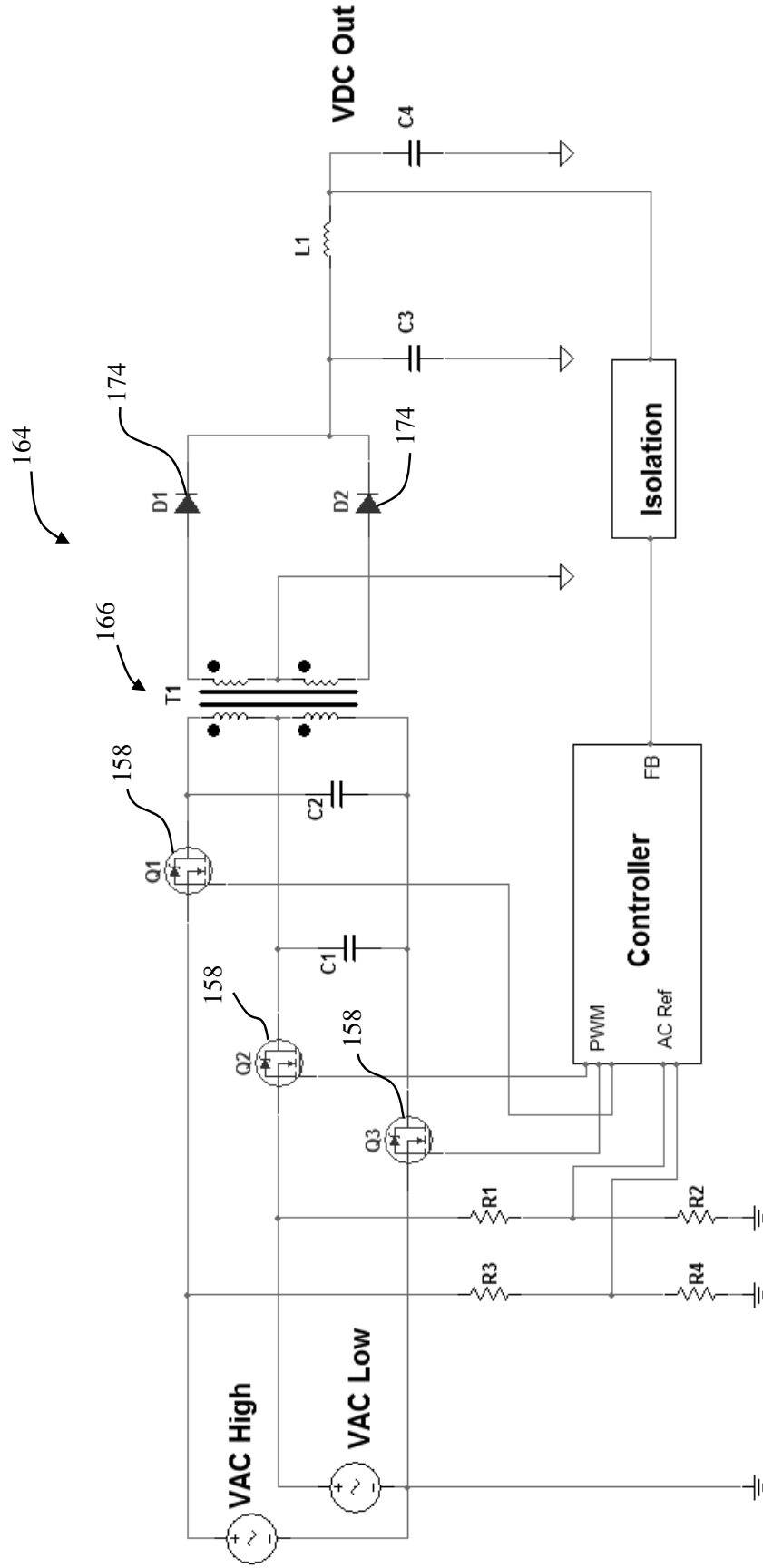
**FIG. 42**

Three (3) BiDFET Power Circuitry Diagram



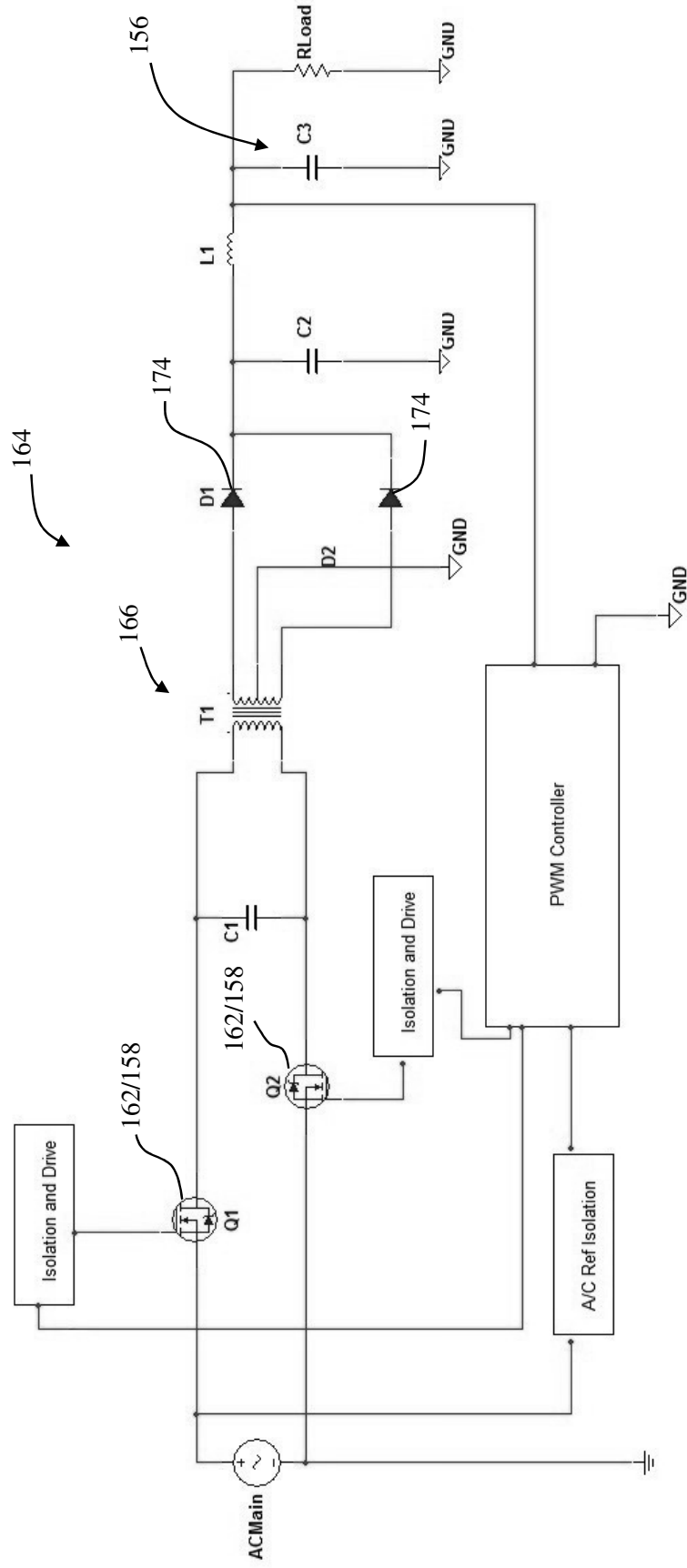
BiD FET = Bi-Directional
Field Effect Transistor

FIG. 44a



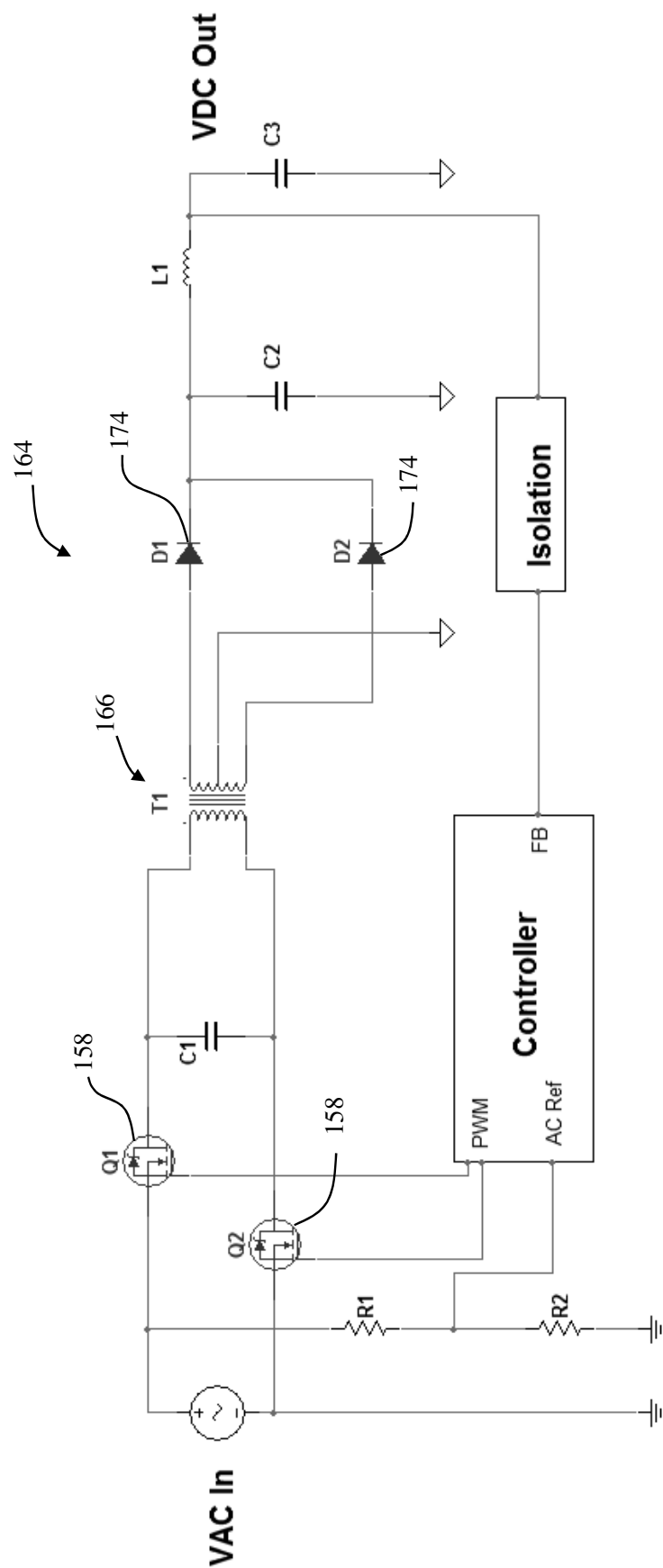
BiDFET Converter With Multi-Tap Transformer

FIG. 44b



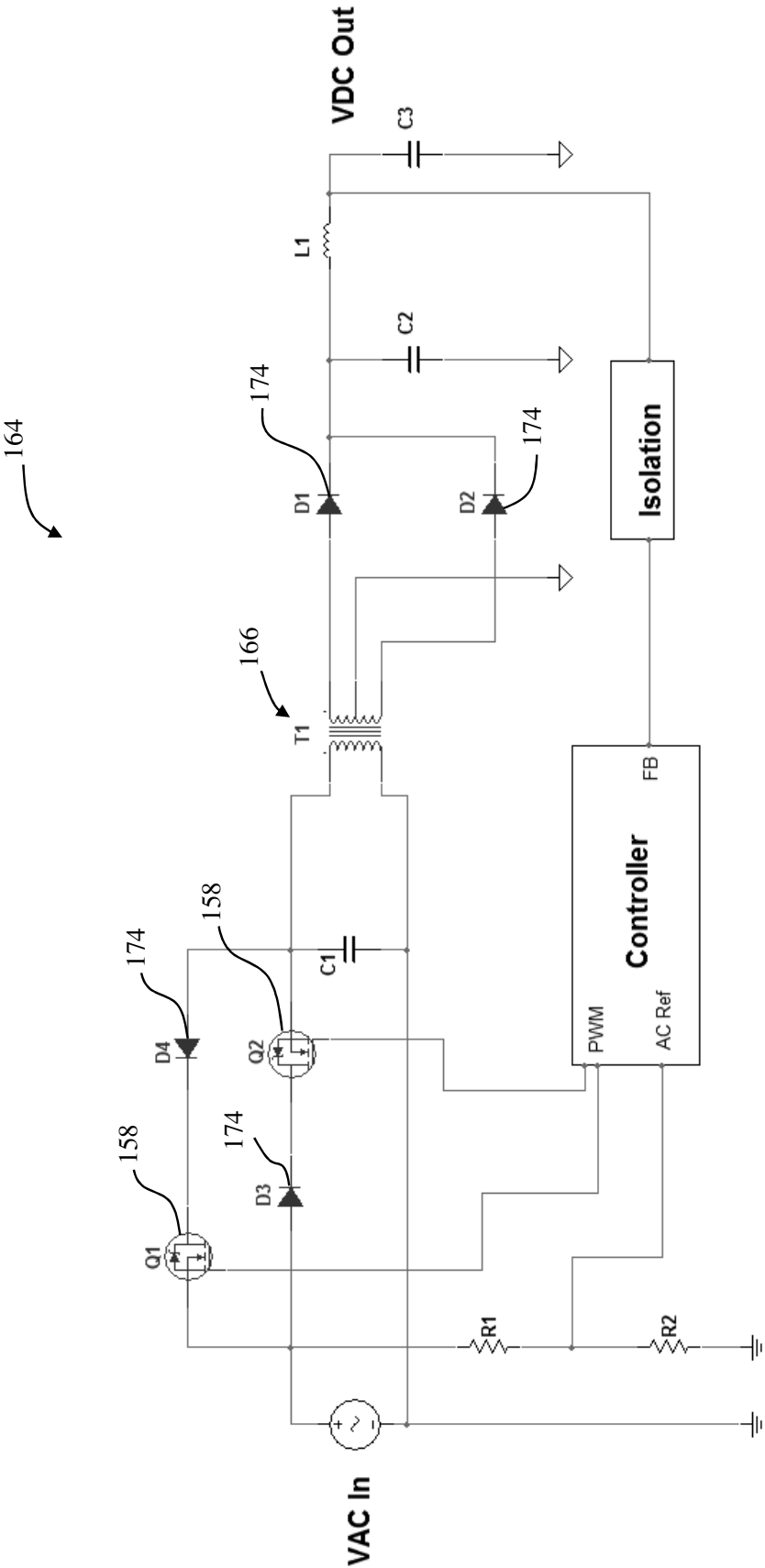
BiDFET with FET Source Connected to AC Main, Asynchronous Secondary, PWM Controller Referenced to Secondary

FIG. 45a



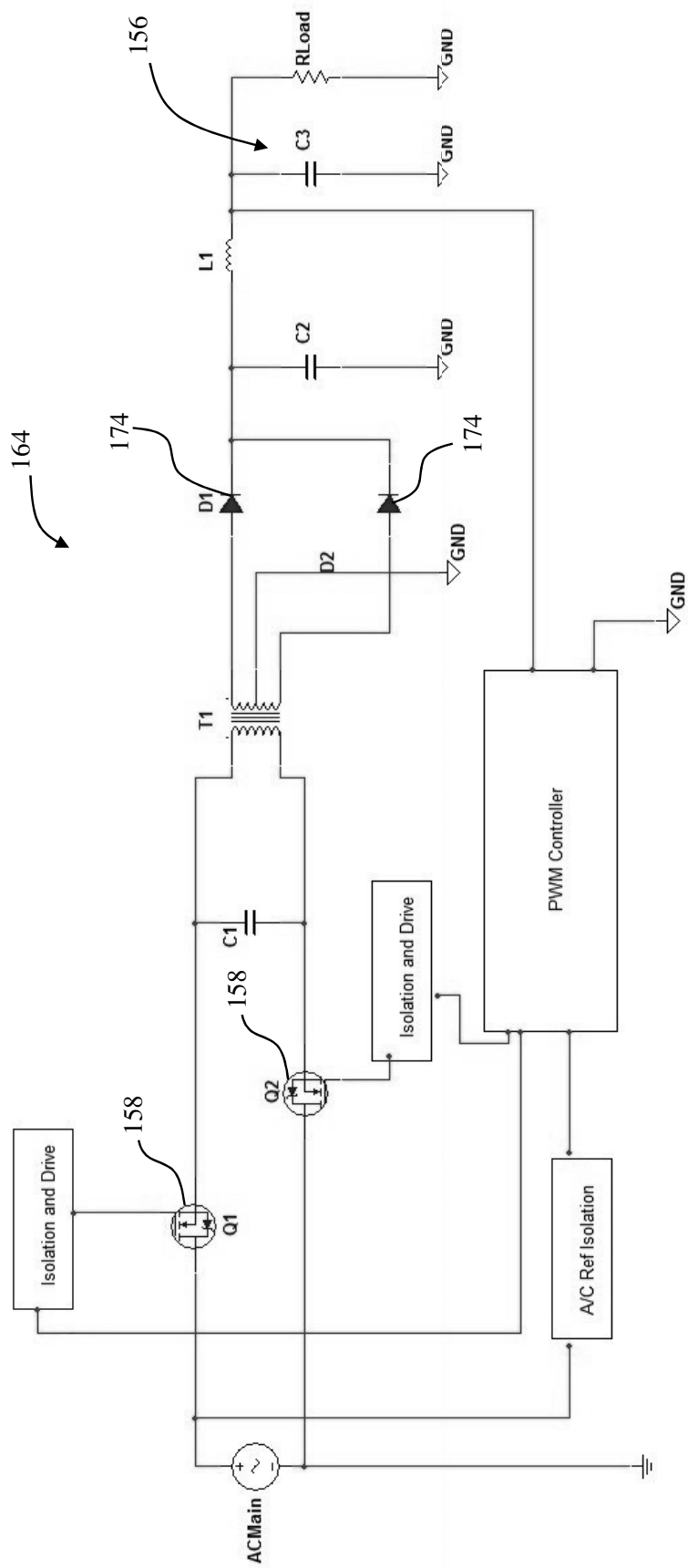
Asynchronous BiDFET with FETs Blocking Current from Transformer

FIG. 45b



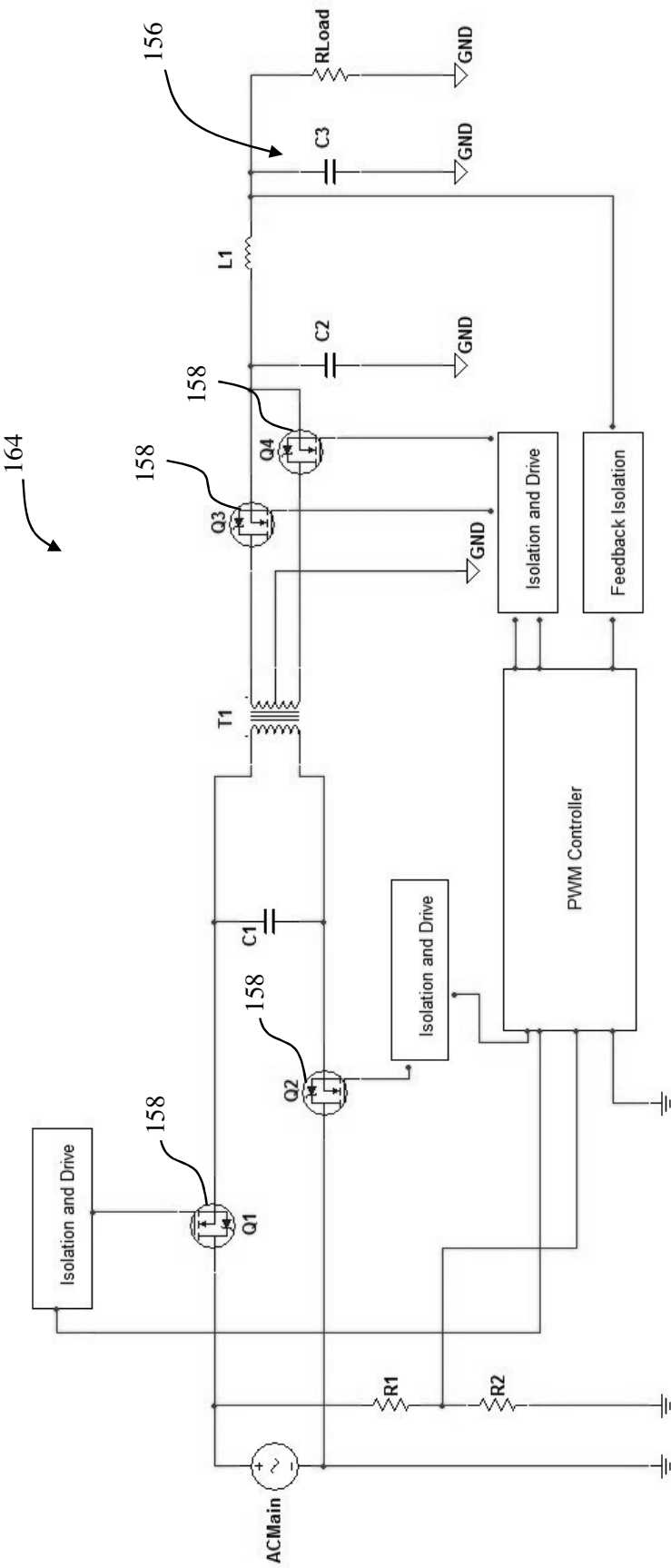
BiDFET With Single Side Switching

FIG. 45c



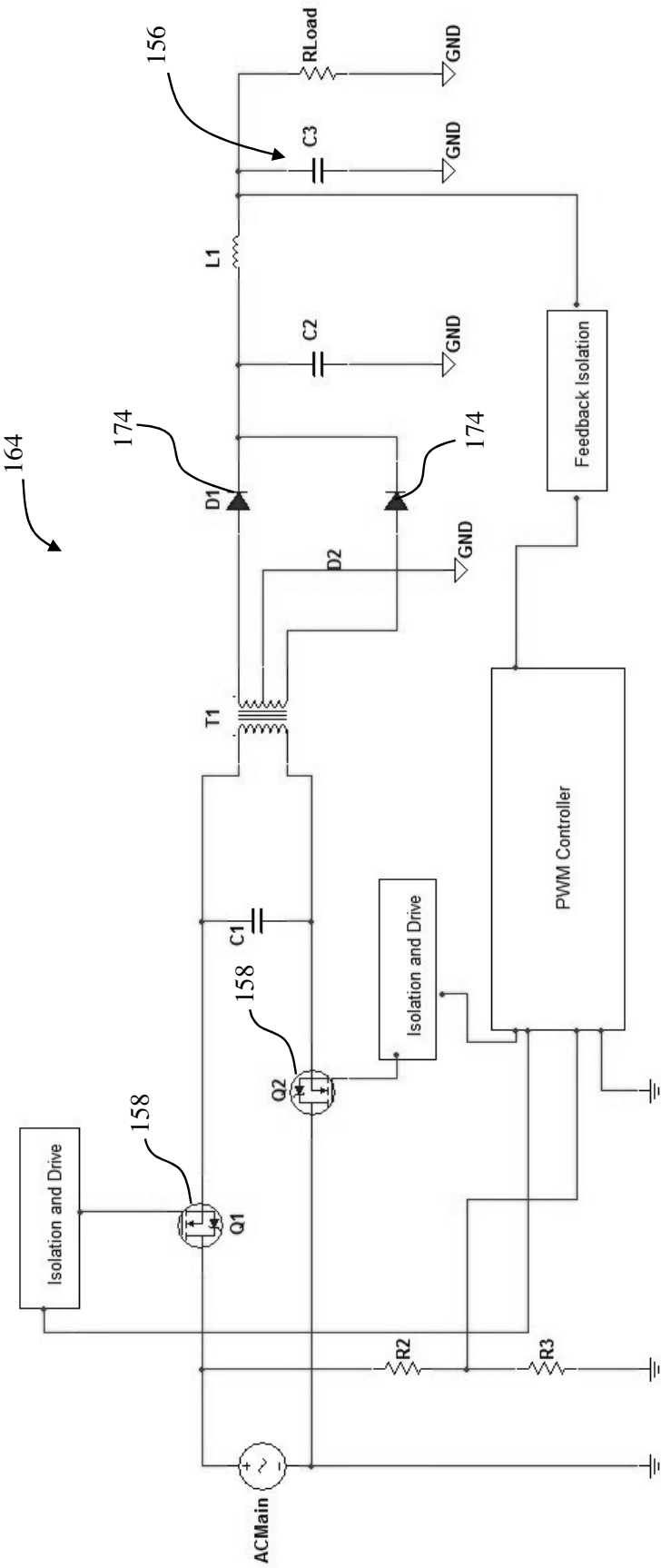
BiDFET with FET Source Connected to Transformer and PWM Controller Referenced to Asynchronous Secondary

FIG. 47



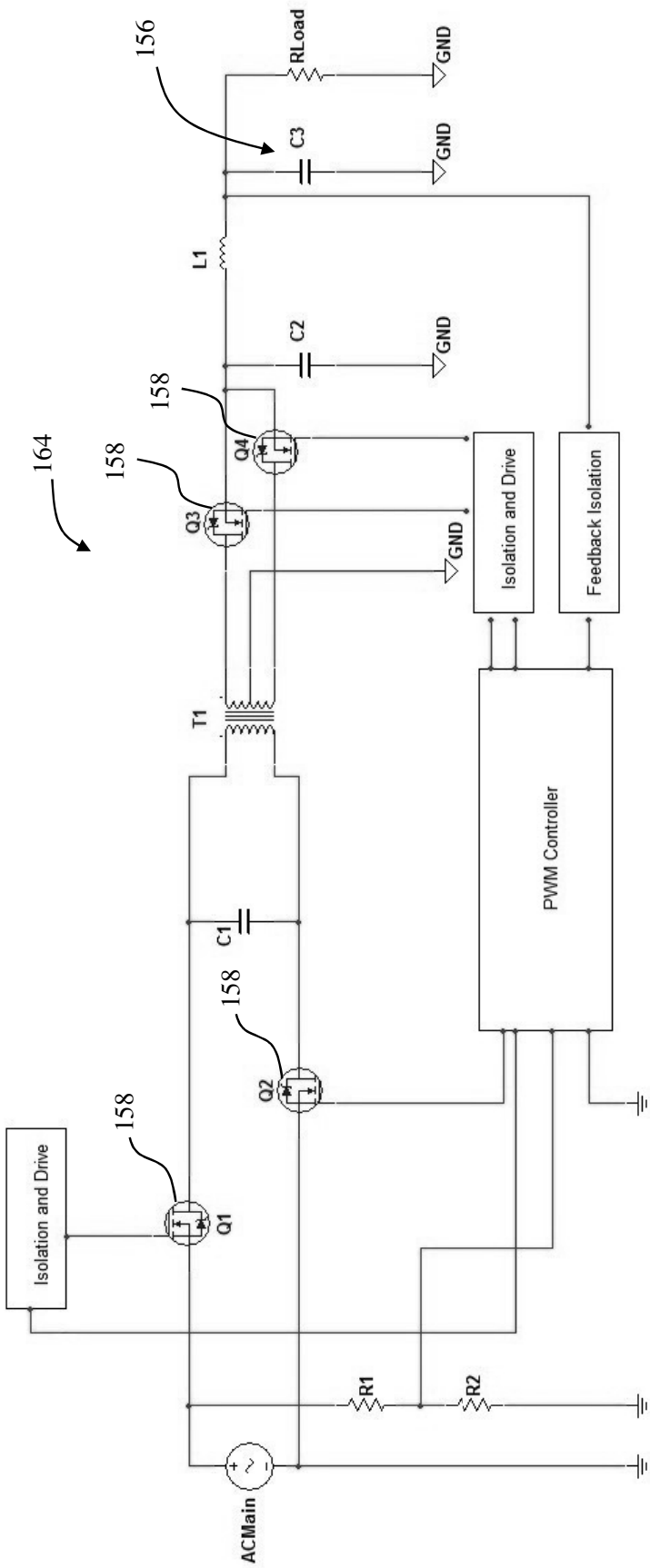
BiDFET with FET Source Connected to Transformer, Synchronous Secondary, PWM Controller Referenced to Primary

FIG. 48



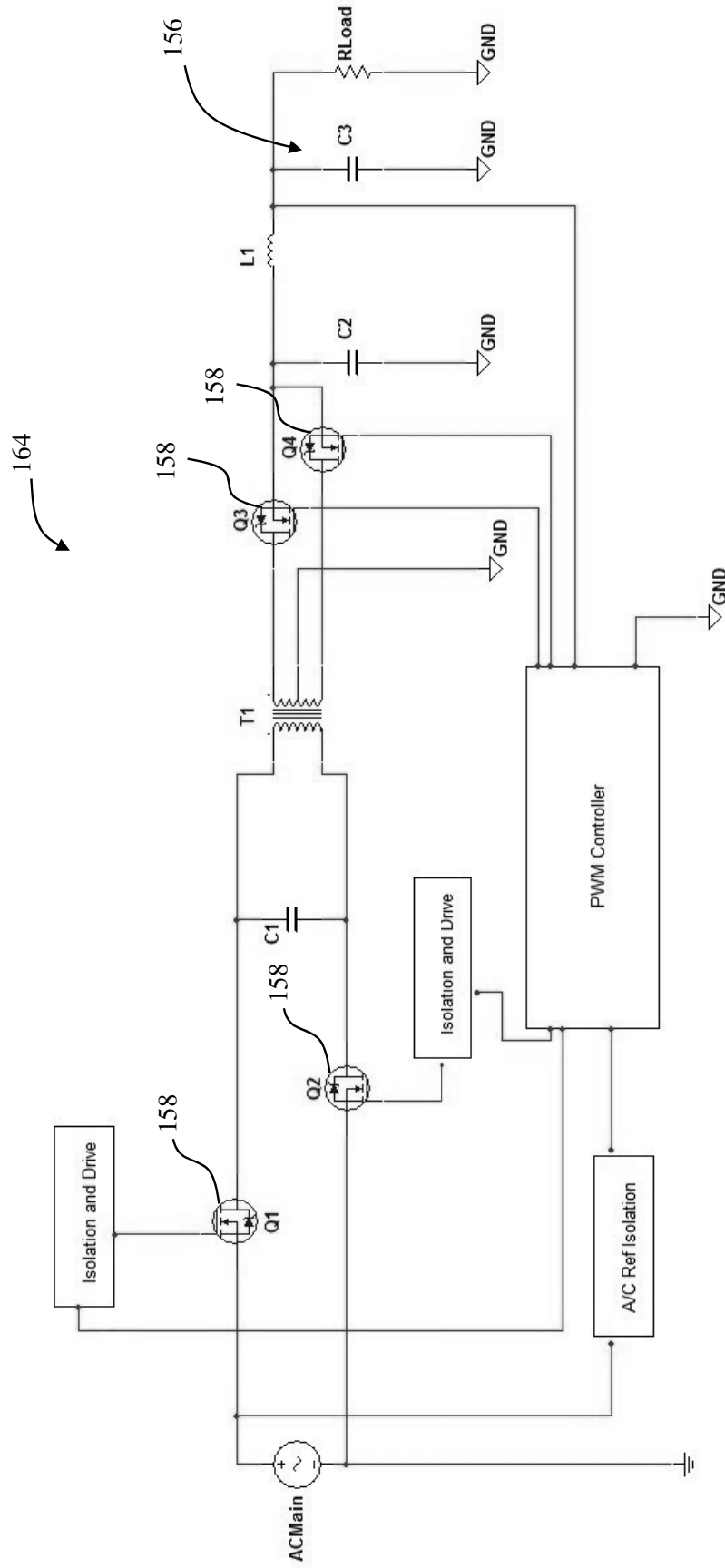
BiFET with FET Source Connected to Transformer, Asynchronous Secondary, PWM Controller Referenced to Primary

FIG. 49a



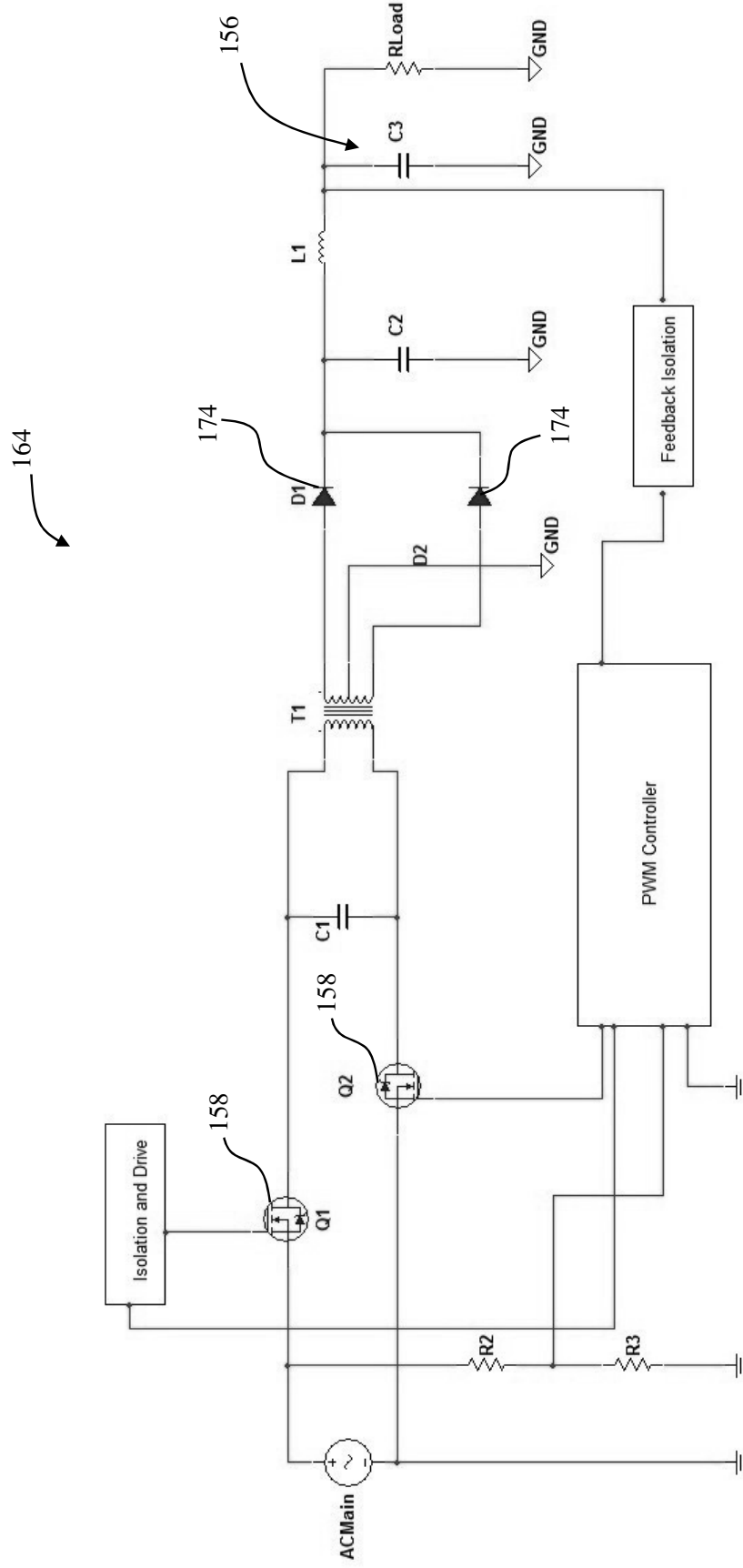
BiFET with FET Source Connected to AC Main, Synchronous Secondary, PWM Controller Referenced to Primary

FIG. 50a



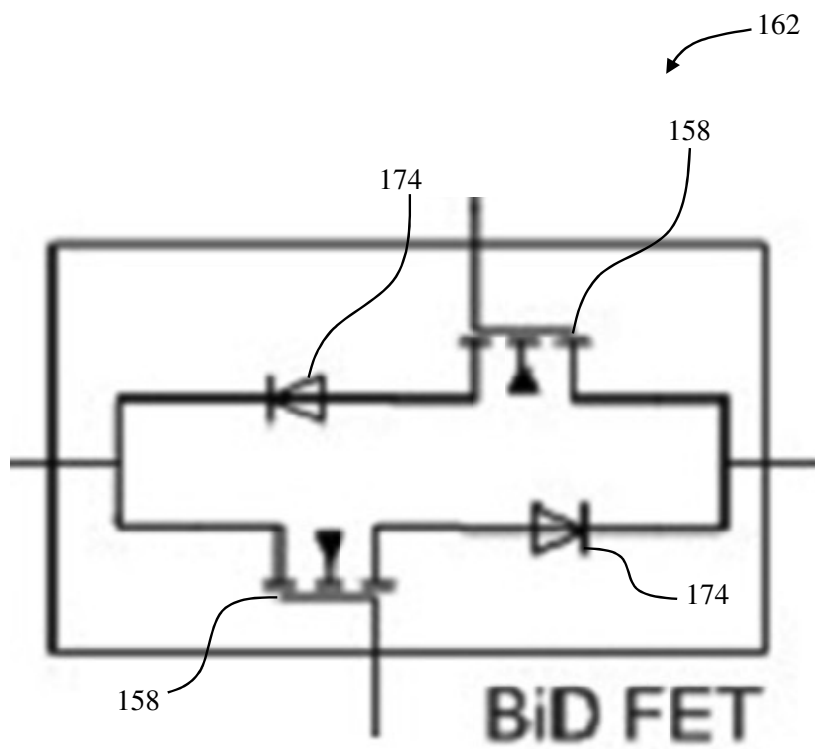
BIDFET with FET Source Connected to AC Main and PWM Controller Referenced to Synchronous Secondary

FIG. 51



BiDFET with FET Source Connected to AC Main, Asynchronous Secondary, PWM Controller Referenced to Primary

FIG. 52

**FIG. 53**

BiDFET chopped up Sine Wave
Can be evenly “chopped” or unevenly “chopped”

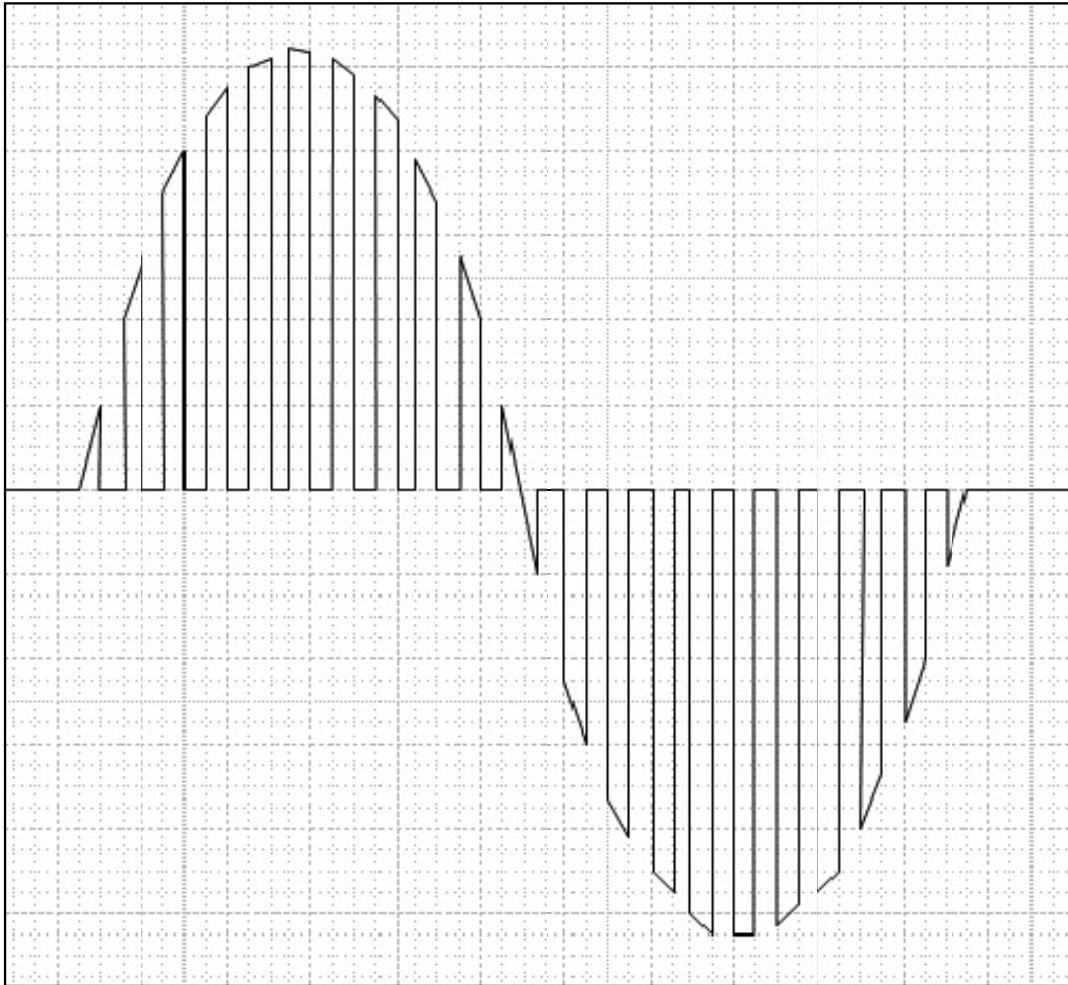
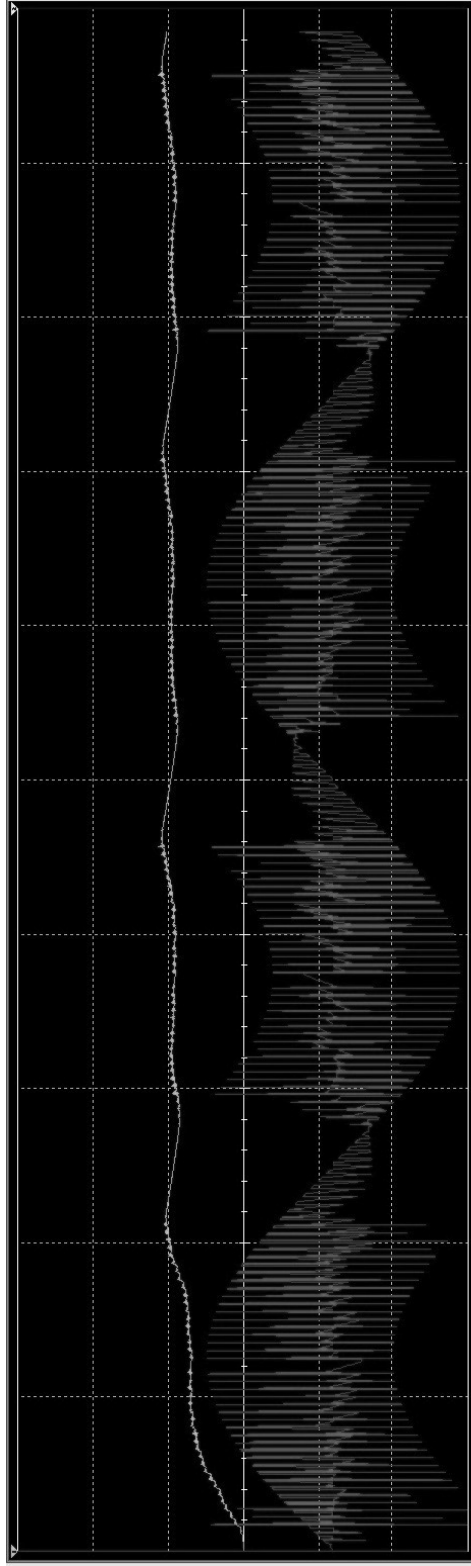
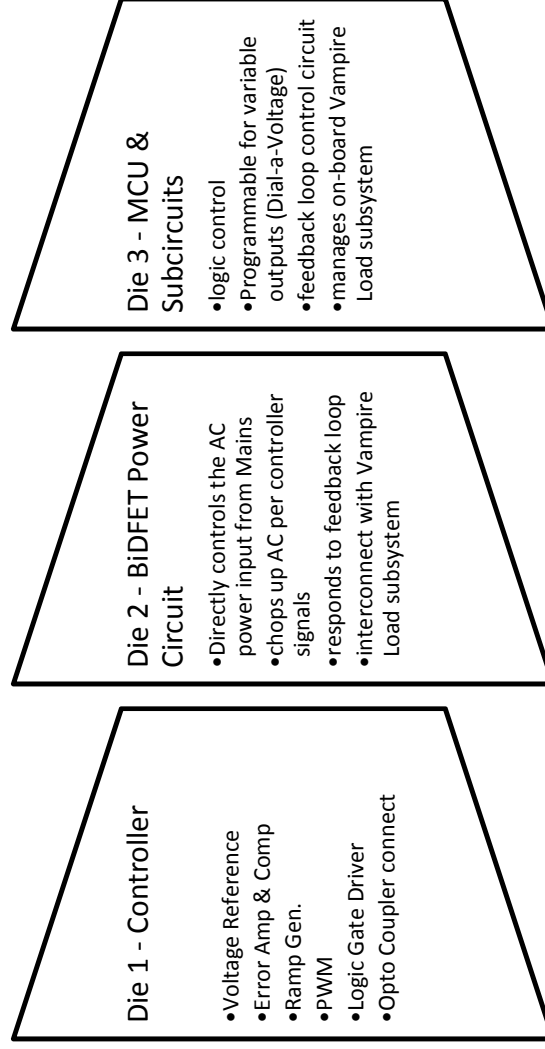


FIG. 54

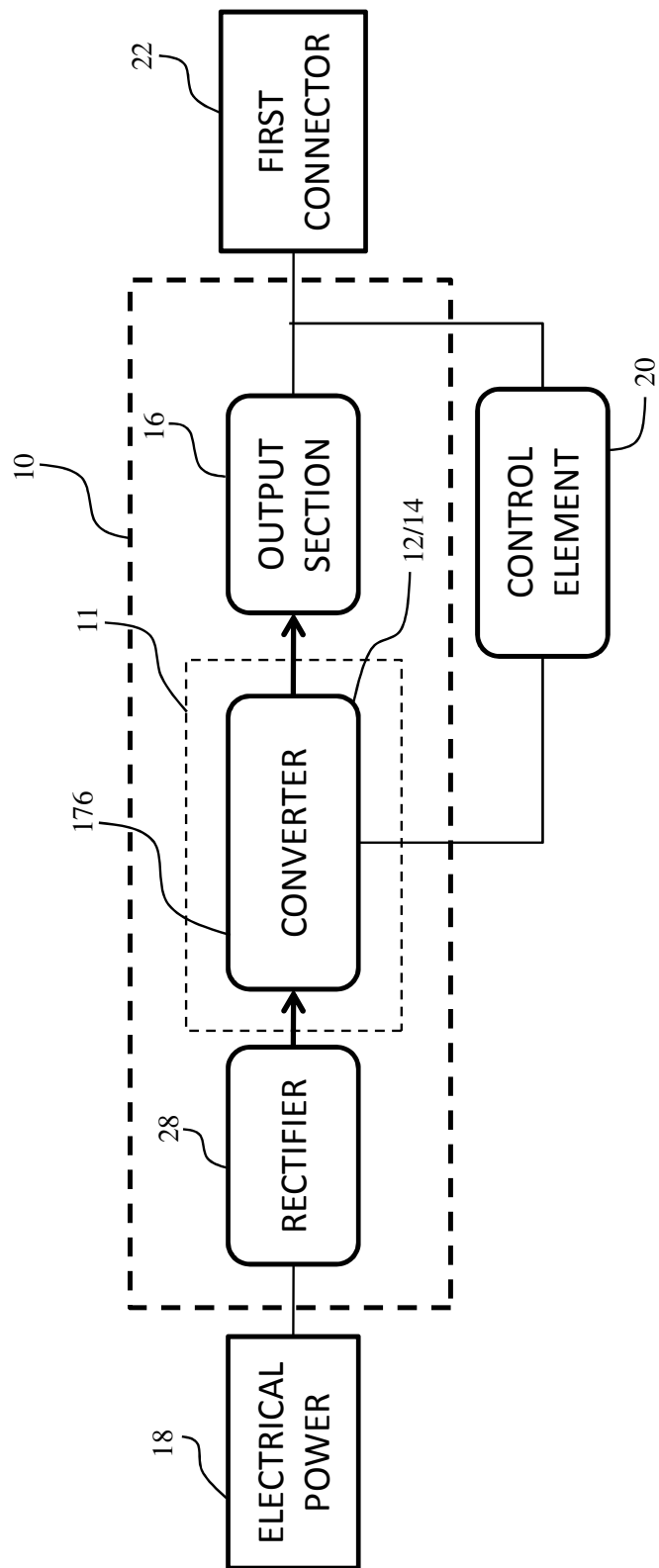
BiDFET Voltage Plot

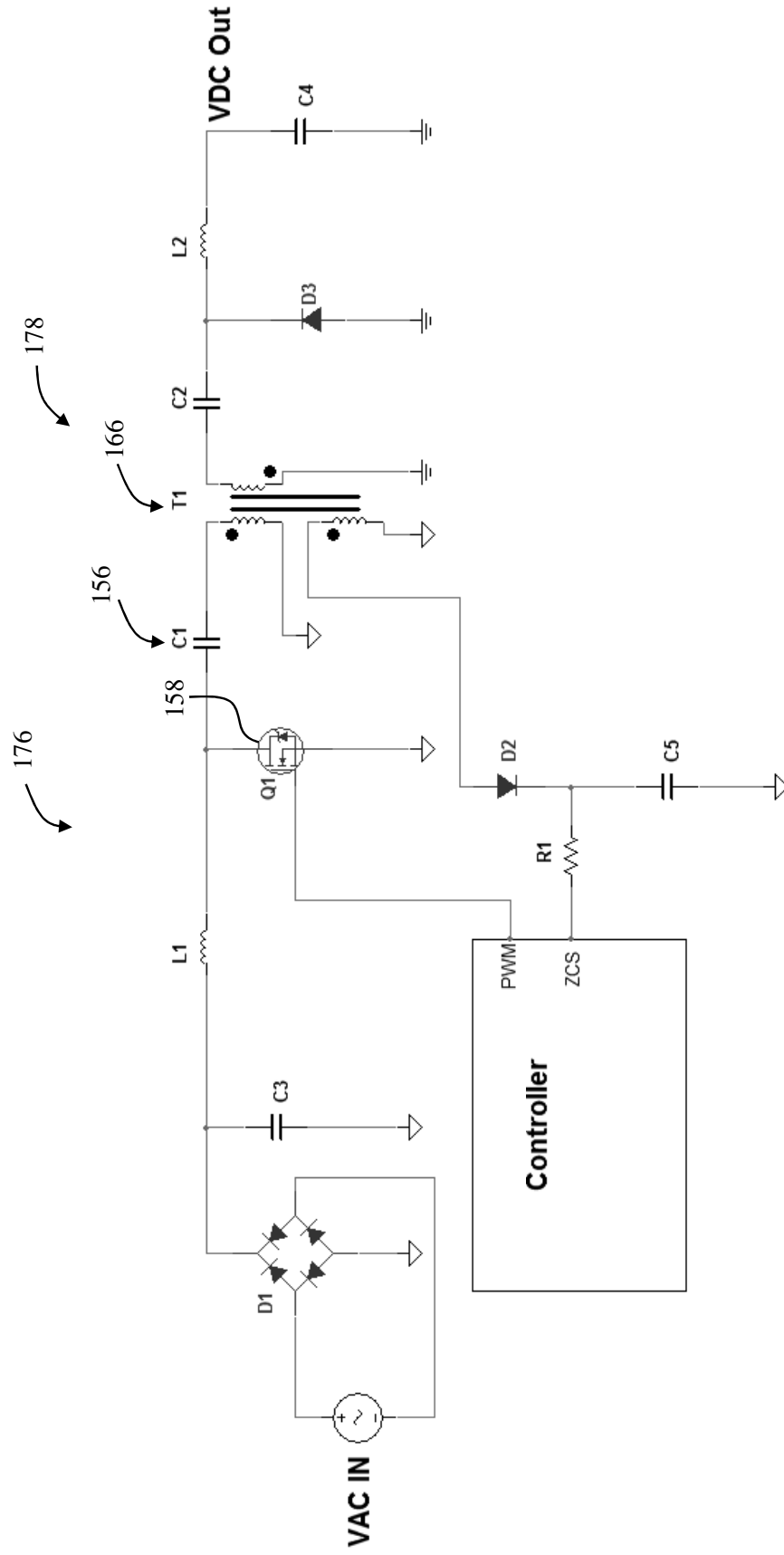
**FIG. 55**



Block Diagram of Dies for a BiDFET Integrated Module Package

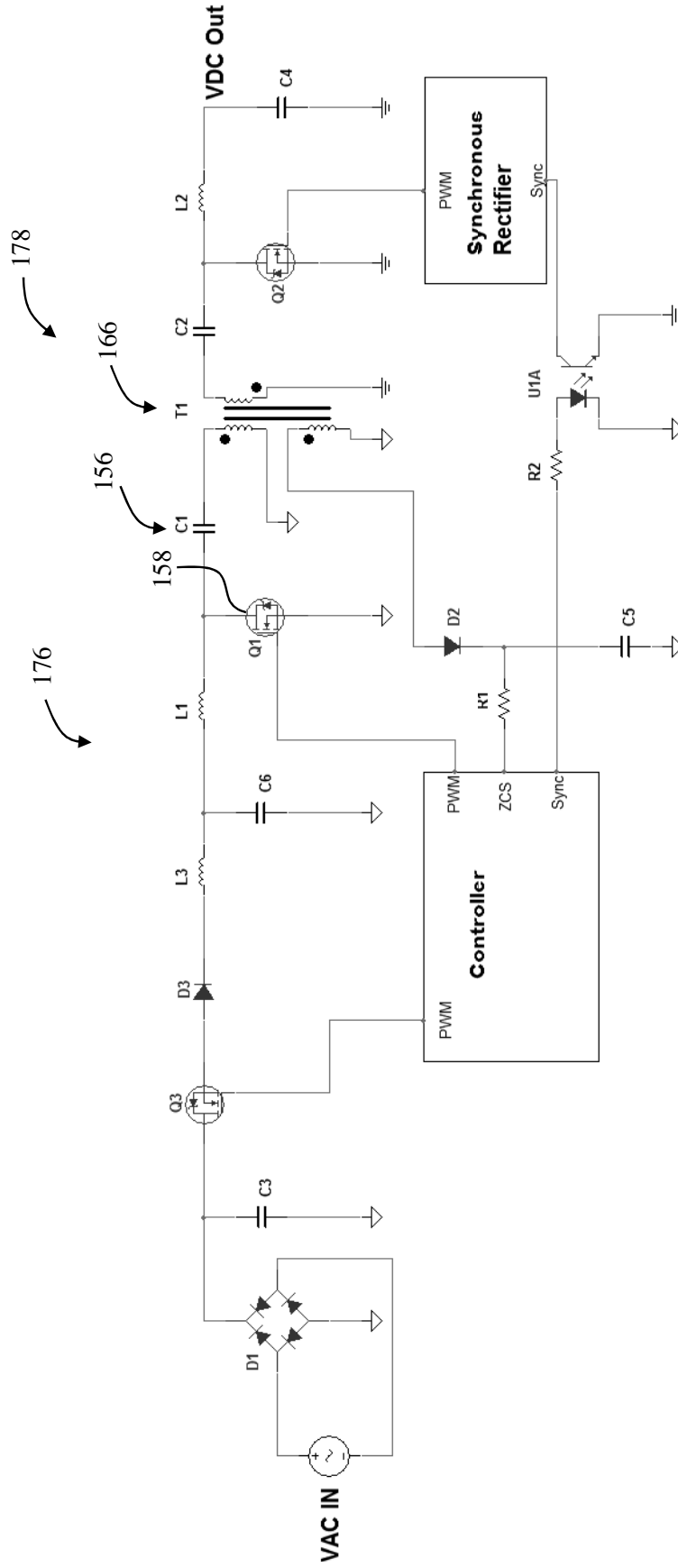
FIG. 56

**FIG. 57**



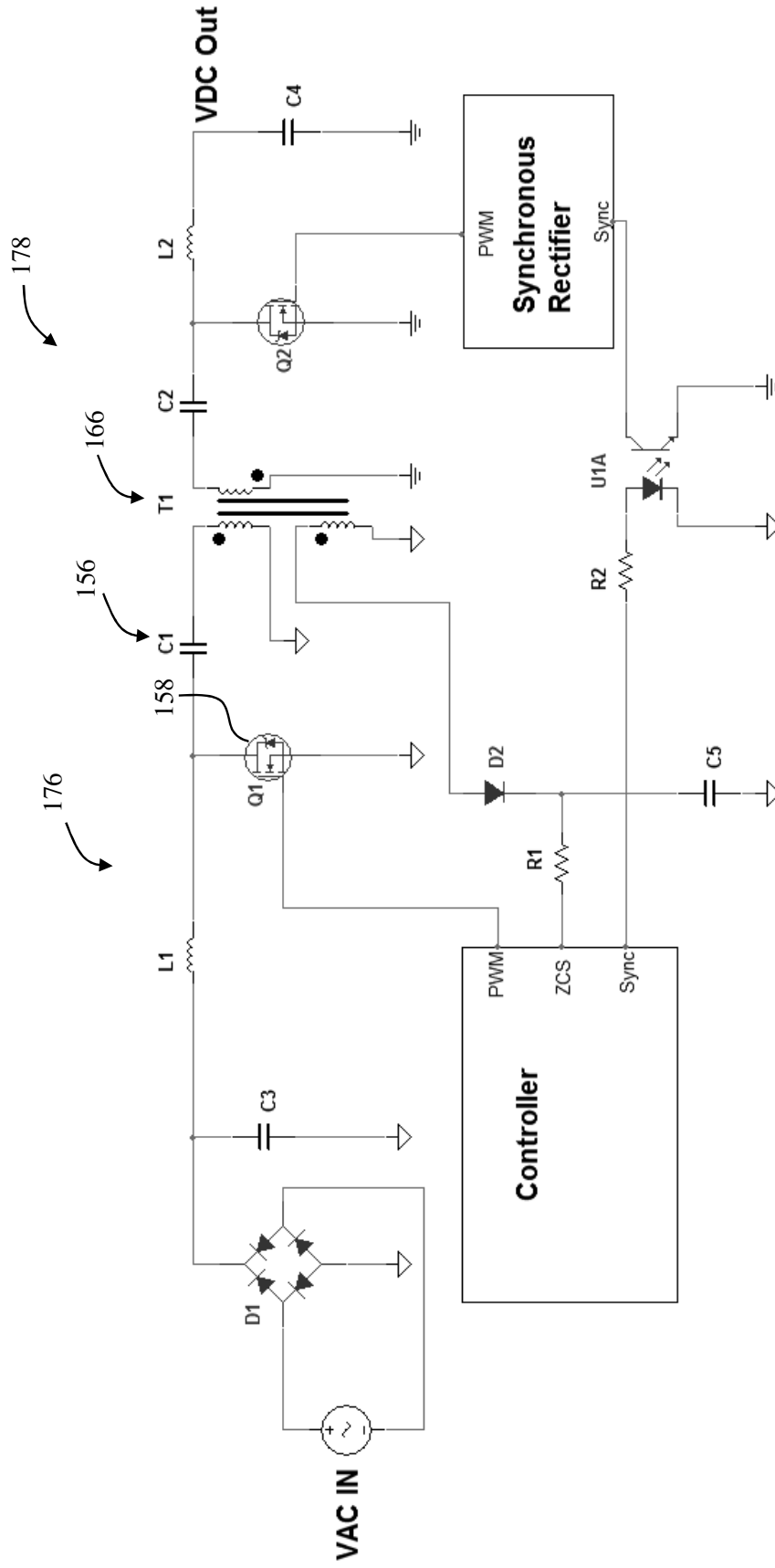
Asynchronous Modified Çuk Converter

FIG. 58



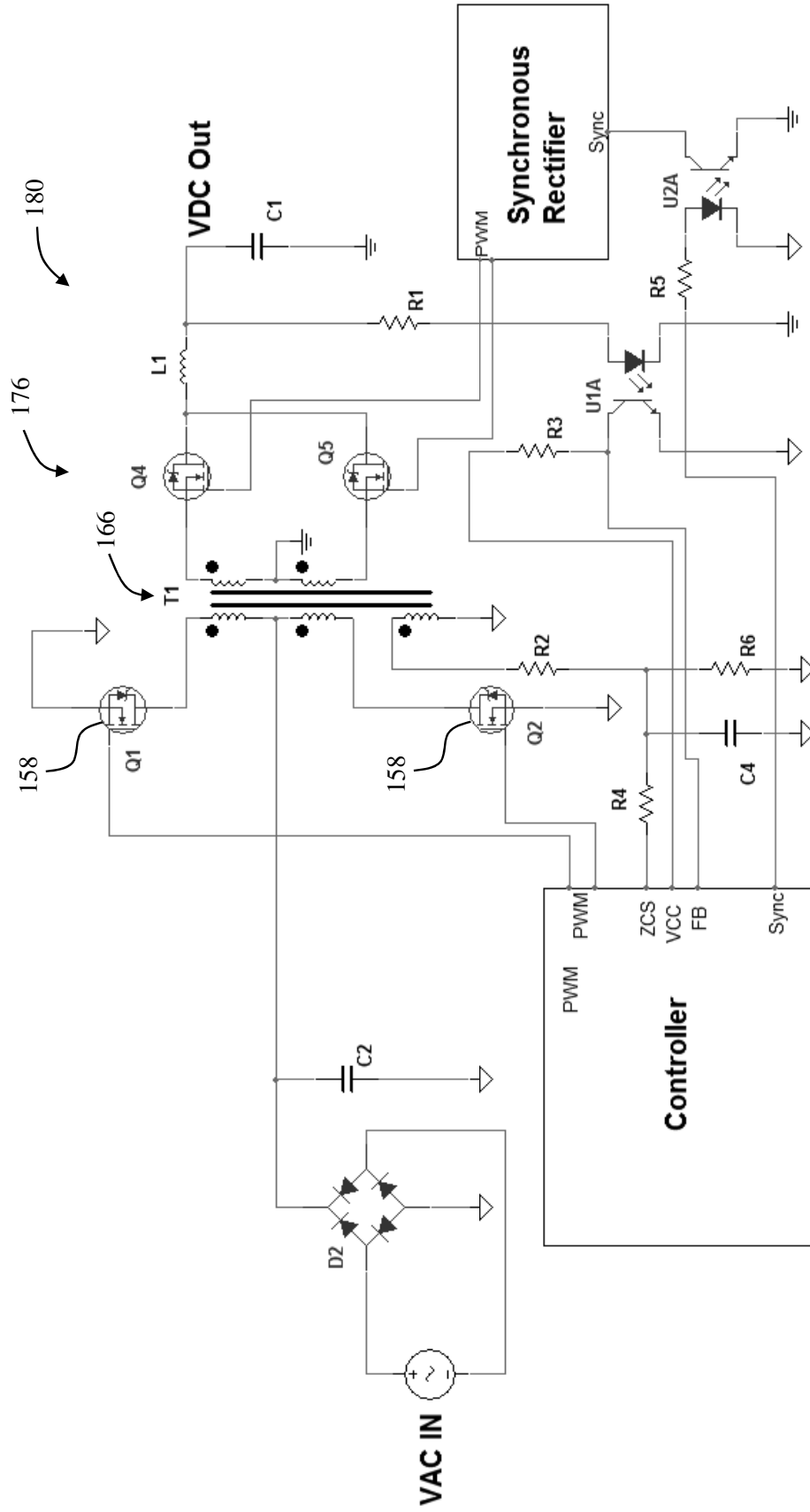
Synchronous Modified Çuk Converter with Quasi-Resonant Front End

FIG. 59



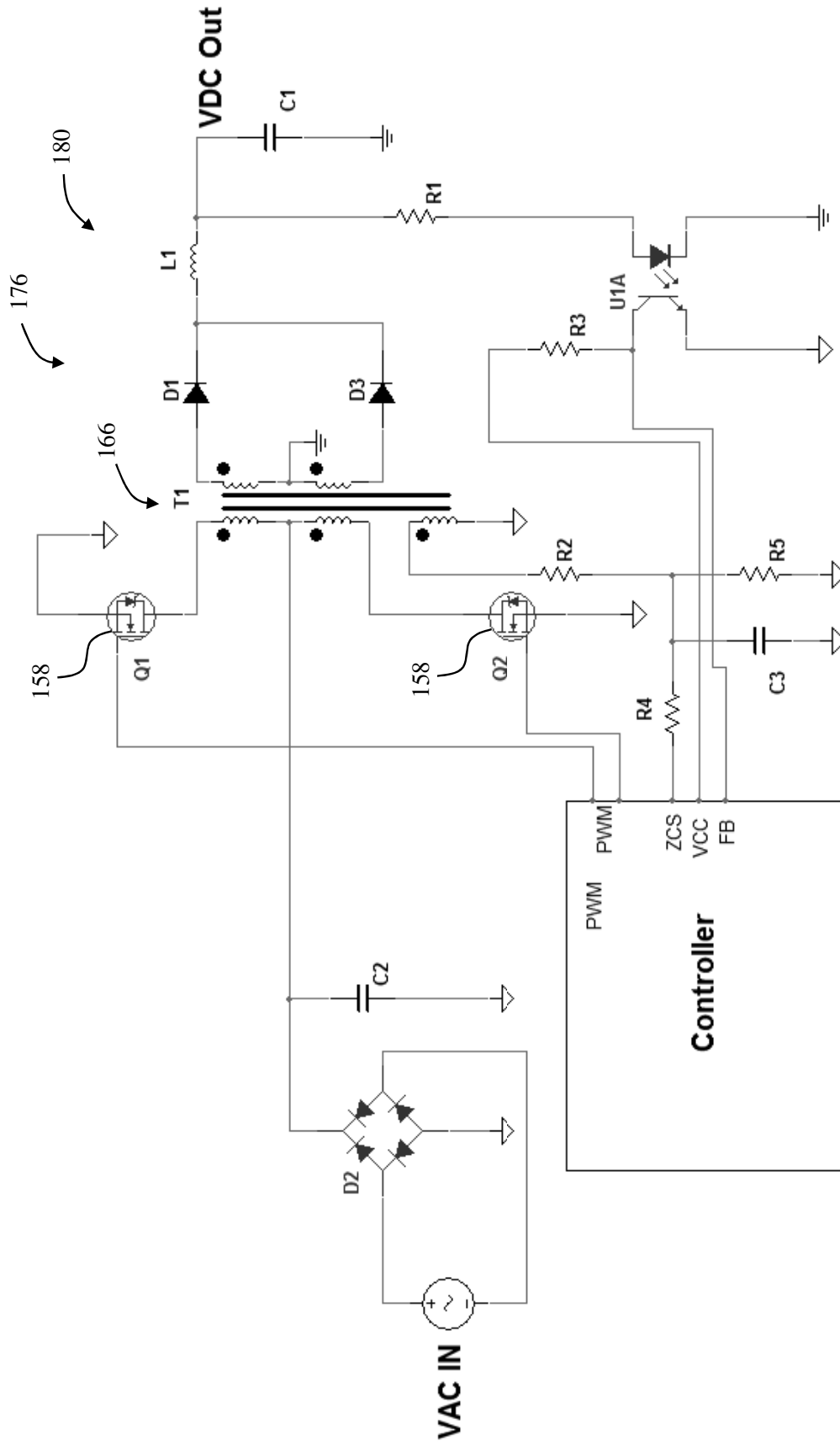
Synchronous Modified Çuk Converter

FIG. 60



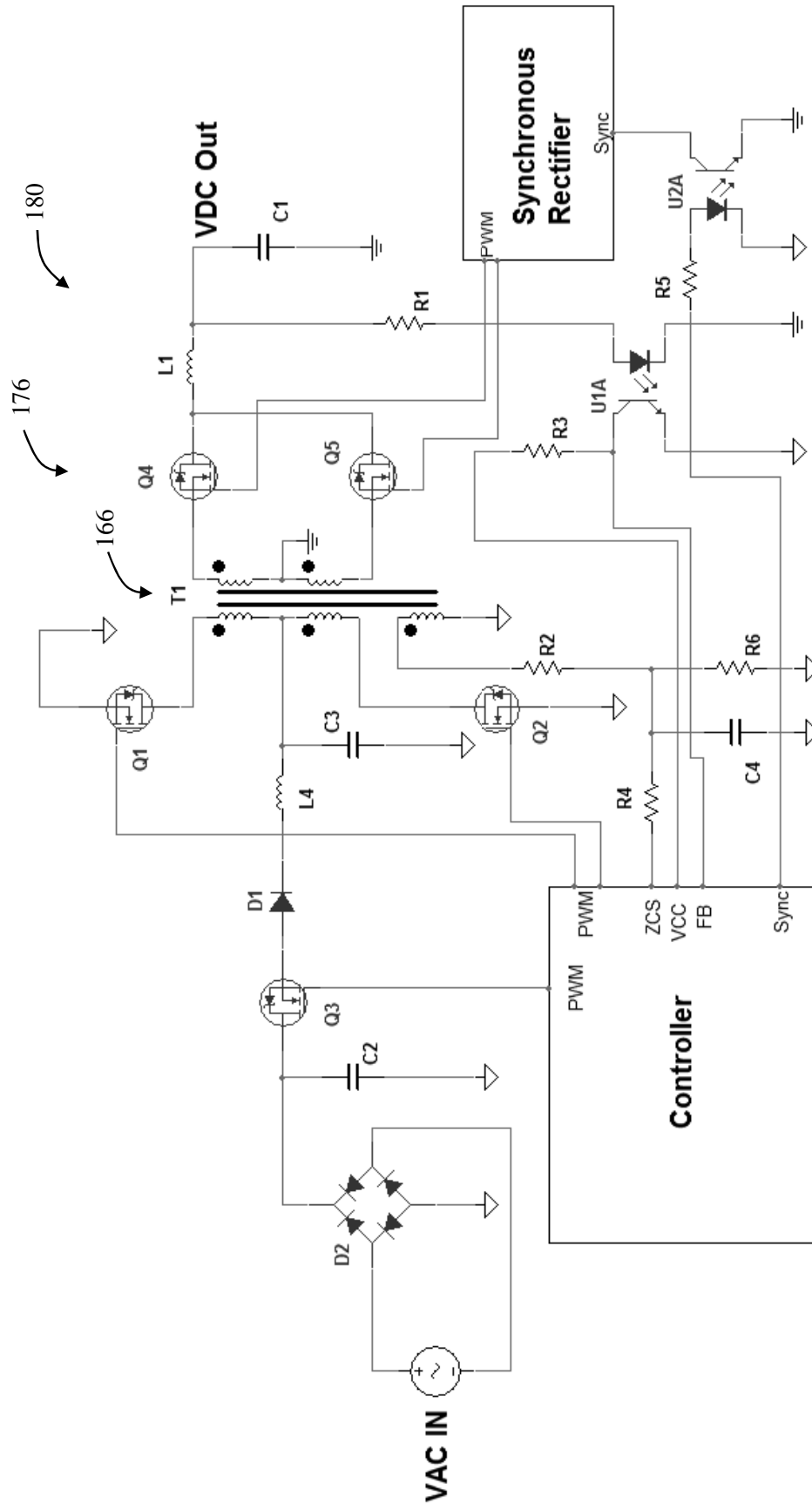
Synchronous Modified Push-Pull Converter

FIG. 61



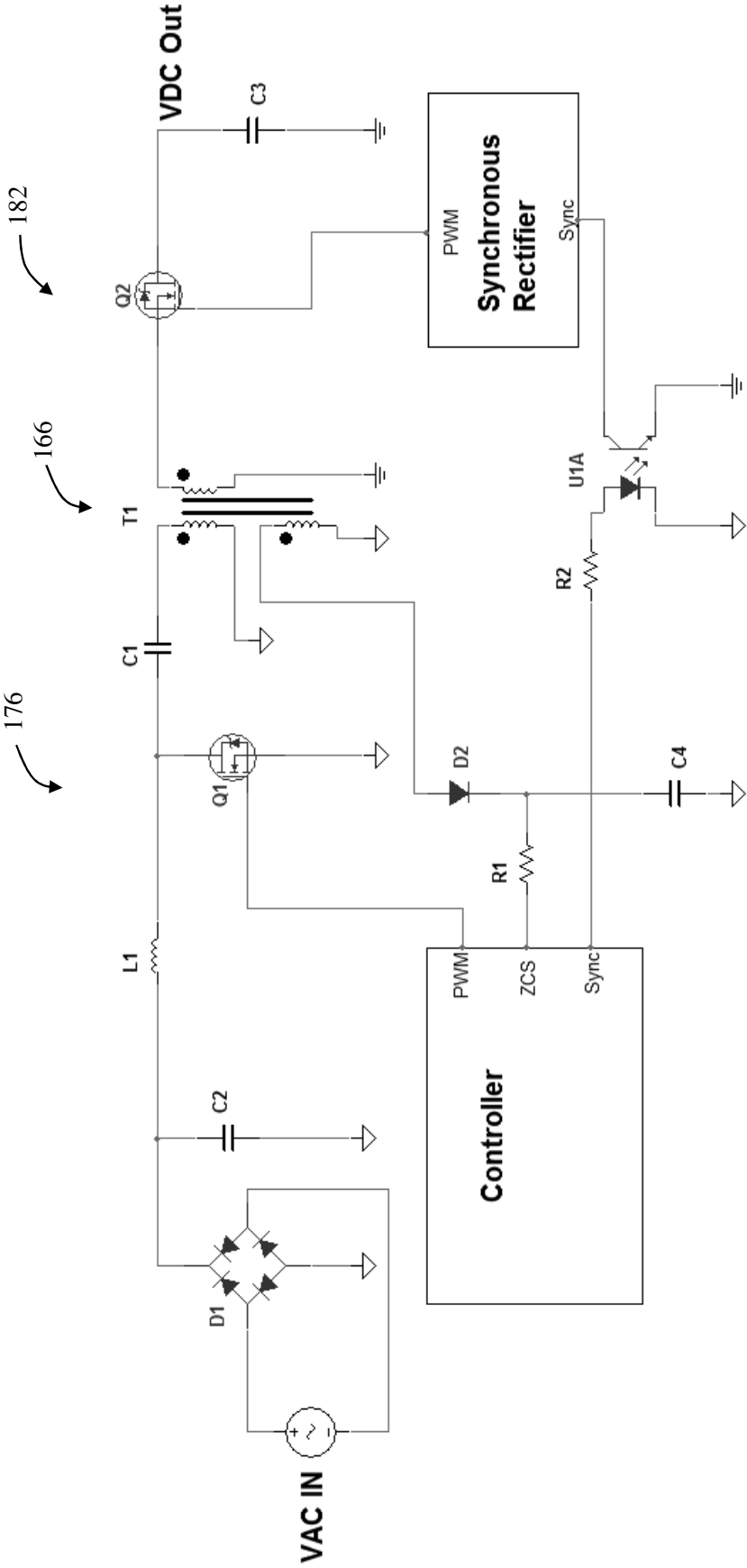
Asynchronous Modified Push-Pull Converter

FIG. 62



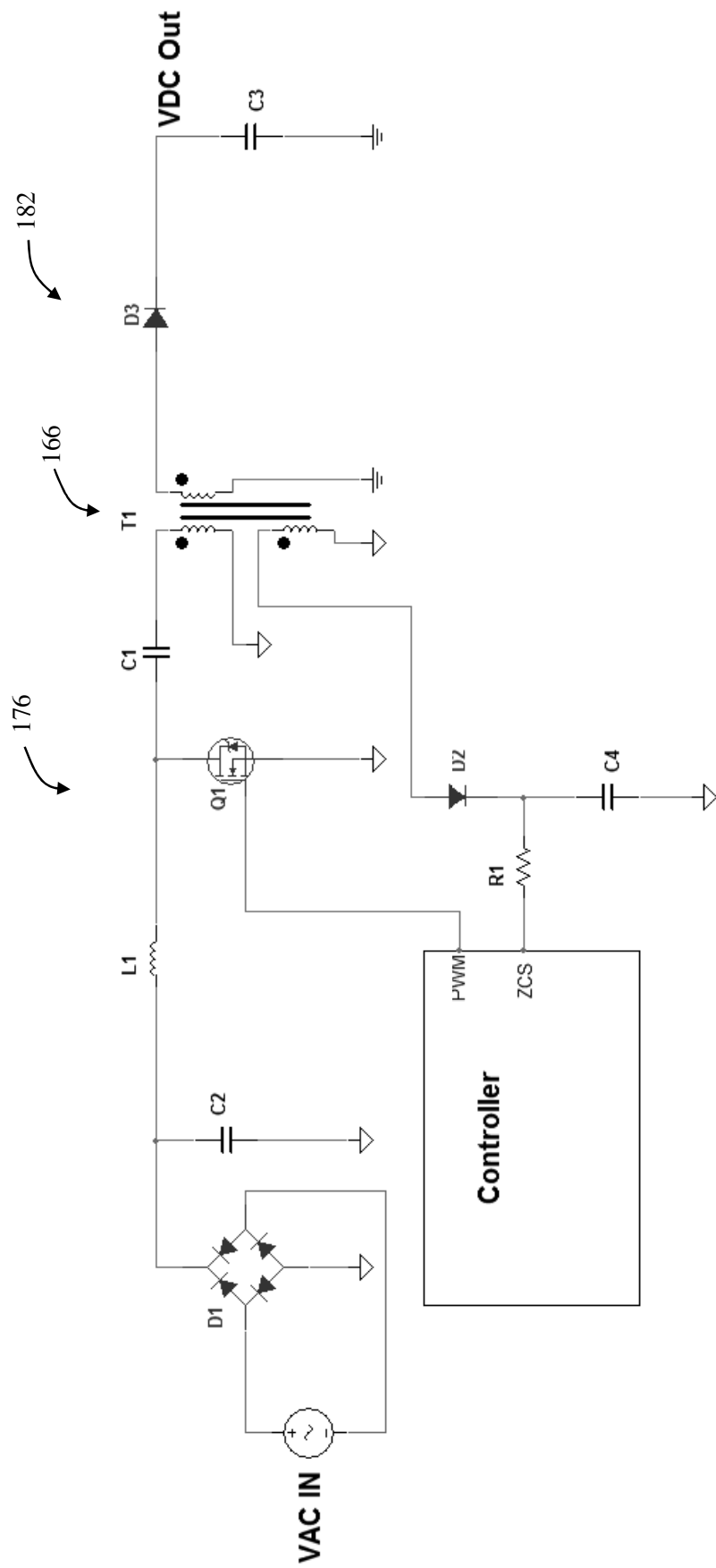
Synchronous Modified Push-Pull Converter With Quasi-Resonant Front End

FIG. 63



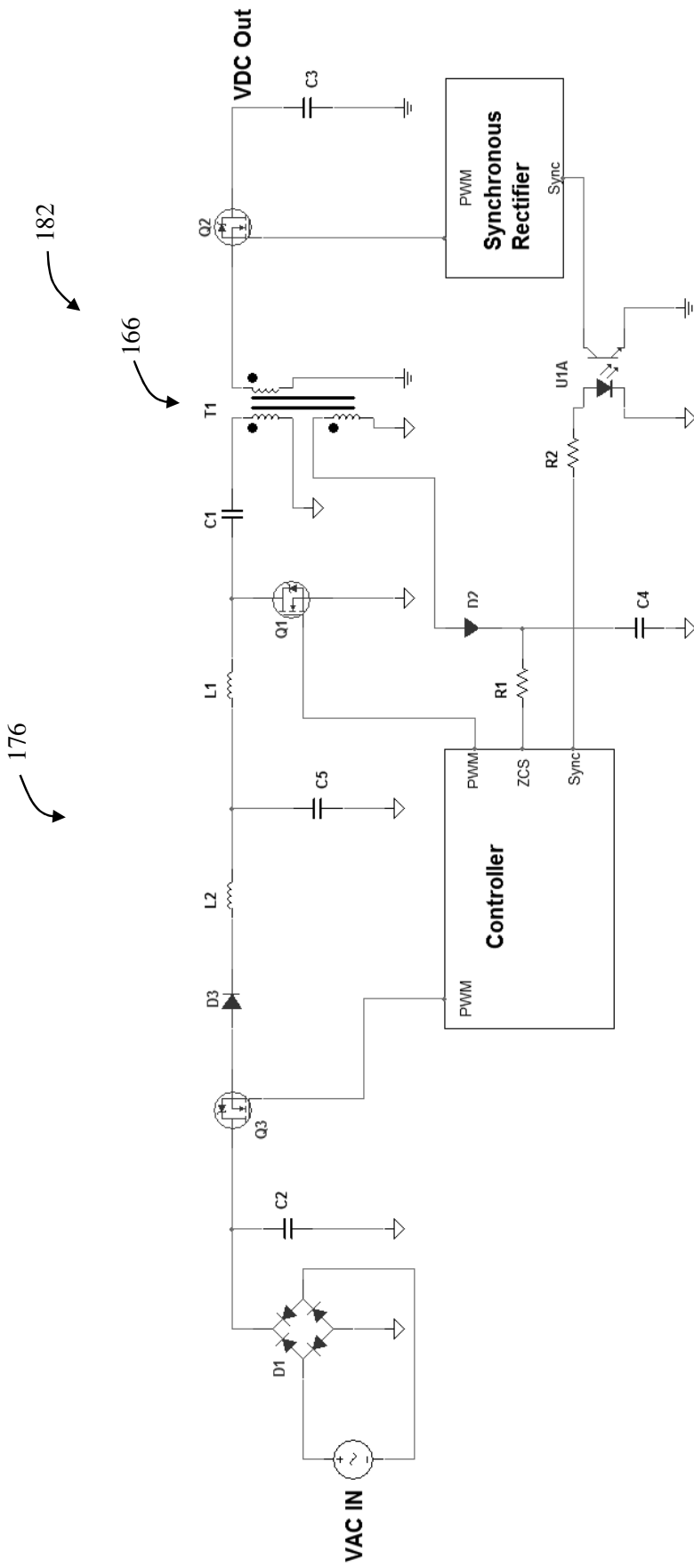
Synchronous Modified SEPIC Converter

FIG. 64



Asynchronous Modified SEPIC Converter

FIG. 65



Synchronous Modified SEPIC Converter With Quasi-Resonant Front End

FIG. 66

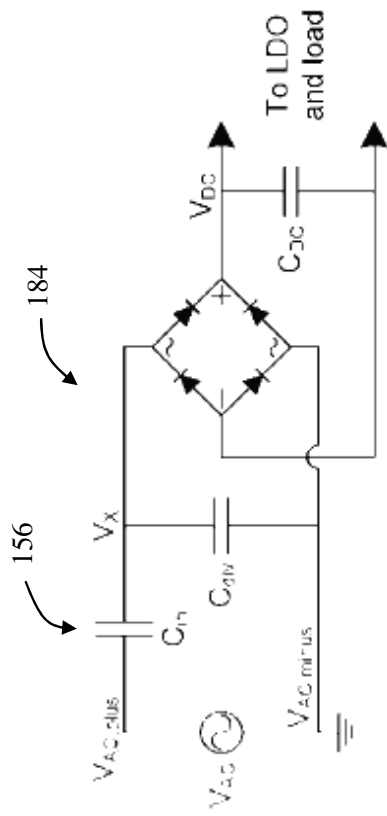


FIG. 67

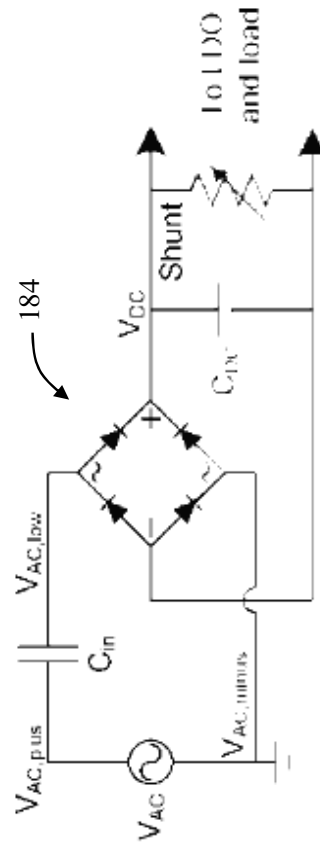


FIG. 68

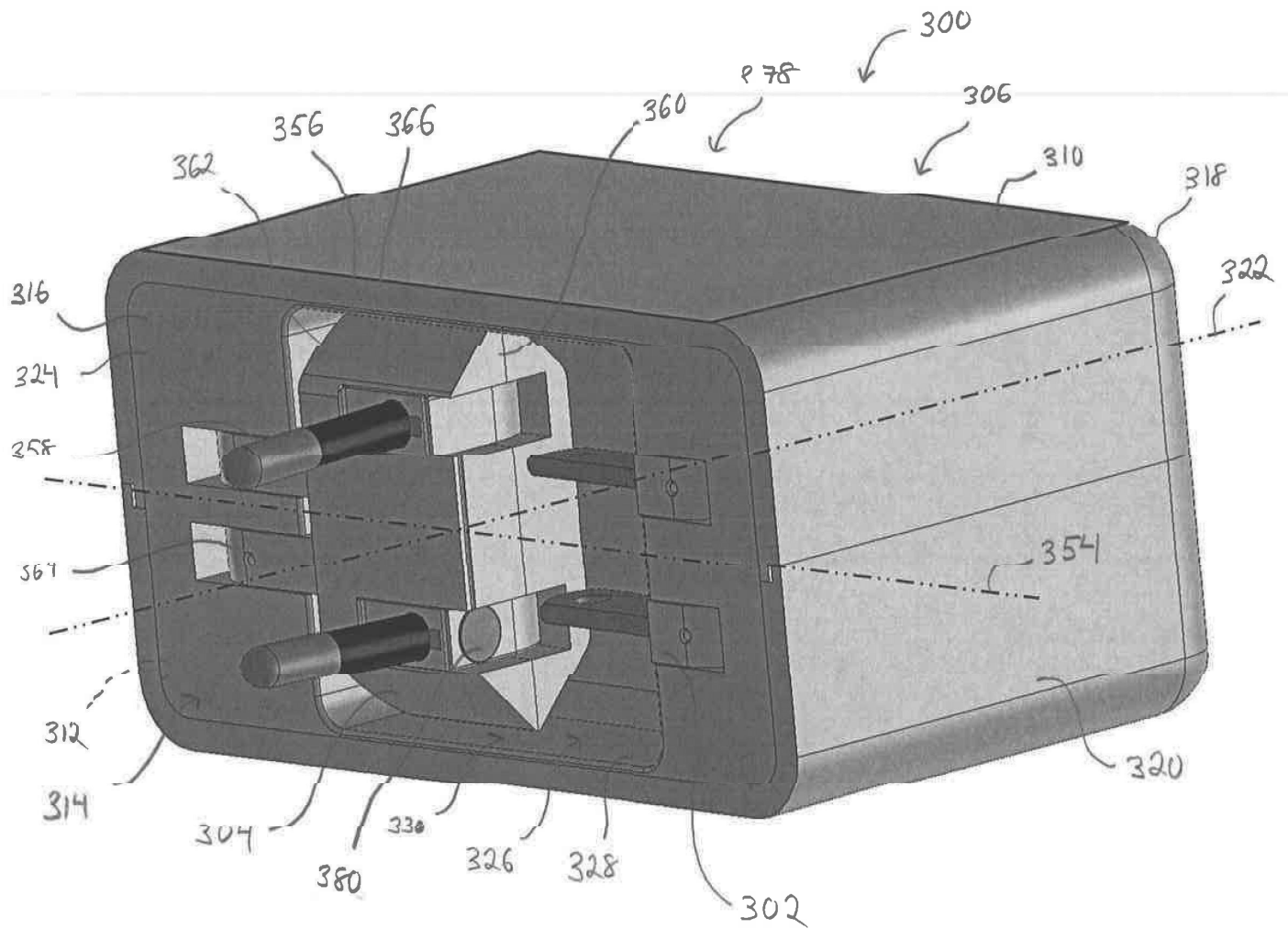


FIG. 69

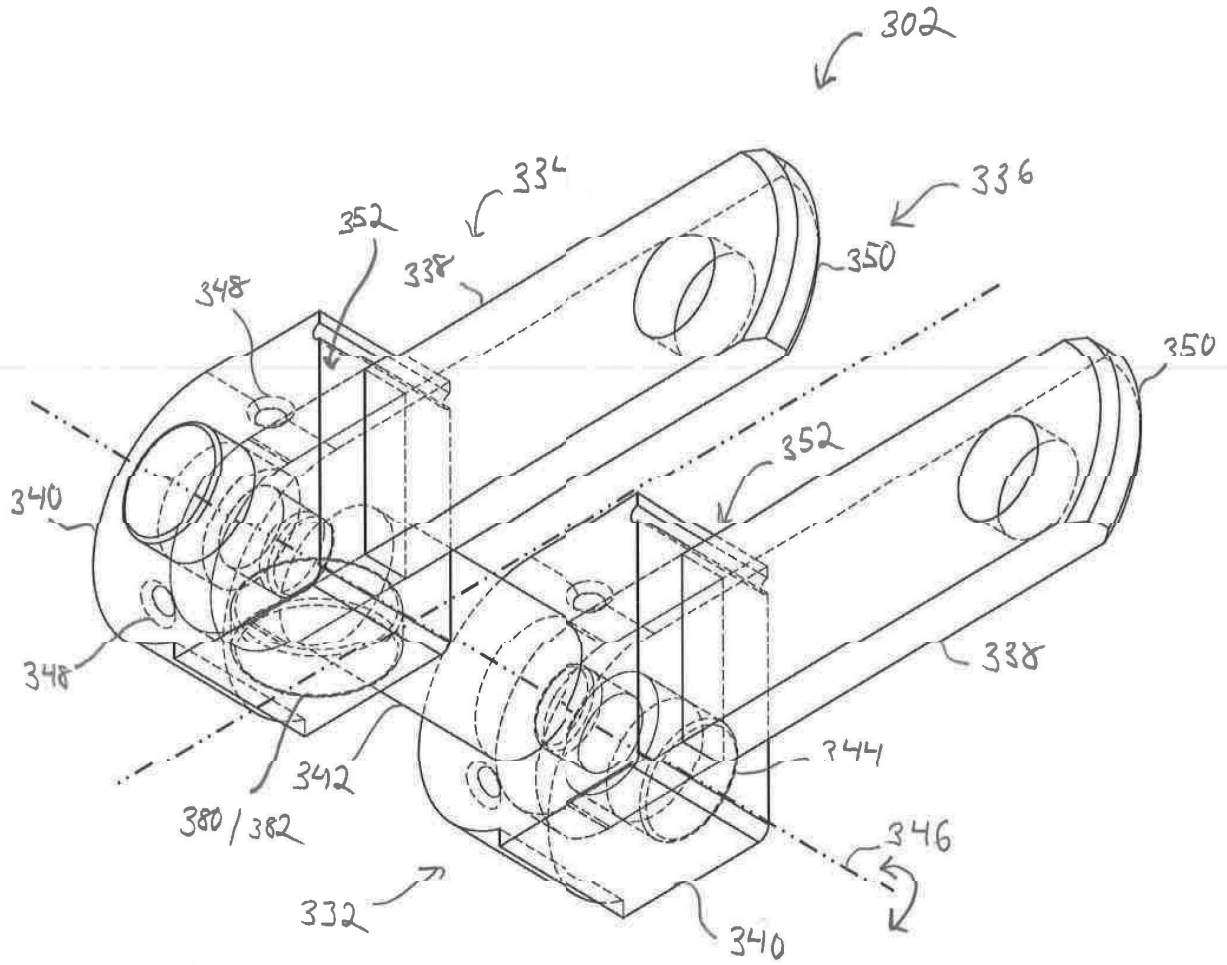


FIG. 70

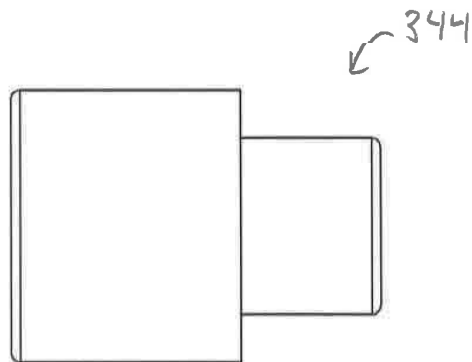


FIG. 71

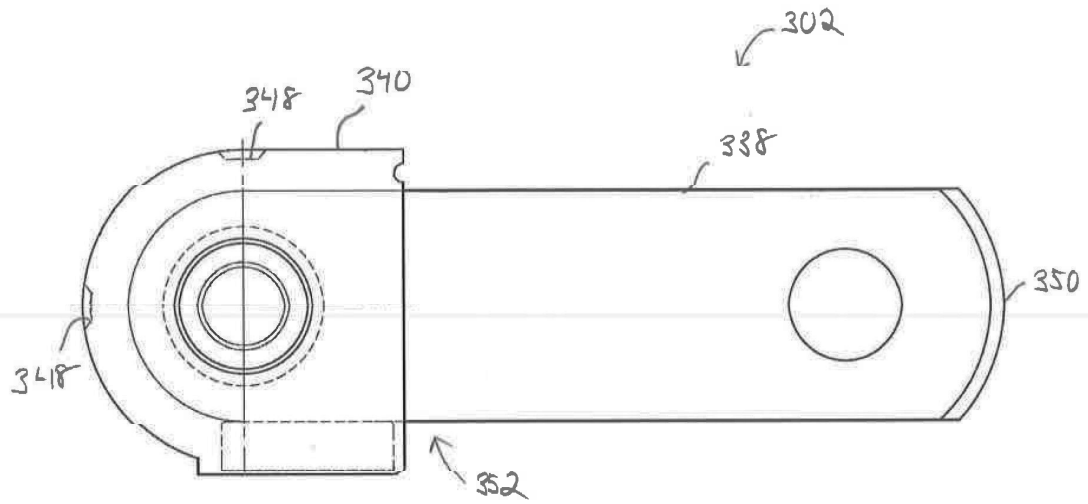


FIG. 72

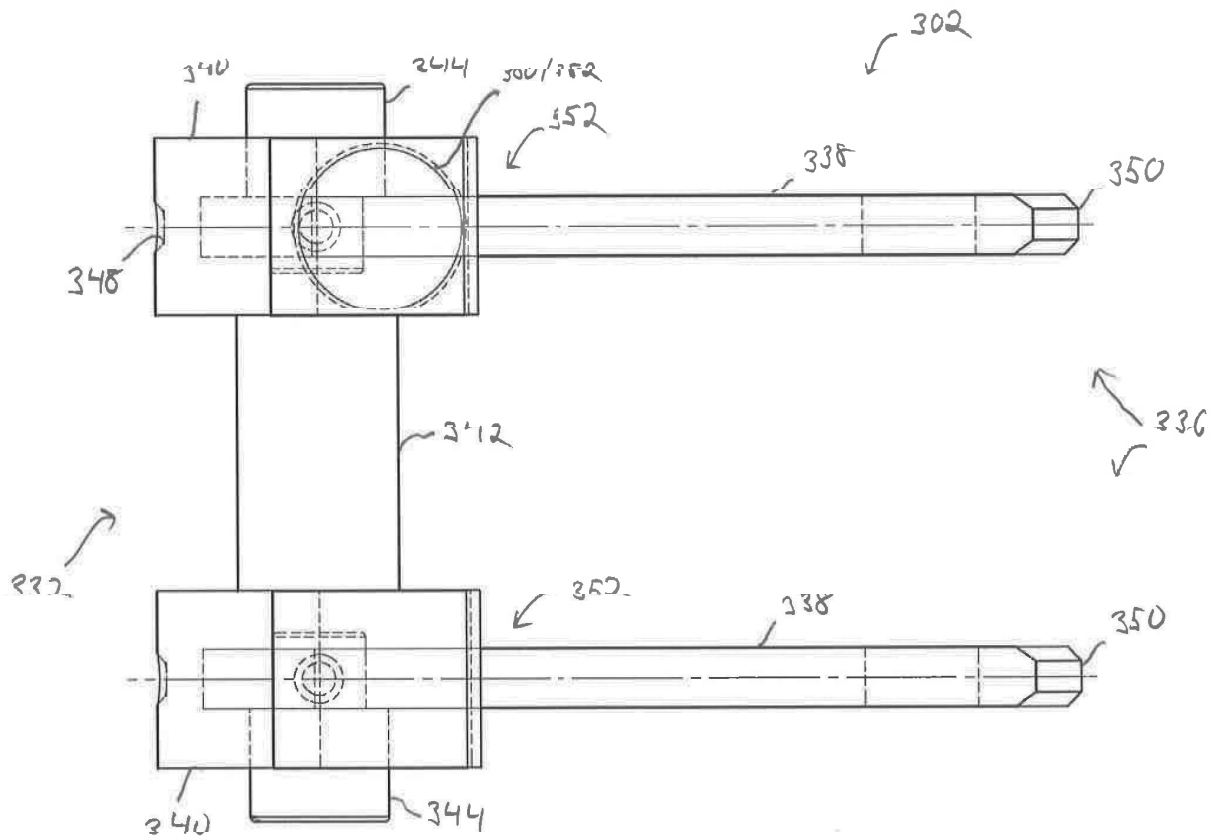


FIG. 73

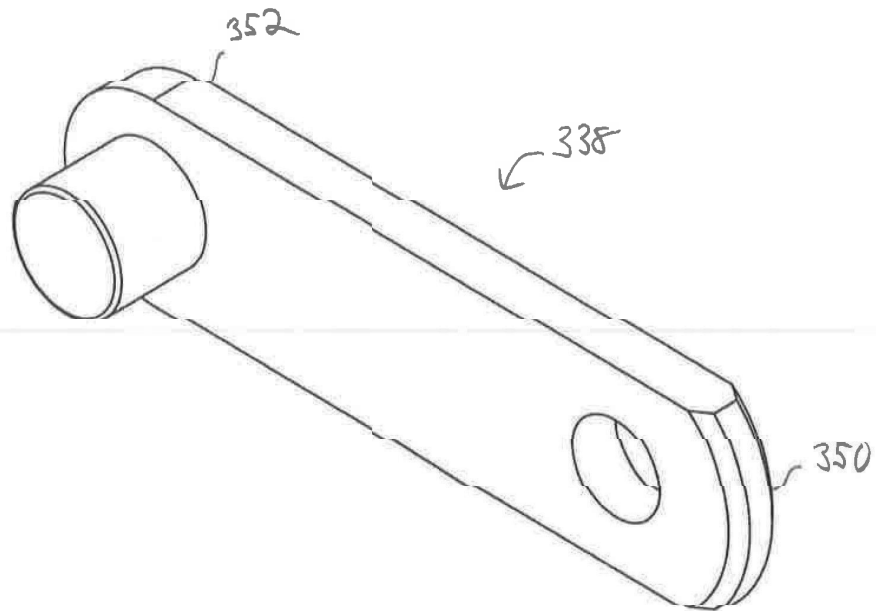


FIG. 74

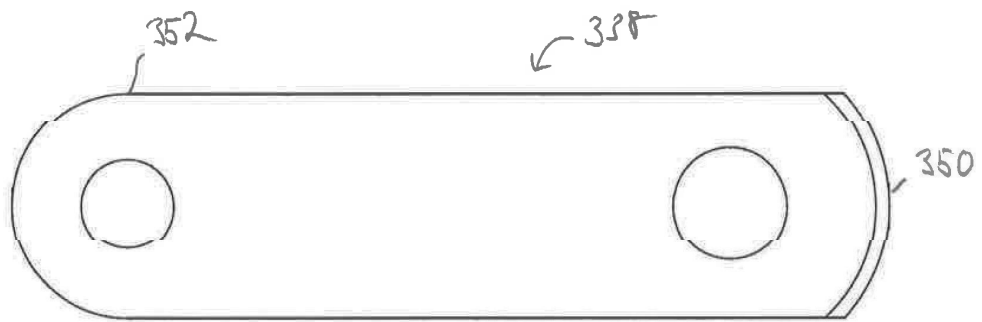


FIG. 75

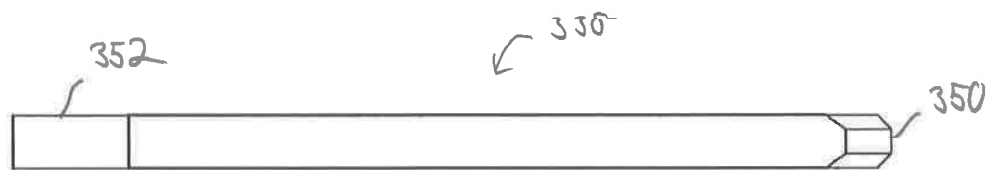


FIG. 76

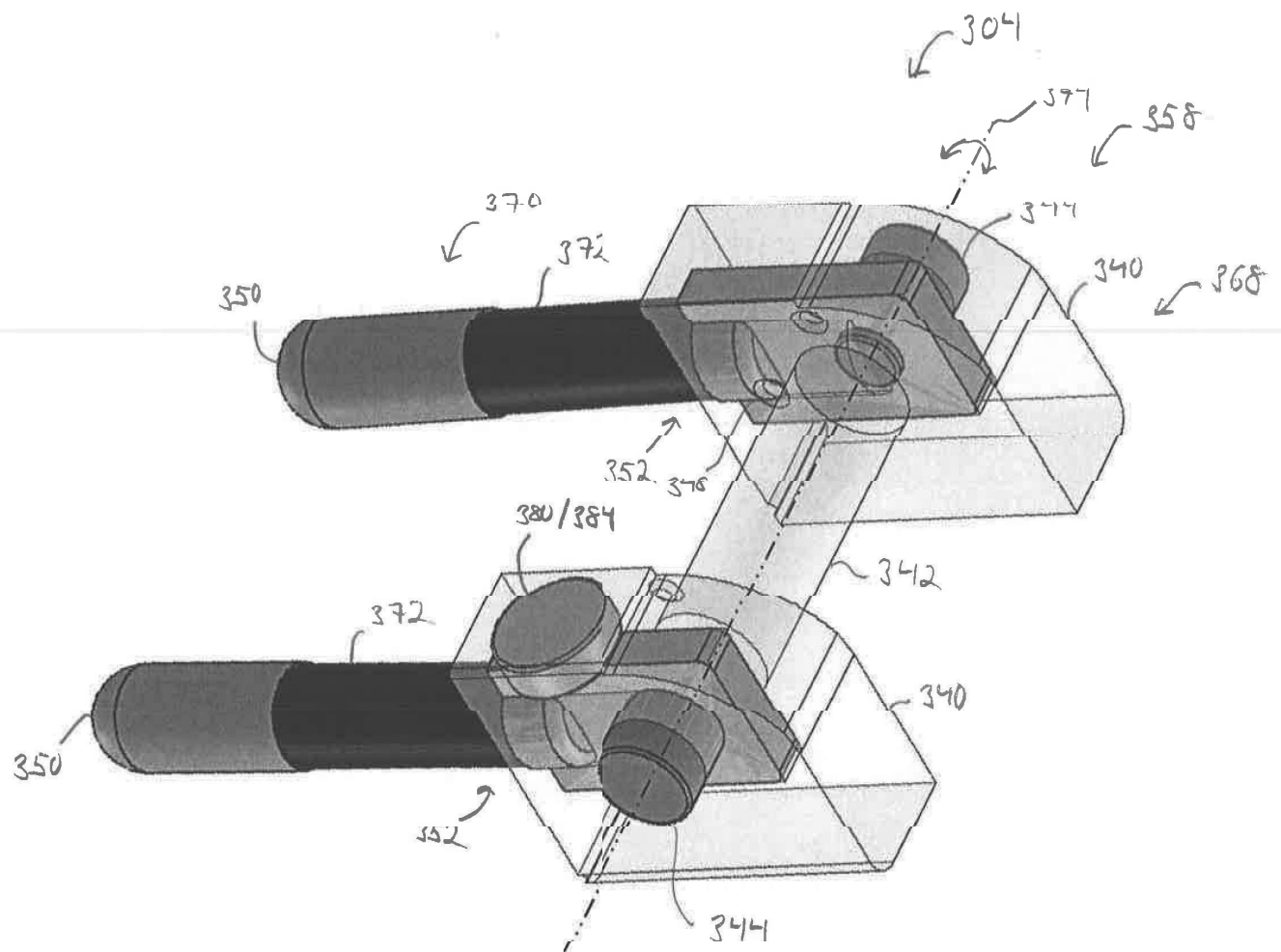


FIG. 77

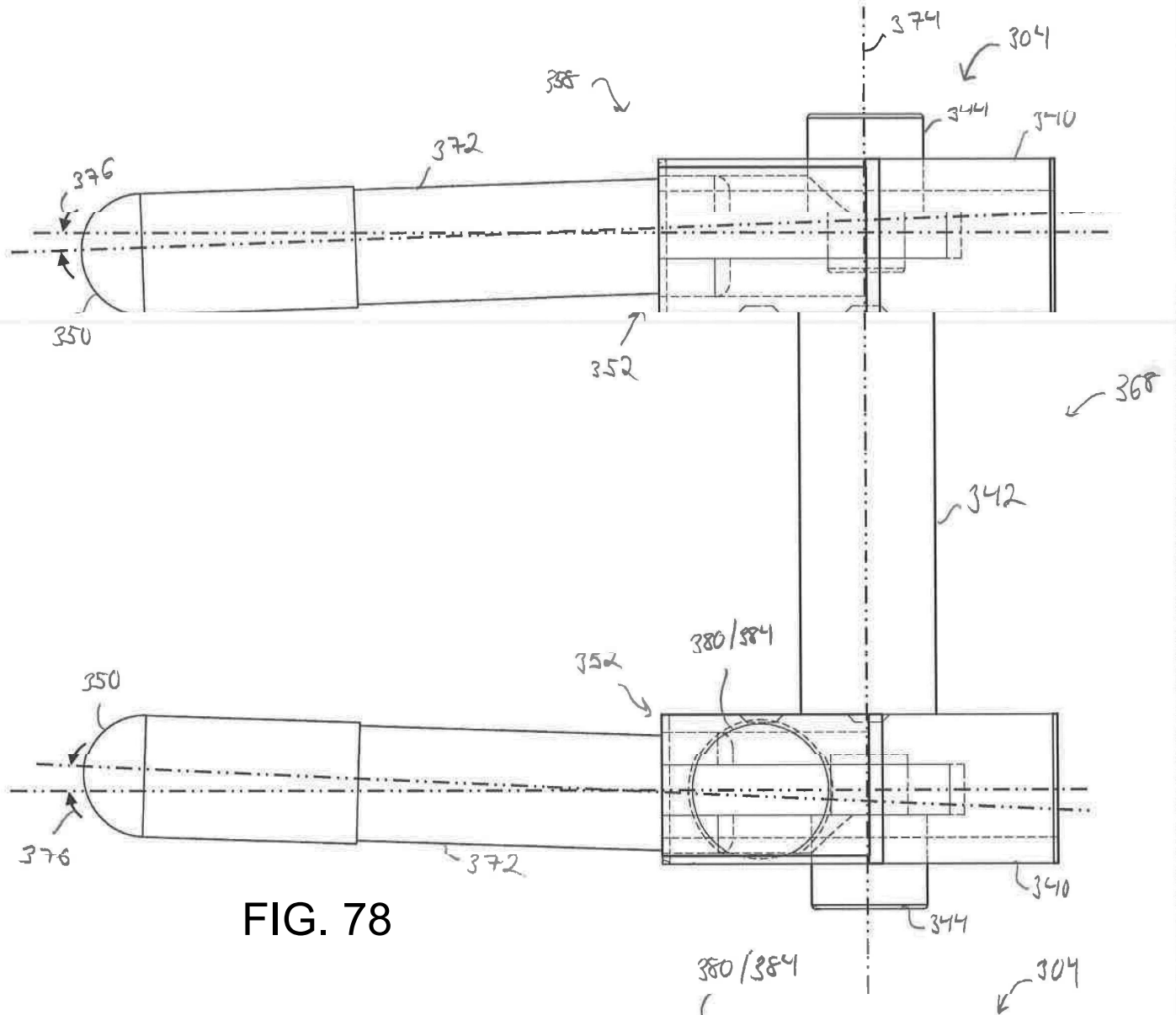


FIG. 78

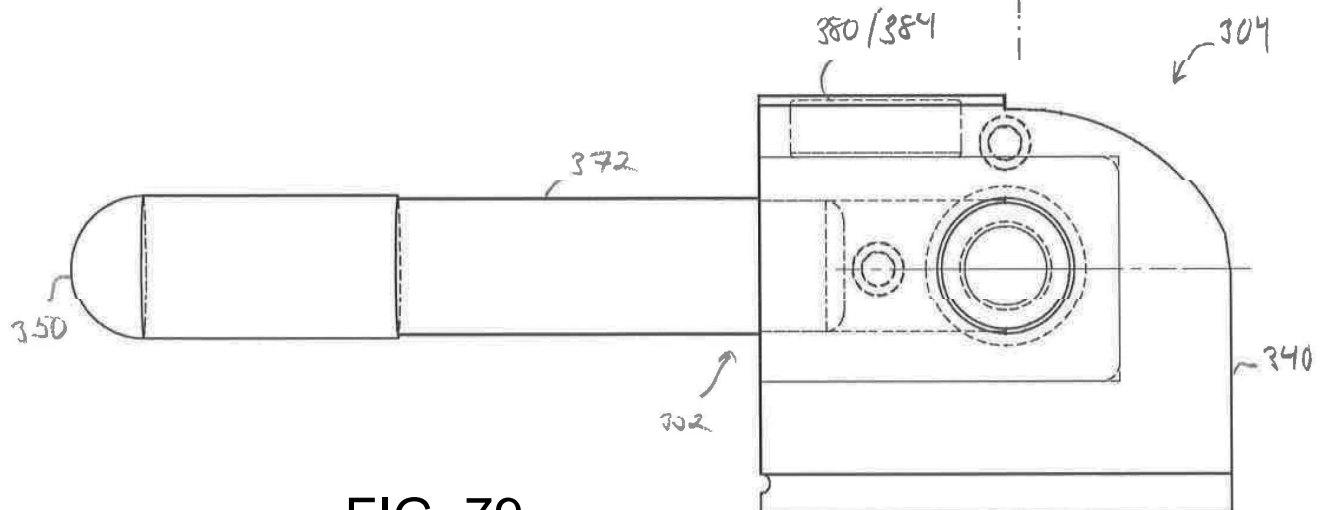


FIG. 79

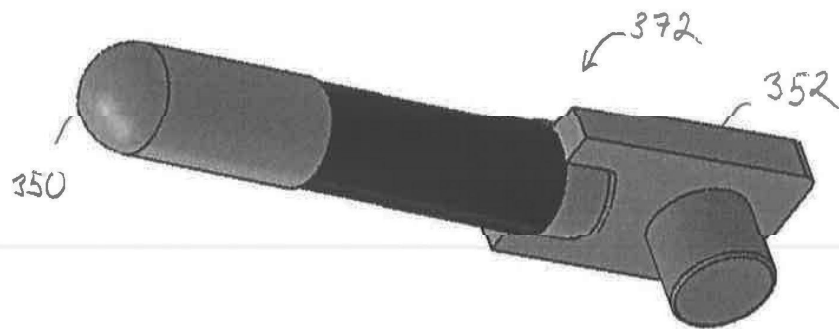


FIG. 80

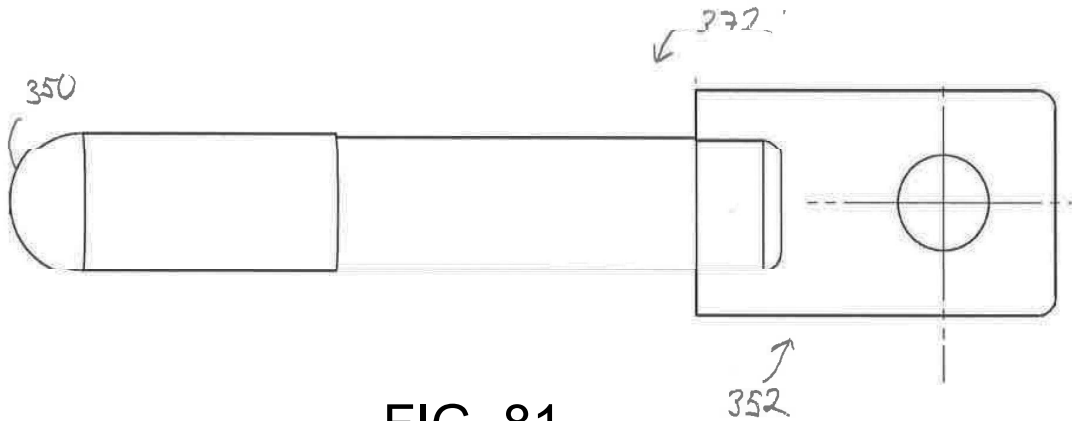


FIG. 81

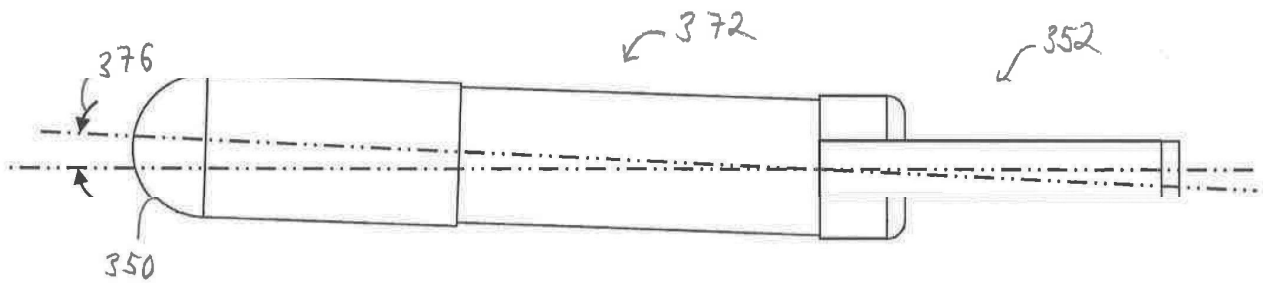


FIG. 82

FIG. 83

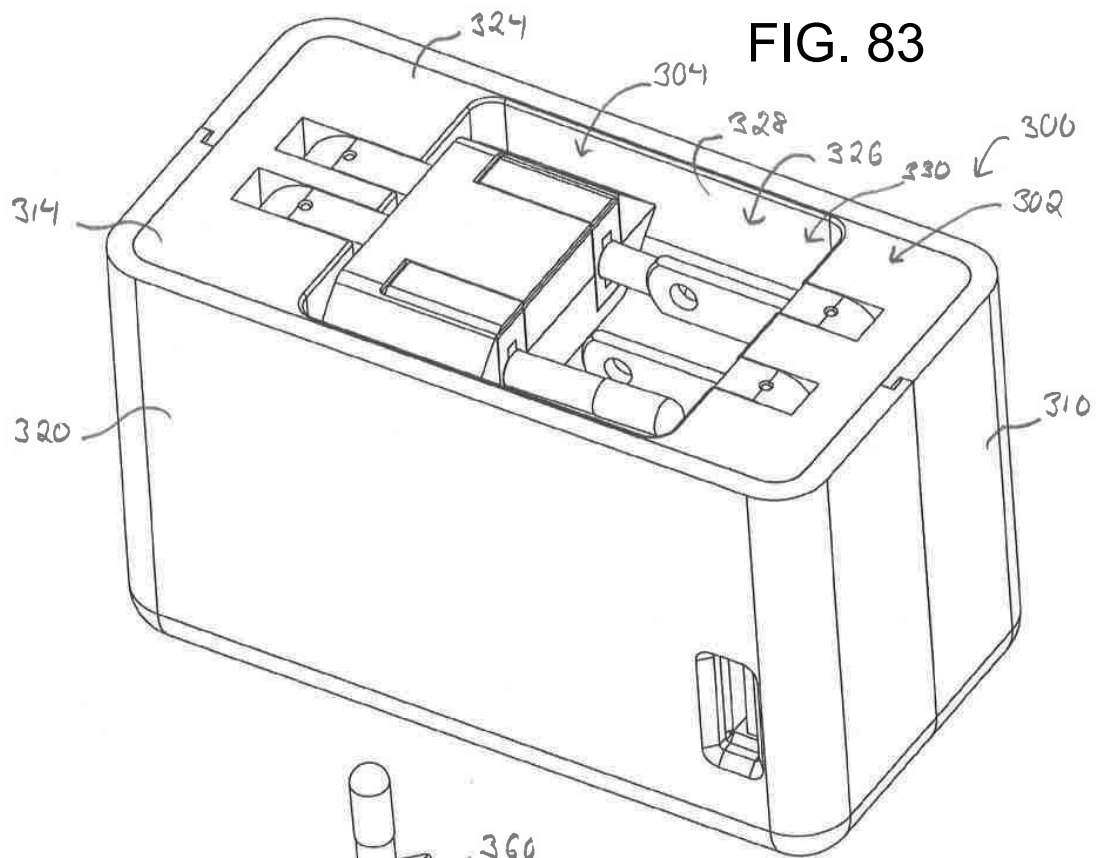


FIG. 84

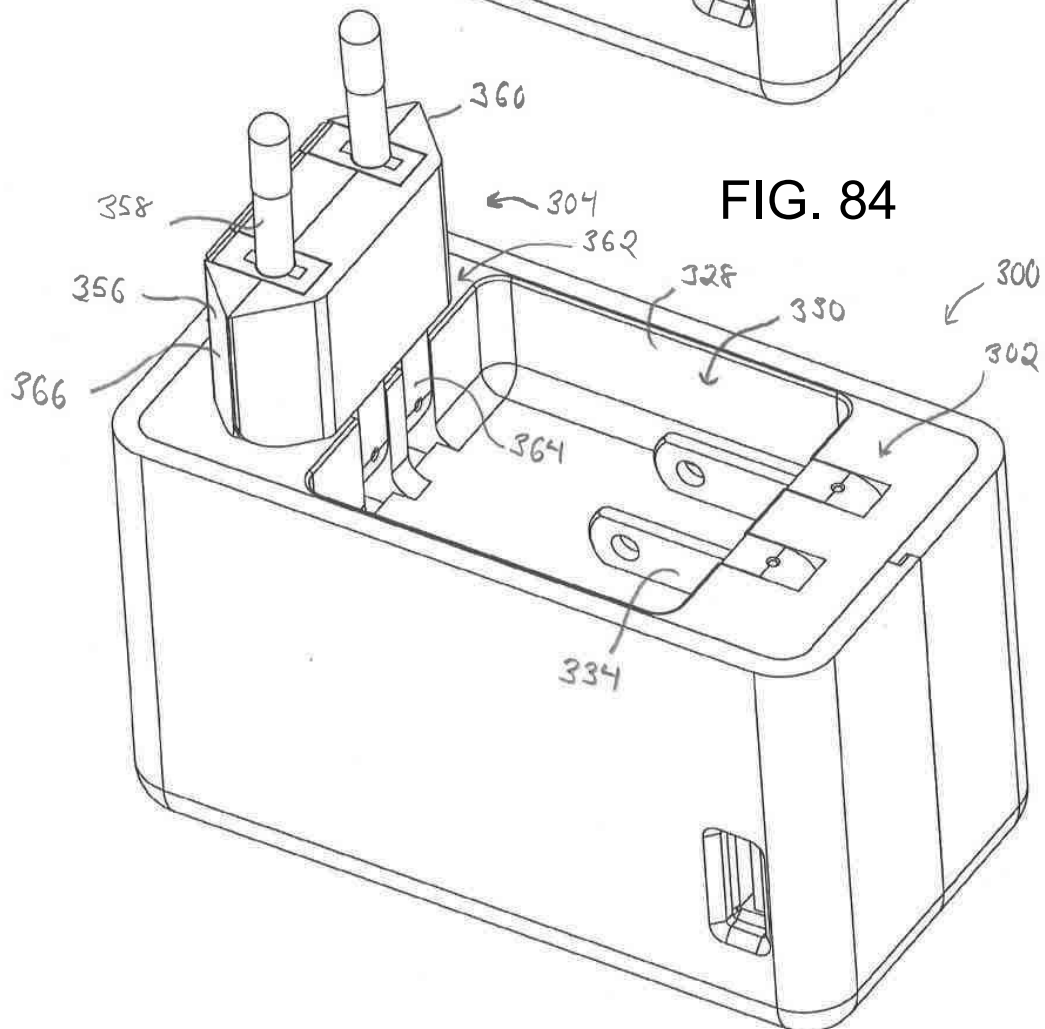


FIG. 85

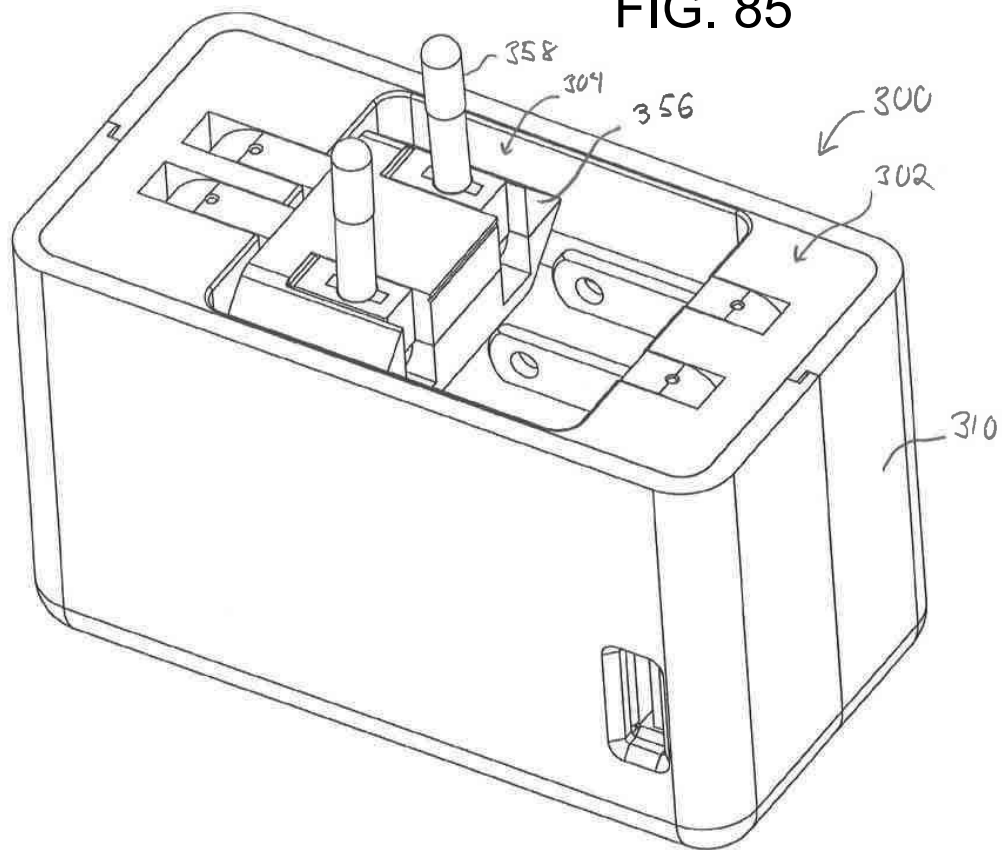
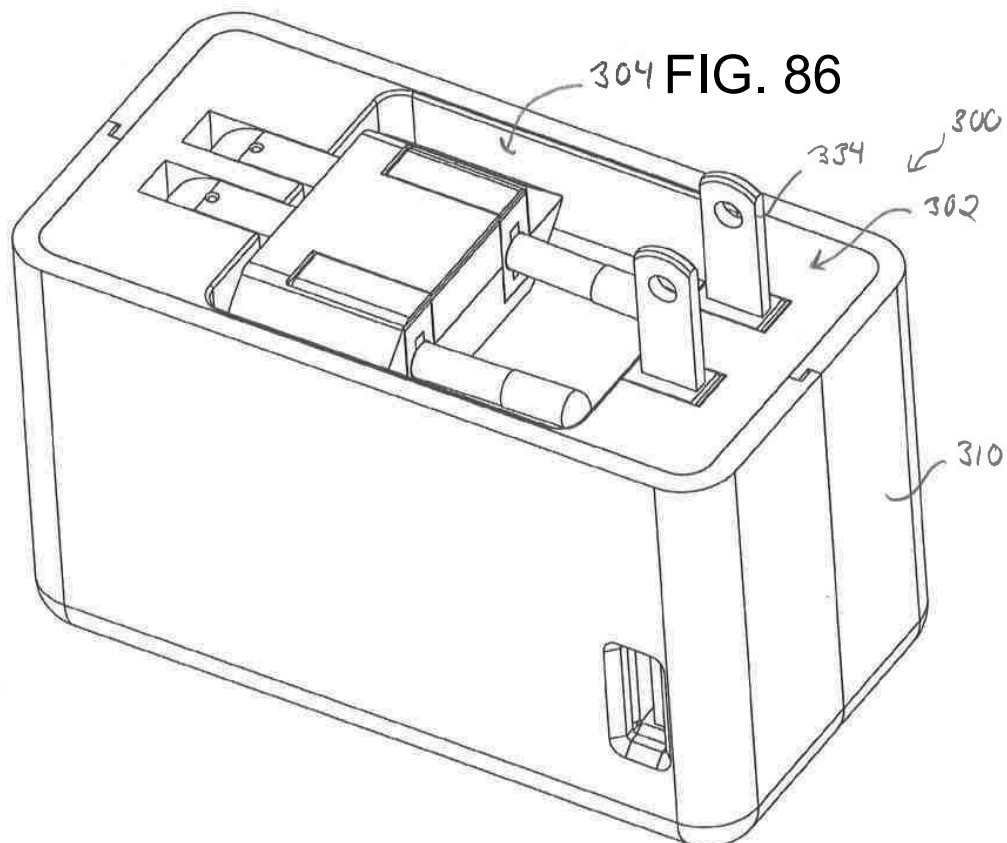
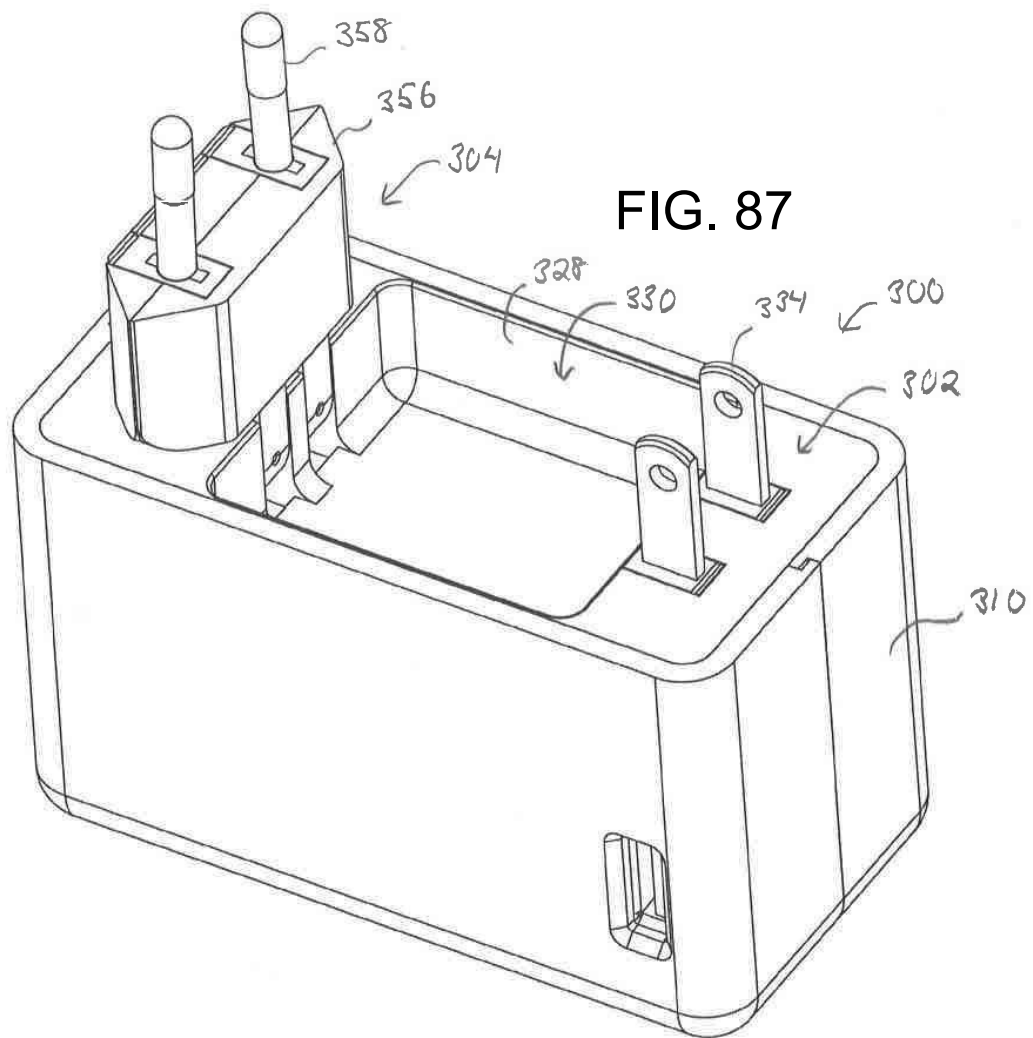


FIG. 86





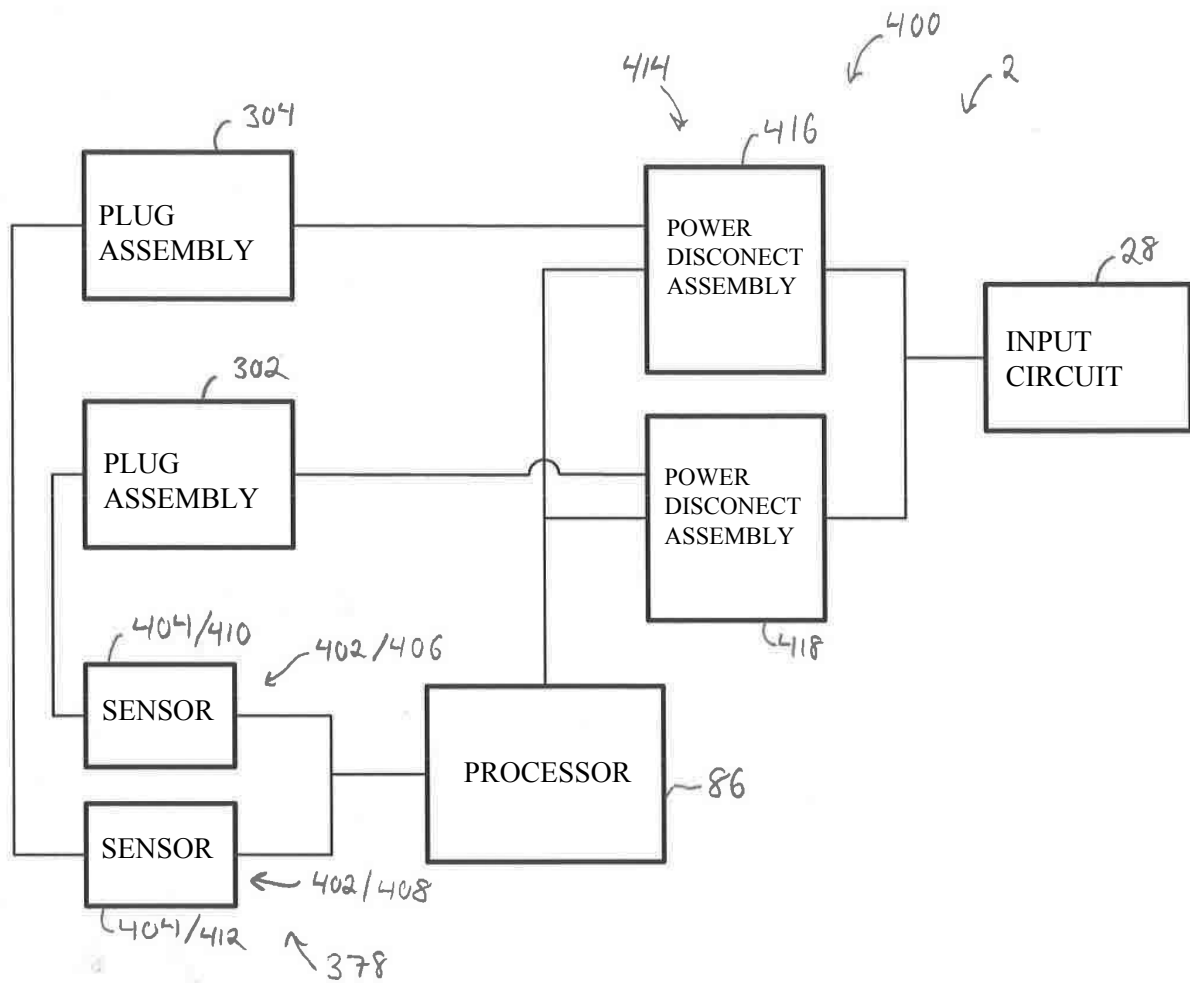


FIG. 88

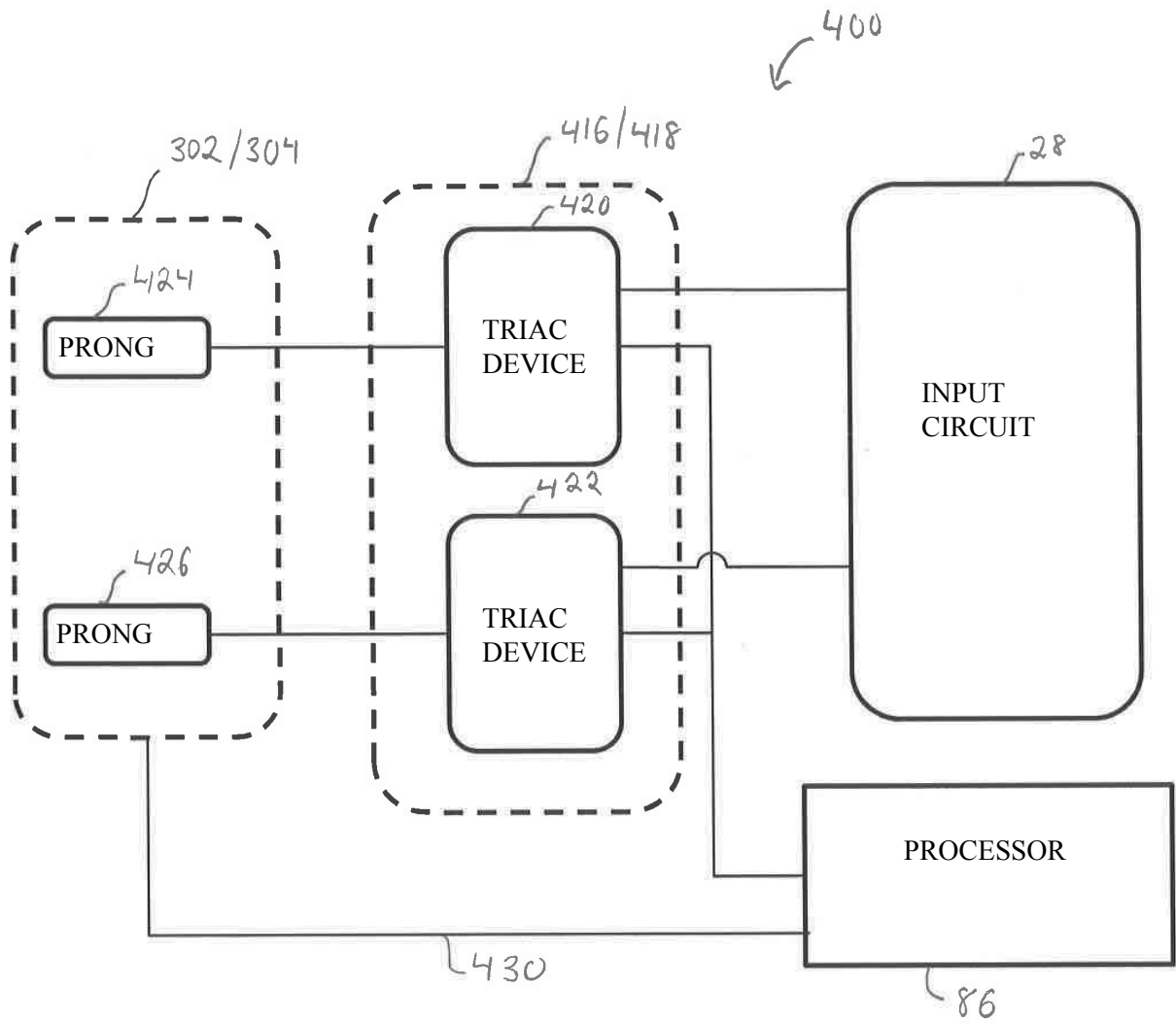


FIG. 89

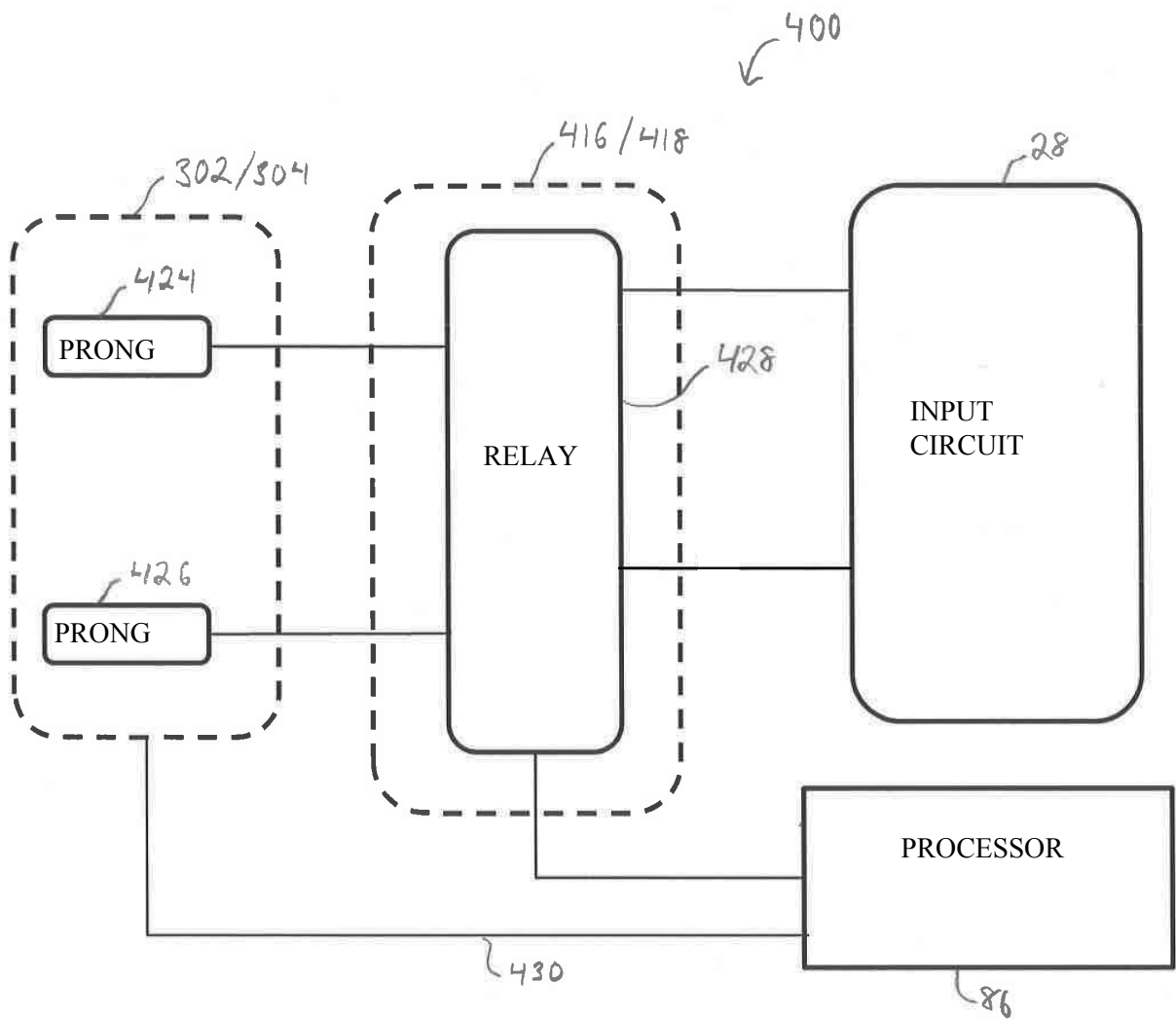


FIG. 90

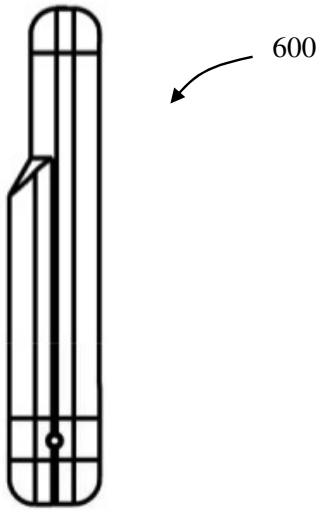


FIG. 91

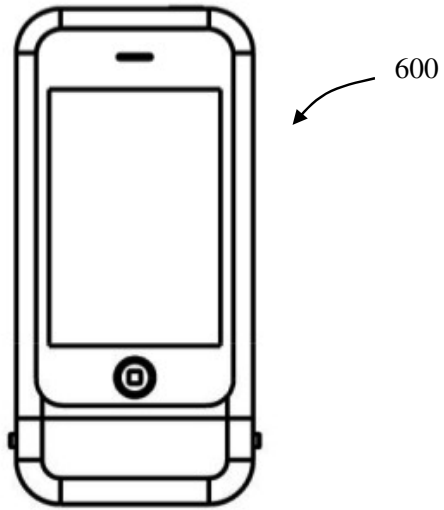


FIG. 92

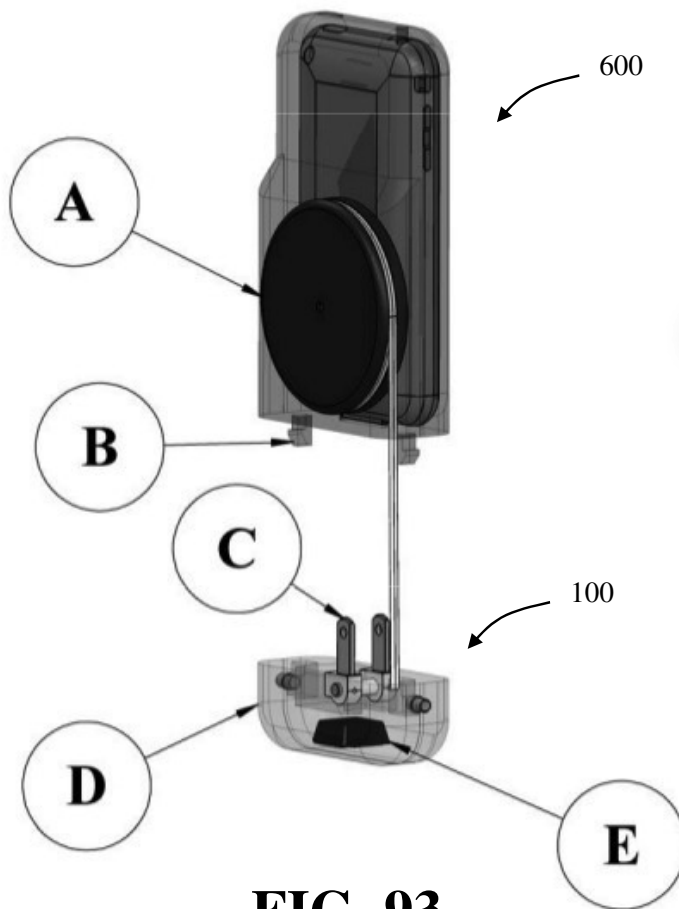


FIG. 93

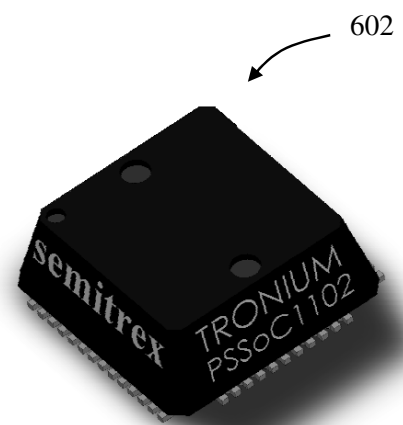


FIG. 94