

ABSTRACT

A resistive memory device includes a memory cell array, control logic, a voltage generator, and a read-out circuit. The memory cell array includes memory cells connected to bit lines. Each memory cell includes a variable resistance element to store data. The control logic receives a read command and generates a voltage control signal for generating a plurality of read voltages based on the read command. The voltage generator sequentially applies the read voltages to the bit lines based on the voltage control signal. The read-out circuit is connected to the bit lines. The control logic determines values of data stored in the memory cells by controlling the read-out circuit to sequentially compare values of currents sequentially output from the memory cells in response to the plurality of read voltages with a reference current.

FIG. 1