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PATENT SPECIFICATION

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(54) IMPROVEMENTS IN OR RELATING TO ELECTRONIC ALARM TIMEPIECES

(71) We, KABUSHIKI KAISHA DAINISEIKOSHA, a Japanese company, of 31-1, 6-chome, Kameido, Koto-ku, Tokyo, Japan, do hereby declare the invention for which we pray that a patent may be granted to us and the method by which it is to be performed to be particularly described in and by the following statement:—

This invention relates to electronic alarm timepieces, that is to say to electronic timepieces which will give an alarm when a preset alarm time is reached.

Electronic timepieces are of two main kinds, namely those which display days, hours and minutes and those which display hours and minutes only. In conventional multi-alarm electronic timepieces different control systems have had to be provided for setting the alarm times in a plurality of memory channels according as to whether the timepiece has a display displaying days, hours and minutes or has a display displaying hours and minutes without a day display. In other words, two different kinds of control system have had to be provided namely (a) a control system which produces a control signal in respect of days, hours and minutes, and (b) a control system which produces a control signal in respect of the hours and minutes of a predetermined time.

The present invention seeks to avoid the necessity of having to provide two different kinds of control system for the two different kinds of electronic alarm timepiece and to provide a relatively simple single control system which can be used for alarm time setting in either kind of timepiece, thus simplifying the circuitry and permitting the common use of circuits in both kinds of timepiece.

According to this invention there is provided an electronic alarm timepiece comprising a time counting system; a plurality of selectable alarm time setting memory system channels for setting a plurality of alarm times; means for giving an alarm when a time counted by the time

counting system coincides with a set alarm time in an alarm time setting memory system channel; channel display means one for each channel for displaying a selected memory system channel and means for displaying the set time content thereof when said channel is selected and for causing intermittent (i.e. on and off) display of the selected channel when coincidence occurs.

The whole timepiece arrangement may be such that, when the turning on and off of the display of the selected channel occurs, there is no display of the other channel or channels or it may be such that said display of said other channel or channels is constant.

The timepiece may have a time modification circuit including a counter arranged to act as a trinary counter for producing a control signal for modifying days, hours and minutes in time modification and as a binary counter when an alarm time is set by selecting a memory system channel.

The invention is illustrated in the accompanying drawings which show, so far as is necessary to an understanding of the invention, one embodiment, Figure 1 being a block logic diagram and Figure 2 being a more detailed circuit diagram.

Referring to Figure 1, the watch therein represented has a relatively high frequency quartz crystal controlled time standard oscillator 1, the output of which is fed to a divider 2 which produces a 1Hz output signal. This signal is fed to a seconds counter 3 followed by a switch 7 (represented as though it were a mechanical switch although in practice it is an electronic switching circuit) which, when in one switching position feeds output from counter 3 into a minutes counter 4. 5 is an hours counter which is connectable to the counter 4 by another switch 8 like the switch 7 and 6 is a day counter which is connectable to the hours counter 5 through a third switch 9 like the switches 7 and 8. The switches 7, 8 and 9 are controlled

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by control signals from minute, hour and day displayed time modification circuits 22, 23 and 24 respectively. The switches 7, 8 and 9 are electronic switching circuits composed of transmission gates and are adapted, when they are on the lower "contacts" shown in Figure 1, to change the counts in the following respective counters 4, 5 and 6 under the control of the time modification circuits 22, 23 and 24 respectively, by utilising a 1Hz signal which is fed as shown to the said lower "contacts" from the output of the divider 2.

25, 26 and 27 are channel selection control circuits and 10, 11, 12 and 16, 17 and 18 are memories. Suppose it is required to modify the time in No. 1 channel which is that to which channel selection control circuit 25 applies. Memories 16 and 10 are first selected by the selection control circuit 25. Memory 16 is a minute counter and the memory 10 is an hour counter. Time modification is performed as regards the hour setting by feeding in the 1Hz signal from divider 2 to the hours counter 10 through an AND gate 13 which receives one of its three inputs from the control circuit 25. After hour setting is finished, minute setting is performed by a similar process involving selection of the minutes memory 16 by a control signal from the time modification control circuit 25 and feeding memory 16 with 1Hz signals through an AND gate 19. As will be more clearly appreciated later, the AND gates 13, 14, 15, 19, 20 and 21 in the paths to the hours memories 10, 11, 12 and the minutes memories 16, 17 and 18 respectively serve to select the memory to which the 1Hz signal is fed. Memories 16 and 10 are the No. 1 channel memories; 17 and 11 are the No. 2 channel memories; and 18 and 12 are the No. 3 channel memories.

Referring to Figure 2 which shows the circuitry in more detail, and in which circuit elements belonging to the three channel memories are indicated by the general references M_1 , M_2 and M_3 , the time modification circuits 22, 23 and 24 are trinary counters constituted by D-type flip-flops, but, when the content of a memory is selected, i.e. one of the channel selection control circuits 25, 26 or 27 is selected, the trinary counter in question is turned into a binary counter by changing over the function of one of the transmission gates shown and then produces an hour or minute modification signal. The channel selection control circuits 25, 26 and 27 are also D-type flip flops. For display of the time of day and of the contents of the memories (the display device itself is not shown in Figure 2) display, all the outputs of the channel selection control circuits are digital "0" and therefore the output of a NOR circuit 30,

which receives said outputs, is "1" and this output, applied to the transmission gates as shown causes the time modification control circuits 22, 23 and 24 to act as trinary ring counters.

A "1" pulse signal produced by closure of the channel selection switch SW_1 is fed as a clock input to the channel selection control circuit 25, the output of which accordingly becomes "1". Also the count contents in the No. 1 channel are displayed. In addition, the output of the NOR circuit 30 changes to '0' and this causes the time modification control circuits 22, 23 and 24 to act as binary counters. A switch SW_2 serves both as a reset switch and as a safety switch. While this switch is closed, days, hours and minutes are displayed on the time display unit of the timepiece and time is counted in the ordinary way.

There will now be described the way in which the display provided by the digital display unit assumed to be a liquid crystal display unit, is controlled to indicate which channel contents is displayed. The display unit, which is a three-channel display unit, is only diagrammatically represented by electrodes S_1 , S_2 , S_3 for channels Nos. 1, 2 and 3 respectively, and a common counter electrode SS. For the sake of brevity of explanation only the case in which channel No. 1 is selected will be described. If the channel selection control circuit 25 is selected by pushing the channel selection switch SW_1 once, the output of said circuit 25 becomes "1". This "1" is fed in to one input of a NAND circuit 31, the other input of which is a 1 Hz signal from the divider 2. The output of the said NAND circuit 31 is therefore a 1Hz signal but there is no output from NAND circuit 32 or 33 because the outputs of channel selection control circuits 26 and 27 are still "0". The output of NAND circuit 31 is passed to one input of a NOR circuit 34 which produces at its output the 1 Hz signal inverted if the other input of NOR circuit 34 is "0". The 1 Hz output from 34 is applied to the No. 1 channel display driver 41. There are three channel display drivers 41, 42 and 43 and each comprises, as shown for driver 41, two AND circuits 37, 38, an inverter 37' and a NOR circuit 39. The 1 Hz output from 34 is applied directly to one input of 38 and through inverter 37' to one input of 37. A 32 Hz signal taken from the divider 2 is applied directly to the other input of 37 and, through an inverter 40, to the other input of 38. The outputs of 37 and 38 are fed to the respective inputs of the NOR circuits 39, the output from which is fed to S_1 . The 32 Hz signal from divider 2 is also fed at 44 to the common electrode SS. Accordingly an intermittent display appropriate to channel No. 1, i.e. between S_1 and SS, will be given, the said display

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going on and off every second. There will be no display at S_2 or S_3 because the voltages thereon will be in the same phase as that on the common electrode SS.

It is not essential for the non-selected channels (Nos. 2 and 3 in the foregoing example) to be arranged to give no display for the circuitry may be so modified that, instead of applying voltages in phase to S_2 and S_3 and to the common electrode SS, a fixed voltage is applied between S_2 and S_3 on the one hand and the common electrode SS on the other. It is not thought necessary to illustrate this modification which, for obvious reasons of increased power consumption, is not preferred.

There will now be described the indicating operation which shows which channel number coincides with the turning on and off of a channel display.

The apparatus for this comprises reset flip-flop circuits 80, 81 and 82 for memorising the presence of a stored memory in each channel; NOR circuits 61, 63 and 67, OR circuits 64, 68 and 69, and three input AND circuits 62, 65 and 66. Again, in order to simplify the description, the operation with respect to only the No. 1 channel will be described.

At first, when the safety switch SW_2 is closed and no selection of the memories for the hours and minutes displays has been made, the output of a NAND circuit 70 will be "0". Also if there is no content in the No. 1 channel, i.e. the R-S flip-flop 80 is in reset condition, the output of NOR circuit 55 in that flip-flop is "1", and the output of NOR circuit 61 is "0". This is fed to one input of the OR circuit 64, the other input to which is the output of the AND circuit 62. One of the inputs to said AND circuit 62 is the 1Hz signal from the divider 2, another is the output from a NOR circuit 52 which is cross-connected with another NOR circuit 51 to form an R-S flip-flop. 50 is a coincidence control circuit providing one input to the flip-flop 51-52, the other input to which is taken from the divider 2. In the absence of coincidence between set alarm time and counted time the output of the NOR circuit 51 is "1", the output of the AND circuit 62 is "0" and the output of the OR circuit 64 is "0". Display occurs when the output of NOR circuit 34 is "0" and that of 52 is "1". Now suppose there is some stored memory content in the No. 1 channel. The clock pulse (obtained by closure of switch SW_3) used to set the No. 1 channel is also fed in to the set-input terminal SI of the R-S flip-flop 80. The output from the NOR circuit 55 in this flip-flop becomes "0" due to the presence of stored memory, the output of the OR circuit 64 becomes "1" and the display for the No. 1 channel becomes activated steadily, i.e.

without turning on and off. When a set alarm time coincides with current counted time the coincidence signal produced by the coincidence control circuit 50 (this circuit may be arranged as well known per se to respond to such coincidence and is only diagrammatically represented) is fed in to the flip-flop NOR circuit 51 and the output of NOR circuit 52 becomes "1". This is used as a reset signal which resets the No. 1 channel stored memory thus "clearing off" its content. This reset "1" signal from 52 is also fed to the reset terminal R, of the NOR circuit 56, the output of NOR circuit 55 again becomes "1", the output of NOR circuit 61 becomes "0". This is fed in to one input of the OR circuit 64. The reset "1" signal from 52, applied at terminal R, is also fed to the remaining (third) input of AND circuit 62. The AND circuit 62 can therefore produce a 1Hz output signal only when the output of the NOR circuit 52 is "1" and consequently a turn-on-and-off display is given for the No. 1 channel. The time during which the said "turn-on-and-off" display continues can be repeated and brought to an end, after a predetermined time, by applying a short pulse signal formed by a latching circuit (not shown) actuated by a signal from the seconds counter after said predetermined time to the NOR circuit 52 so as to cause the channel display and the sound alarm (if any) to stop after a certain number of repetitions. As shown a sound alarm is given by a sound source 100 driven through a transistor, an inverter 54 and a NAND circuit 53, the said NAND circuit receiving as input a comparatively high frequency from the divider 2 and a lower frequency such as 16Hz from the NOR circuit 52.

As will now be seen, the arrangement described achieves improved circuit simplicity, having regard to the performance obtained, by use of a time modification control system both in the time counting part of the timepiece and the selection control system for setting the hours and minutes time of the alarm. It also has the advantage of simplifying the switching operations the user has to perform.

Further, as will also be seen, when a particular channel is selected, the corresponding channel display goes on-and-off which is more noticeable to the user than the customary steady light channel display given by some known digital alarm electronic timepieces. Again, the arrangement is made such that when the time counting signal coincides with the set alarm time in the selected channel, the corresponding channel display repeats an on and off operation and, at the end of a predetermined time turns off altogether and

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at the same time the sounding of the alarm is caused to cease. At the time when a preset alarm is produced the hours and minutes displayed by the channel displays flash on and off at the time the alarm is produced thus clearly indicating which channel alarm setting has been reached so that the user finds it easy to remember why that particular channel time was set.

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WHAT WE CLAIM IS:—

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1. An electronic alarm timepiece comprising a time counting system; a plurality of selectable alarm time setting memory system channels for setting a plurality of alarm times; means for giving an alarm when a time counted by the time counting system coincides with a set alarm time in an alarm time setting memory system channel; channel display means, one for each channel for displaying a selected memory system channel and means for displaying the set time content thereof when said channel is selected and for intermittent i.e. on and off display of the selected channel only when coincidence occurs.

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2. A timepiece as claimed in claim 1

wherein when the turning on and off of the display of the selected channel occurs, there is no display of the other channel or channels.

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3. A timepiece as claimed in claim 1 wherein when the turning on and off of the display of the selected channel occurs, the display of the other channel or channels is constant.

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4. A timepiece as claimed in any of the preceding claims wherein there is a time modification circuit including a counter arranged to act as a trinary counter for producing a control signal for modifying days, hours and minutes in time modification and as a binary counter when an alarm time is set by selecting a memory system channel.

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5. Electronic alarm timepieces substantially as herein described and illustrated in the accompanying drawings.

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1. An electronic alarm timepiece comprising a time counting system; a plurality of selectable alarm time setting memory system channels for setting a plurality of alarm times; means for giving an alarm when a time counted by the time counting system coincides with a set alarm time in an alarm time setting memory system channel; channel display means, one for each channel for displaying a selected memory system channel and means for displaying the set time content thereof when said channel is selected and for intermittent i.e. on and off display of the selected channel only when coincidence occurs.

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