WHAT IS CLAIMED IS:

1. A method of programming a three-dimensional (3D) nonvolatile memory device including a cell string, the cell string including a pillar structure comprising a ground selection transistor, a plurality of memory cells, and a string selection transistor sequentially stacked in a direction that is perpendicular to a substrate, wherein the memory cells comprise a first cell group and a second cell group stacked on the first cell group, and wherein a horizontal width of at least a portion of the pillar structure decreases in a depth direction towards the substrate, the method comprising:

initializing a channel of a memory cell of the first cell group of the cell string through the ground selection transistor of the pillar structure; and then

applying a program voltage to the memory cell of the pillar structure of the cell string.

2. The method of claim 1, further comprising sequentially executing said initializing and said applying for each of remaining memory cells of the first cell group of the cell string which are to be programmed among the memory cells of the first cell group of the cell string.

3. The method of claim 2, wherein a horizontal width of the pillar structure decreases in the depth direction from the string selection transistor to the ground selection transistor, and wherein the memory cells of the cell string are sequentially programmed in order from an uppermost memory cell furthest from the substrate to a lowermost memory cell closest to the substrate by sequentially executing said initializing and said applying for each of the memory cells of the cell string.

4. The method of claim 1, wherein a horizontal width of an uppermost memory

cell of the first cell group is greater than a horizontal width of an adjacent lowermost memory cell of the second cell group, the method further including:

sequentially programming the memory cells of the cell string in order from an uppermost memory cell of the second cell group furthest from the substrate to a lowermost memory cell of the first cell group closest to the substrate by sequentially executing said initializing and said applying for each of the memory cells of the cell string.

5. The method of claim 1, wherein a memory cell having a smallest horizontal width among the memory cells of the first cell group is programmed with fewer bits than a memory cell having a largest horizontal width of the memory cells of the first cell group.

6. The method of claim 1, wherein a memory cell having a smallest horizontal width among the memory cells of the second cell group is programmed with fewer bits than a memory cell having a largest horizontal width of the memory cells of the second cell group.

7. The method of claim 1, wherein the method includes incremental step pulse programming (ISPP) comprising a plurality of program loops, and wherein a second program operation for programming the memory cell during a first portion of the program loops is different from a fourth program operation for programming the memory cell during a second portion of the program loops, wherein a voltage applied to a common source line of the cell string is different between the second and fourth program operations.

8. A three dimensional non-volatile memory device, comprising:

a memory cell array including a cell string, the cell string including a pillar structure comprising a ground selection transistor, a plurality of memory cells, and a string selection

transistor sequentially stacked in a direction perpendicular to a substrate, wherein the memory cells comprise a first cell group and a second cell group stacked on the first cell group, and wherein a horizontal width of at least a portion of the pillar structure decreases in a depth direction towards the substrate;

an address decoder configured to supply string selection line voltage to the string selection transistor, word line voltages to word lines connected to the memory cells, ground selection line voltages to the ground selection transistor, and a common source line voltage to a common source line of the memory cell array;

a page buffer circuit configured to output bit data from selected ones of the memory cells of the memory cell array;

control logic; and

a voltage generator configured to supply voltages to the address decoder in response to the control logic,

wherein the memory device is configured to initialize a channel of a memory cell of the first cell group of the cell string through the ground selection transistor of the pillar structure, and then apply a program voltage to the memory cell of the pillar structure of the cell string.

9. The memory device of claim 8, wherein the memory device is configured to sequentially initialize the channel through the ground selection transistor, and then apply the program voltage, for each of remaining memory cells of the first cell group of the cell string which are to be programmed among the memory cells of the first cell group of the cell string.

10. The memory device of claim 9, wherein a horizontal width of the pillar structure decreases in the depth direction from the string selection transistor to the ground

selection transistor, and wherein the memory device is configured to sequentially program the memory cells of the cell string in order from an uppermost memory cell furthest from the substrate to a lowermost memory cell closest to the substrate by sequentially initializing the channel through the ground selection transistor, and then applying the program voltage, for each of the memory cells of the cell string.

11. The memory device of claim 8, wherein a horizontal width of an uppermost memory cell of the first cell group is greater than a horizontal width of an adjacent lowermost memory cell of the second cell group, and wherein the memory device is configured to:

sequentially program the memory cells of the cell string in order from an uppermost memory cell of the second cell group furthest from the substrate to a lowermost memory cell of the first cell group closest to the substrate by sequentially initializing the channel through the ground selection transistor, and then applying the program voltage for each of the memory cells of the cell string.

12. The memory device of claim 8, wherein the memory device is configured to program a memory cell having a smallest horizontal width among the memory cells of the first cell group with fewer bits than a memory cell having a largest horizontal width of the memory cells of the first cell group.

13. The memory device of claim 8, wherein a memory cell having a smallest horizontal width among the memory cells of the second cell group is programmed with fewer bits than a memory cell having a largest horizontal width of the memory cells of the second cell group.

14. The memory device of claim 8, wherein the memory device is configured to program the memory cell using incremental step pulse programming (ISPP) comprising a plurality of program loops, and wherein a second program operation for programming the memory cell during a first portion of the program loops is different from a fourth program operation for programming the memory cell during a second portion of the program loops, wherein a voltage applied to a common source line of the selected memory string is different between the second and fourth program operations.

15. A method of programming a three-dimensional (3D) nonvolatile memory device, including a memory cell array having a plurality of cell strings each connected to one of a plurality of bit lines, the cell strings each including a pillar structure comprising a ground selection transistor, a plurality of memory cells each connected to one of a plurality of word lines, and a string selection transistor sequentially stacked in a direction perpendicular to a substrate, wherein the memory cells of each cell string comprise a first cell group and a second cell group stacked on the first cell group, and wherein a horizontal width of at least a portion of the pillar structure decreases in a depth direction towards the substrate, the method comprising:

providing bit line voltages to the bit lines to select one of the bit lines;

supplying string selection line voltages to string selection transistors of cell strings connected to the selected bit line to select one of the cell strings; and

precharging the pillar structure of the selected cell string through the ground selection transistor of the pillar structure, and then applying word line voltages to the word lines connected to the memory cells of the cell string to program a selected memory cell.

16. The method of claim 15, further comprising sequentially executing said

providing, supplying, precharging and applying for each of remaining memory cells of the selected cell string which are to be programmed among the memory cells of the selected cell string.

17. The method of claim 16, wherein a horizontal width of the pillar structure decreases in the depth direction from the string selection transistor to the ground selection transistor, and wherein the memory cells of the cell string are sequentially programmed in order from an uppermost memory cell furthest from the substrate to a lowermost memory cell closest to the substrate by sequentially executing said providing, supplying, precharging and applying for each of the memory cells of the cell string.

18. The method of claim 15, wherein a horizontal width of an uppermost memory cell of the first cell group is greater than a horizontal width of an adjacent lowermost memory cell of the second cell group, the method further including:

sequentially programming the memory cells of the cell string in order from an uppermost memory cell of the second cell group furthest from the substrate to a lowermost memory cell of the first cell group closest to the substrate by sequentially executing said initializing and said applying for each of the memory cells of the cell string.

19. The method of claim 15, wherein a memory cell having a smallest horizontal width among the memory cells of the second cell group is programmed with fewer bits than a memory cell having a largest horizontal width of the memory cells of the second cell group.

20. The method of claim 15, wherein the method of programming the memory cell includes incremental step pulse programming (ISPP) comprising a plurality of program loops,

and wherein a second program operation for programming the memory cell during a first portion of the program loops is different from a fourth program operation for programming the memory cell during a second portion of the program loops, wherein a voltage applied to a common source line of the cell string is different between the second and fourth program operations.