

ABSTRACT

A semiconductor device includes a peripheral circuit structure disposed on a substrate; a lower stack disposed on the peripheral circuit structure and an upper stack disposed in the lower stack, the lower stack including a plurality of lower insulating layers and a plurality of lower word lines alternately stacked with the lower insulating layers; a plurality of channel structures extending through the lower stack and the upper stack in the cell array area; a pair of separation insulating layers extending vertically through the lower stack and the upper stack and extending in a horizontal direction, the pair of separation insulating layers being spaced apart from each other in a vertical direction; and a word line separation layer disposed at an upper portion of the lower stack and crossing the pair of separation insulating layers when viewed in a plan view, the word line separation layer extending vertically through at least one of the lower word lines.

FIG. 1