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INTEGRATED CIRCUIT ARRAY

This invention relates to integrated circuits (ICs) and, in particular, to integrated circuit arrays.

5 Within the past 20 years the speed at which computers can operate has increased by many orders of magnitude while their cost has decreased equally dramatically. All of this has been made possible by the invention of semiconductor devices and the development of integrated circuits. By means of this technology
10 many thousands of circuit elements can be fitted onto a chip of semiconductor material measuring only a fraction of an inch on each side. Typically, hundreds of such circuits are made simultaneously side-by-side, on a common wafer. The yield in such a process, however, tends to decrease as the packing density and the size of
15 each chip is increased. In addition, heat dissipation tends to become a problem as the packing density is increased. Finally, as the elements proliferate, more and more of the chip surface area is taken up by the interconnecting leads. On present day ICs, anywhere from 30 to 90 percent of the chip can be so occupied. Furthermore,
20 as the chip size increases, the increased lead lengths become a limiting factor determining the speed at which the device can operate.

In the invention as claimed the chips form an array in which two-way coupling between the chips is effected optically. This
25 permits the use of smaller, less densely packed chips, resulting in correspondingly higher yields. In addition, the use of smaller, less densely packed chips serves to reduce the chip surface area required by the interconnecting leads. It also reduces the lengths of the interconnection lead, thereby permitting higher operating
30 speeds.

Some embodiments of the invention will now be described by way of example with reference to the accompanying drawings in which:-

FIG. 1 shows an exploded view of an optically coupled array of
35 integrated circuits according to the invention;

FIG. 2 shows a section through the array of FIG. 1;

FIGS. 3 to 5 show illustrative embodiments of LEDs and photodetectors for use in such arrays; and

FIG. 6 shows the use of focussing means in a coupling aperture.

5 Referring to the drawings, FIG. 1 shows an exploded view of a three-dimensional array 10 of n integrated circuit chips 11-1, 11-2 ... 11- n , in accordance with the present invention. The chips are disposed between heat sinks 12-1, 12-2 ... 12- $(n + 1)$ with their broad planar surfaces parallel to and in contact with the planar
10 surfaces of the adjacent heat sinks.

Each of the chips is provided with the necessary electrical connectors, such as 13 and 14, for providing electrical power to the circuits and, where appropriate, for coupling information signals into and out of the array. Signals can also be coupled into and out
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optically by means of optical fibres 16 and 17. In addition, optical means are employed to couple signals among the integrated circuits of the array. This is shown in greater detail in FIG. 2 which is a section taken through the array. Using the same identification numerals as are used in FIG. 1 to identify corresponding components, FIG. 2 shows fibre 16 extending through an aperture 20 in heat sink 12-1 and a photodetector 21 incorporated into chip 11-1 for receiving radiant energy emitted from fibre 16. Also shown incorporated into chips 11-1 and 11-2 are LEDs 22 and 25 and associated photodetectors 19, 24 and 27. Radiant energy is coupled between LED 22 and detector 24 through an aperture 23 in heat sink 12-2. Similarly, radiant energy is coupled between LED 25 and detector 27 through an aperture 26 in heat sink 12-2. In addition, radiant energy from source 22 is shown directed downward to a detector 19 on chip 11-n through apertures, such as 28 and 29, in the intervening chips and heat sinks. By this means signals can be readily coupled among the chips without requiring conductive leads which, in prior art chips, must be run from the originating portion of the integrated circuit to the perimeter of the first chip, through an external connection to the perimeter of the second chip, and then to the receiving location of the second integrated circuit. In addition to using up space on the chips, the lead lengths involved in making these connections tend to place an upper limit upon the operating speed of the resulting circuit.

IC chips 11-1 through 11-n are substantially similar to present day IC chips except that they are preferably made from direct-gap semiconductor materials (e.g. GaAs, InP or InGaAsP) so that small, low-power LEDs and photodetectors can be included at various locations thereon. (See, for example, the article by F.H. Eisen entitled "Materials and processes for GaAs integrated circuits," Inst. Phys. Conf. Ser. No. 63 Chapter 11 Paper presented at Symp. GaAs and Related Compounds, Japan, 1981).

FIGS. 3 to 5 show in greater detail illustrative LED and photodetector structures for use in the arrays. In the device of FIG. 3 an epitaxial layer 30 of a first conductivity material, deposited upon a mesa 32 of opposite conductivity substrate material 31, forms a photodiode. For purposes of illustration, the substrate is characterized as n-type and the epitaxial layer as p-type material. The upper surface is covered with an insulating layer 33 in which an aperture is formed above layer 30. Ohmic contact to the photodiode is made by depositing a first metallic (e.g. gold) layer 35 above layer 30 and a second metallic layer 34 on the bottom surface of the substrate 31. Radiant energy is coupled into or out of the diode through an aperture 36 in layer 34.

When used as a signal emitter, a drive current is applied to upper contact 35, and radiant energy is extracted through the aperture 36 in the lower contact 34, as shown in FIG. 3. If used as a detector, radiant energy is directed onto the diode through the aperture 36 and the resulting output current appears on contact 35.

To focus the radiated energy derived from the photodiode, and thus preclude spurious cross coupling to other photodetectors, contact 35 advantageously extends down the side of mesa 32.

The device of FIG. 4 is basically the same as FIG. 3 comprising a layer 40 of n-type semiconductor material deposited upon a mesa of the underlying substrate 41 of p-type material to form a photodiode. Ohmic contact is made to the diode by means of a first metallic connector 44 through an aperture in an insulating layer 46, and a second metallic connector 47 in contact with the lower surface of substrate 41. In this device radiant energy is coupled into and out of the photodiode through an aperture 45 in the upper metallic connector 44.

FIG. 5 shows a planar diode configuration for use in connection with the present invention in which the photodiode is formed by diffusing a suitable dopant into

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the chip substrate 50 to form a region of opposite conductivity, for example, a p-type region 51 in an n-type substrate. A metallic connector 52 makes ohmic contact to region 51 through an aperture 58 in insulating layer 53. A
5 second metallic connector 55 makes ohmic contact to the bottom surface of the substrate.

In this device, radiant energy can be coupled into or out of the diode through insulating layer 53 and/or through an aperture 56 in the second metallic connector 55.
10 In this way, optical coupling can be simultaneously affected between a chip and two other oppositely situated chips in the array, or between a chip and a fibre, or any combination thereof.

It is an advantage of the arrangement described
15 that a large number of relatively small ICs can be assembled in a single package in a way that does not impair the speed of the arrangement. Inasmuch as the manufacturing yield for small chips is always greater than the yield of larger chips, a greater percentage of
20 processed wafers could be utilized in such an optically coupled array than would be the case if the same function was incorporated into a single larger chip. In addition, the packages for present day ICs are typically much larger than the IC chip within because of the need to
25 mechanically fan-out the many electrical connections. An optically coupled chip array, by contrast, can be made with fewer external connections and can be designed so as to require only external d.c. connections and an optical fibre ribbon. Thus, smaller packages are
30 obtainable.

As shown in FIGS. 1 and 2, heat sinks can be provided between chips. If required, the heat sinks can be made thick enough to contain ducts for coolant fluids. In addition, a lens can be included in the coupling aperture
35 to increase the optical coupling efficiency, as illustrated in FIG. 6 wherein lens 60 is shown disposed in a coupling aperture 61. The latter can be located in either a chip or
38 a heat sink through which energy is being transmitted. The

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use of spherical glass lenses would eliminate the need for
orientational alignment during manufacture

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CLAIMS

1. An integrated circuit array comprising a plurality of integrated circuit chips, each having a pair of planar surfaces, the chips being stacked so that planar surfaces of each pair of adjacent
5 chips are substantially parallel and opposed to each other, and means for coupling between the chips comprising a plurality of radiation sources and radiation detectors distributed among the chips and including a first radiation source and a first radiation
10 detector located on a first chip and a second radiation source and a second radiation detector located on a second chip, such that the first radiation source can couple radiation to the second radiation detector and the second radiation source can couple radiation to the first radiation detector.

2. An array as claimed in claim 1 including a chip coupled by
15 means of said radiation sources and detectors directly to more than one other chip in the array.

3. An array as claimed in claim 1 or claim 2 including a pair of non-adjacent chips directly coupled by means of said radiation sources and detectors.

20 4. An array as claimed in any of the preceding claims including one or more heat sinks separating adjacent chips.

5. An array as claimed in claim 4 wherein the heat sinks have apertures therein containing lenses to facilitate coupling radiation sources and detectors.

25 6. An integrated circuit array substantially as herein described with reference to the accompanying drawings.

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